Precision, Low Noise, Low Profile Hermetic Voltage Reference

FEATURES

- Hermetic 5mm × 5mm LCC Leadless Chip Carrier Package:
  - Insensitive to Humidity
  - Thermal Hysteresis: 8ppm (0°C to 70°C)
  - Thermal Hysteresis: 60ppm (–40°C to 85°C)
- Low Drift:
  - A-Grade: 5ppm/°C Max
  - B-Grade: 10ppm/°C Max
- High Accuracy:
  - A-Grade: ±0.05% Max
  - B-Grade: ±0.10% Max
- Low Noise: <1ppm Peak-to-Peak (0.1Hz to 10Hz)
- 100% Noise Tested
- Sinks and Sources ±10mA
- Wide Supply Range to 40V
- 8-Pin (5mm × 5mm) LS8 Package

APPLICATIONS

- Instrumentation and Test Equipment
- High Resolution Data Acquisition Systems
- A/D and D/A Converters
- Precision Regulators
- Precision Scales
- Digital Voltmeters

DESCRIPTION

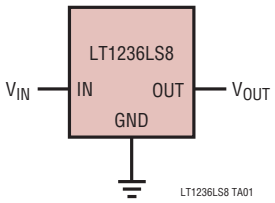
The LT®1236LS8 is a precision reference that combines low drift and noise with excellent long-term stability and high output accuracy. The reference output will both source and sink up to 10mA and remains very constant with input voltage variations.

The hermetic package provides outstanding humidity and thermal hysteresis performance. The LT1236LS8 is only 5mm × 5mm × 1.5mm, offering an alternative to large through-hole metal can voltage references, such as the industry standard LT1021. The LT1236LS8 offers similar performance to the LT1236, with additional stability from the hermetic package.

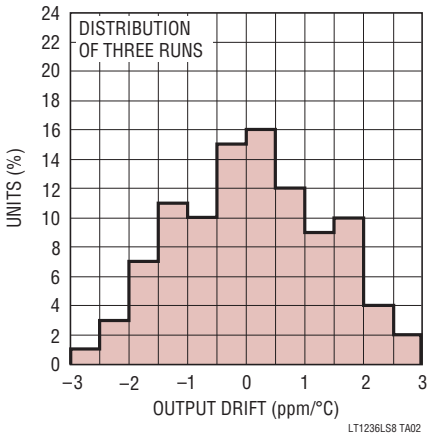
LT1236LS8 is based on a buried Zener diode structure, which enables temperature and time stability, and extremely low noise performance of < 1ppm peak-to-peak. Noise is 100% tested in production. The LT1236LS8 operates on a supply voltage from 7.2V up to 40V. The subsurface Zener exhibits better time stability than even the best bandgap reference, and the hermetic package maintains that stability over a wide range of environmental conditions.

TYPICAL APPLICATION

Basic Connection



Typical Distribution of Temperature Drift

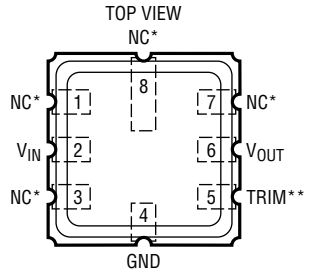


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage.....40V
Input/Output Voltage Differential 35V
Trim Pin-to-Ground Voltage
  Positive..... Equal to V_{OUT}
  Negative.....–20V
Output Short-Circuit Duration
  V_{IN} = 35V.....10 sec
  $V_{IN} \leq$ 20V..... Indefinite
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



LS8 PACKAGE
8-PIN LEADLESS CHIP CARRIER (5mm × 5mm)

*CONNECTED INTERNALLY.
DO NOT CONNECT EXTERNAL
CIRCUITRY TO THESE PINS

**SEE APPLICATIONS
INFORMATION SECTION

T_{JMAX} = 125°C, θ_{JA} = 120°C/W
PACKAGE LID IS GND

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1236AILS8-5#PBF†	12365	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 85°C
LT1236BILS8-5#PBF†	12365	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
†This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, I_{OUT} = 0, unless otherwise noted.

PARAMETER	CONDITIONS		LT1236LS8-5 MIN	LT1236LS8-5 TYP	LT1236LS8-5 MAX	UNITS
Output Voltage (Note 2)	LT1236ALS8		4.9975	5.000	5.0025	V
	LT1236BLS8		4.9950	5.000	5.0050	V
Output Voltage Temperature Coefficient (Note 3)	LT1236ALS8			2	5	ppm/°C
	LT1236BLS8			5	10	ppm/°C
Line Regulation (Note 4)	7.2V ≤ V_{IN} ≤ 10V			4	12	ppm/V
		●			20	ppm/V
	10V ≤ V_{IN} ≤ 40V			2	6	ppm/V
		●			10	ppm/V
Load Regulation (Sourcing Current) (Note 4)	0 ≤ I_{OUT} ≤ 10mA			15	25	ppm/mA
		●			40	ppm/mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, I_{OUT} = 0, unless otherwise noted.

PARAMETER	CONDITIONS		LT1236LS8-5 MIN	LT1236LS8-5 TYP	LT1236LS8-5 MAX	UNITS
Load Regulation (Sinking Current) (Note 4)	$0 \le I_{OUT} \le 10mA$	 ●		60	100 150	ppm/mA ppm/mA
Supply Current		 ●		0.8	1.2 1.5	mA mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz 10Hz ≤ f ≤ 1kHz			3.0 2.2	 3.5	μV_{P-P} μV_{RMS}
Long-Term Stability of Output Voltage (Note 6)	Δt = 1000Hrs Non-Cumulative			20		ppm
Temperature Hysteresis of Output (Note 7)	ΔT = ±25°C ΔT = 0°C to 70°C ΔT = –40°C to 85°C			3 8 60		ppm ppm ppm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 3: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature. **Incremental slope is also measured at 25°C.**

Note 4: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately.

Note 5: RMS noise is measured with a 2-pole highpass filter at 10Hz and a 2-pole lowpass filter at 1kHz. The resulting output is full-wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. Correction factors are used to convert from average to RMS, and 0.88 is used to correct for the non-ideal bandbass of the filters.

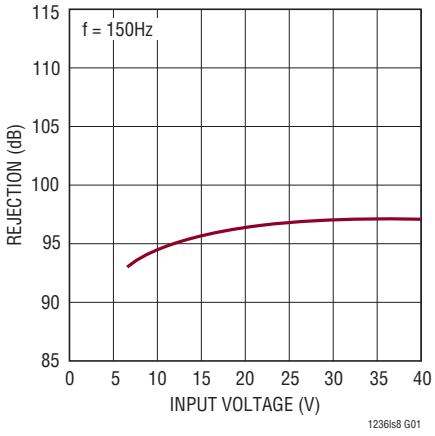
Peak-to-peak noise is measured with a single highpass filter at 0.1Hz and a 2-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

Note 6: Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours, with a continuing trend toward reduced drift with time. Significant improvement in long-term drift can be realized by preconditioning the IC with a 100-200 hour, 125°C burn in. Long term stability will also be affected by differential stresses between the IC and the board material created during board assembly. Temperature cycling and baking of completed boards is often used to reduce these stresses in critical applications.

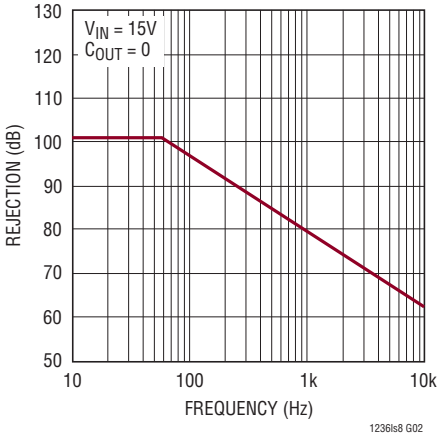
Note 7: Hysteresis in output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to high or low temperature before successive measurements. Hysteresis is roughly proportional to the square of temperature change. Hysteresis is not normally a problem for operational temperature excursions, but can be significant in critical narrow temperature range applications where the instrument might be stored at high or low temperatures. Hysteresis measurements are preconditioned by one temperature cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

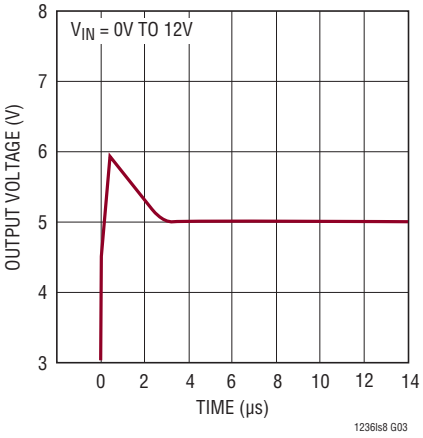
Ripple Rejection



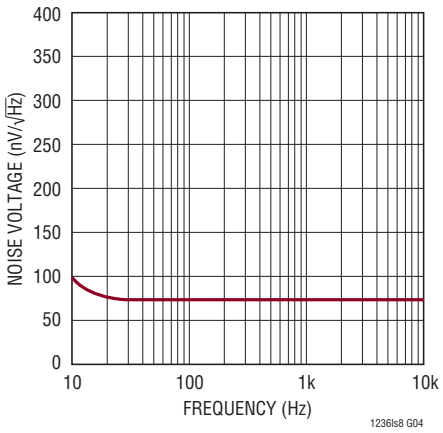
Ripple Rejection



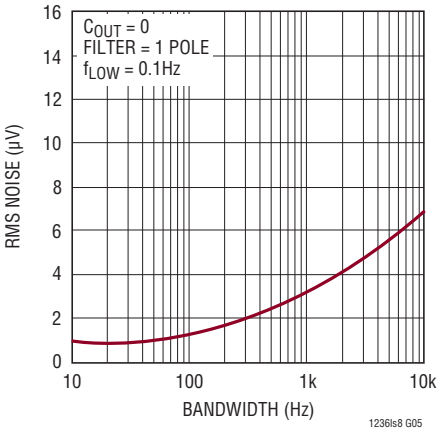
Start-Up



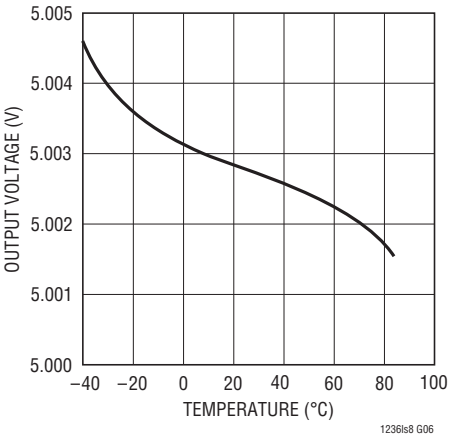
Output Voltage Noise Spectrum



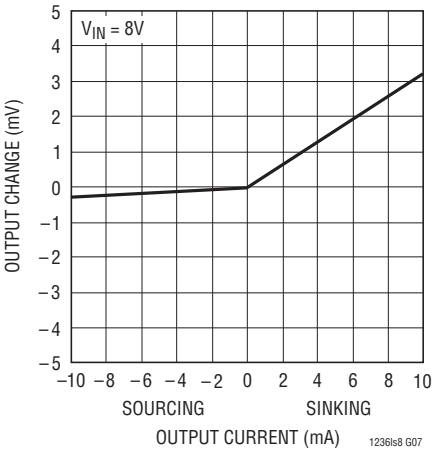
Output Voltage Noise



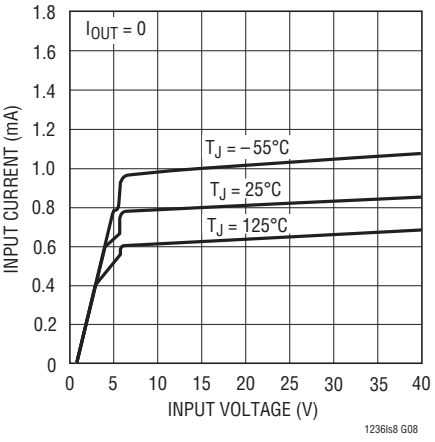
Output Voltage Temperature Drift



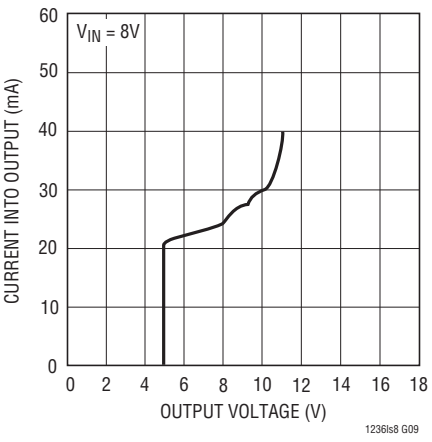
Load Regulation



Quiescent Current

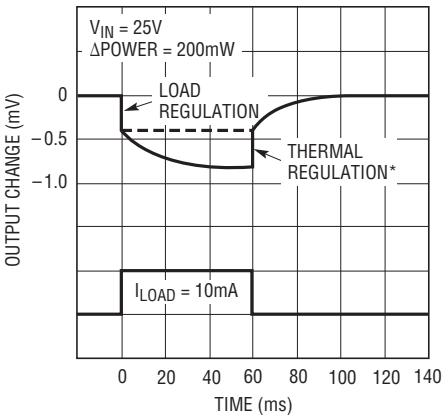


Sink Mode Current Limit



TYPICAL PERFORMANCE CHARACTERISTICS

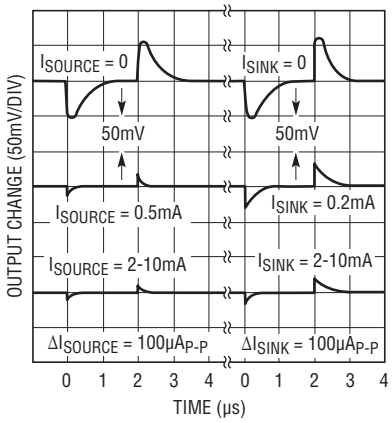
Thermal Regulation



*INDEPENDENT OF TEMPERATURE COEFFICIENT

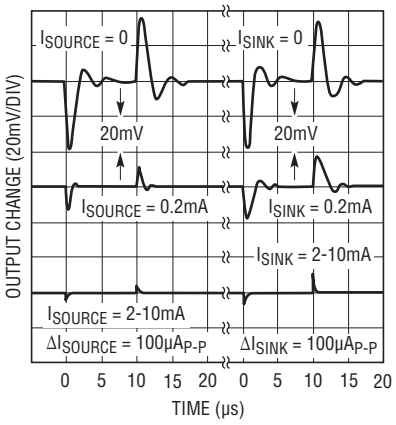
1236ls8 G10

Load Transient Response, C_{LOAD} = 0



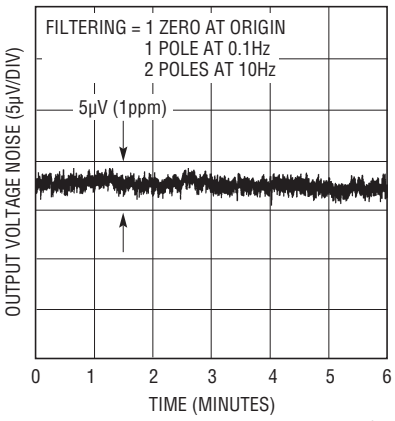
1236ls8 G11

Load Transient Response, C_{LOAD} = 1000pF



1236ls8 G12

Output Noise 0.1Hz to 10Hz



1236ls8 G13

PIN FUNCTIONS

NC (Pins 1, 3, 7, 8): Connected internally, do not connect.

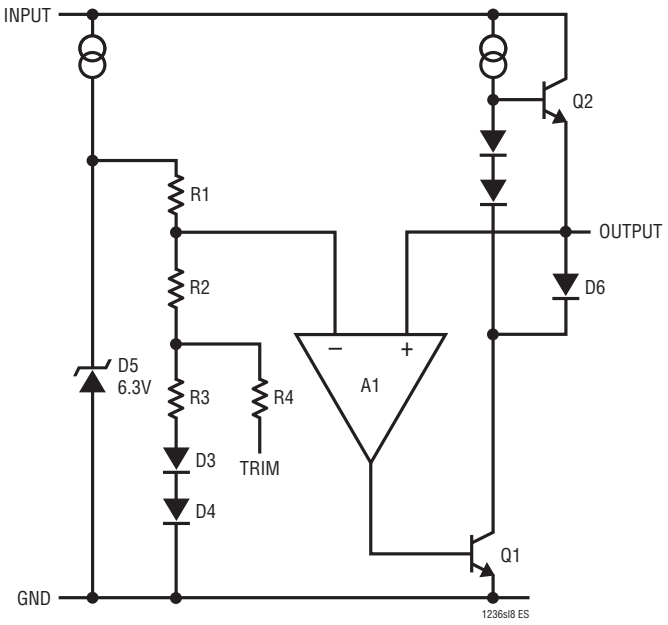
V_{IN} (Pin 2): Power Supply. Bypass with 0.1µF (or larger) capacitor to ground.

GND (Pin 4): Device Ground. See Applications Information section for recommended connection methods.

TRIM (Pin 5): Allows adjustment of output voltage. See Applications Information section for details.

V_{OUT} (Pin 6): Output Voltage. See Applications Information section for details regarding DC and capacitive loading and stability.

BLOCK DIAGRAM

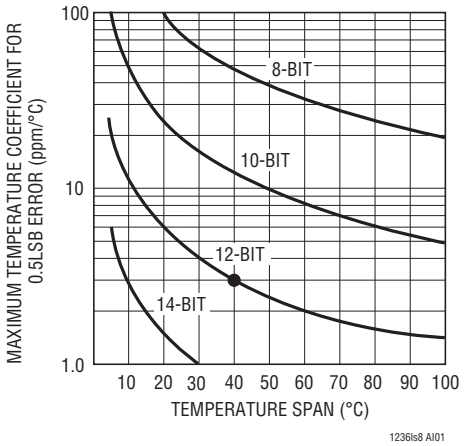


APPLICATIONS INFORMATION

Effect of Reference Drift on System Accuracy

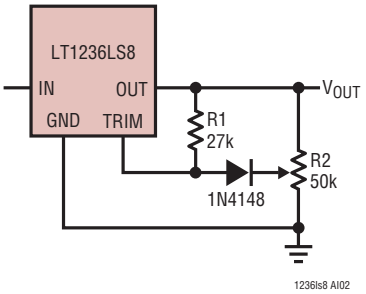
A large portion of the temperature drift error budget in many systems is the system reference voltage. This graph indicates the maximum temperature coefficient allowable if the reference is to contribute no more than 0.5LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 3ppm/°C if it is to contribute less than 0.5LSB error. For this reason, the LT1236LS8 has been optimized for low drift.

Maximum Allowable Reference Drift



Trimming Output Voltage

The LT1236LS8 has an output voltage trim pin, but the temperature drift of the nominal 4V open circuit voltage at pin 5 is about –1.7mV/°C. For the voltage trimming not to affect reference output temperature drift, the external trim voltage must track the voltage on the trim pin. Input impedance of the trim pin is about 100kΩ and attenuation to the output is 13:1. The technique shown below is suggested for trimming the output of the LT1236LS8 while maintaining minimum shift in output temperature coefficient. The R1/R2 ratio is chosen to minimize interaction of trimming and temperature drift shifts, so the exact values shown should be used.



Capacitive Loading and Transient Response

The LT1236LS8 is stable with all capacitive loads, but for optimum settling with load transients, output capacitance should be under 1000pF. The output stage of the reference is class AB with a fairly low idling current. This makes transient response worst-case at light load currents. Because of internal current drain on the output, actual worst-case occurs at I_{LOAD} = 0. Significantly better load transient response is obtained by moving slightly away from these points. See Load Transient Response curves for details. In general, best transient response is obtained when the output is sourcing current. In critical applications, a 10µF solid tantalum capacitor with several ohms in series provides optimum output bypass.

Load Regulation

The LT1236LS8 is capable of driving 10mA to a load. The load regulation at the output of the LT1236LS8 is very good, with a change of less than 25ppm/mA when driving the load. However, the load current will cause a voltage drop in the connecting wire between the LT1236LS8 and the load. This IR drop is dependent on the resistance of the connecting wire and will appear as additional load regulation error. For example, 12 feet of #22 gauge wire or 1 foot of 0.025 inch printed circuit board trace will create 2mV loss at 10mA output current. This is equivalent to 1LSB in a 10V, 12-bit system.

There are three approaches that will reduce this effect. First, limiting the distance between the LT1236LS8 and the load will reduce the trace length, and improve load regulation. Second, use wider traces for the connections between the LT1236LS8 and the load to reduce IR drop. Finally,

APPLICATIONS INFORMATION

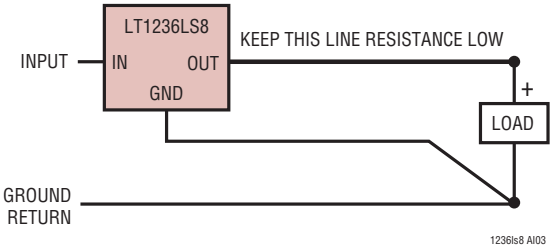
use a star-ground method, with the LT1236LS8 ground tied directly to the load, rather than through a ground plane or other shared ground trace. This last method will reduce drop in the ground trace between the LT1236LS8 and the load. The ground wire in this case will carry only approximately 1mA, which is the ground current of the LT1236LS8, while the load return current will shunt to the system ground separate from the reference-to-load path.

The following circuits show proper hook-up to minimize errors due to ground loops and line losses. Losses in the output lead can be greatly reduced by adding a PNP boost transistor if load currents are 5mA or higher. R2 can be added to further reduce current in the output sense lead.

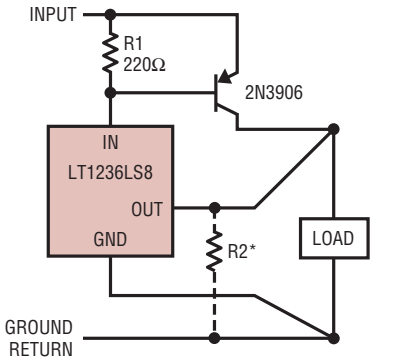
Effects of Air Movement on Low Frequency Noise

The LT1236LS8 has very low noise because of the buried zener used in its design. In the 0.1Hz to 10Hz band, peak-to-peak noise is about 0.5ppm of the DC output. To achieve this low noise, however, care must be taken to shield the reference from ambient air turbulence. Air movement can create noise because of thermoelectric differences between IC package leads and printed circuit board materials and/or sockets. Power dissipation in the reference, even though it rarely exceeds 20mW, is enough to cause small temperature gradients in the package leads. Variations in thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference.

Standard Series Mode



Series Mode with Boost Transistor



*OPTIONAL—REDUCES CURRENT IN OUTPUT SENSE LEAD: R2 = 2.4k

Long-Term Drift

Long-term drift cannot be extrapolated from accelerated high temperature testing. This erroneous technique gives drift numbers that are wildly optimistic. The only way long-term drift can be determined is to measure it over the time interval of interest.

The LT1236LS8 long-term drift data was collected on 80 parts that were soldered into printed circuit boards similar to a *real world* application. The boards were then placed into a constant temperature oven with a T_A = 35°C, their outputs were scanned regularly and measured with an 8.5 digit DVM. Typical long-term drift is illustrated in Figure 1.

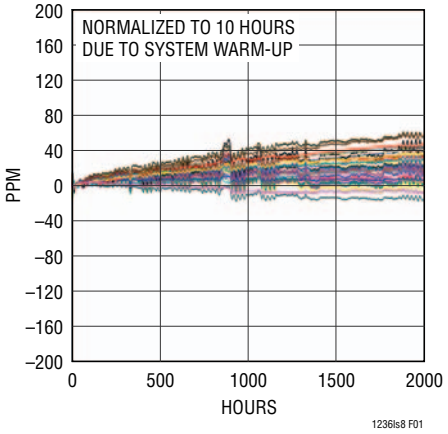


Figure 1. Long-Term Drift

APPLICATIONS INFORMATION

Hysteresis

Thermal hysteresis is a measure of change of output voltage as a result of temperature cycling. Figure 2a and 2b illustrate the typical hysteresis based on data taken from the LT1236LS8. A proprietary design technique minimizes thermal hysteresis.

IR Reflow Shift

The mechanical stress of soldering a part to a board can cause the output voltage to shift. Moreover, the heat of an IR reflow or convection soldering oven can also cause the output voltage to shift. The materials that make up a semiconductor device and its package have different rates of expansion and contraction. After a part undergoes the extreme heat of a lead-free IR reflow profile, like the one shown in Figure 3, the output voltage shifts. After the device expands, due to the heat, and then contracts, the stresses on the die have changed position. This shift is similar, but more extreme than thermal hysteresis.

Experimental results of IR reflow shift are shown below in Figure 4. These results show only shift due to reflow and not mechanical stress.

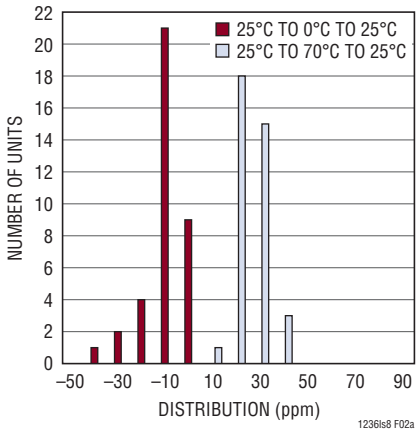


Figure 2a. Hysteresis Plot 0°C to 70°C

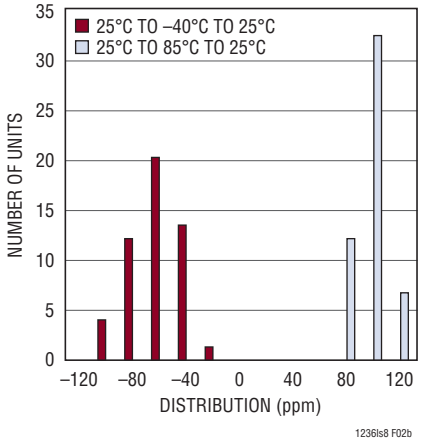


Figure 2b. Hysteresis Plot –40°C to 85°C

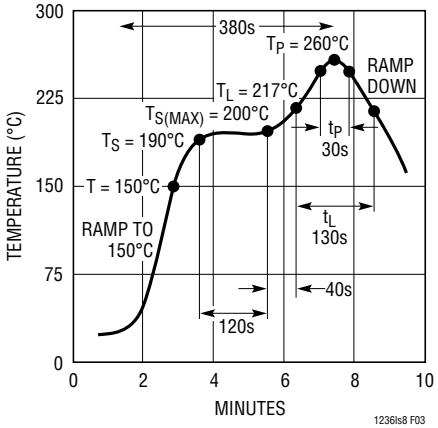


Figure 3. Lead-Free Reflow Profile

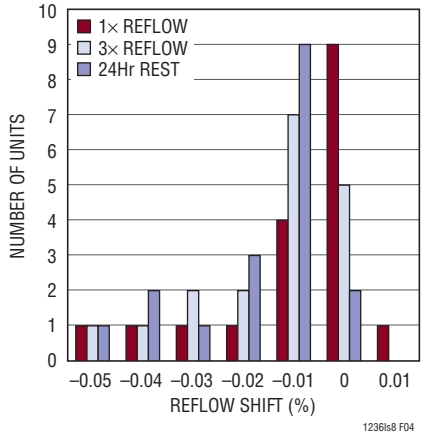


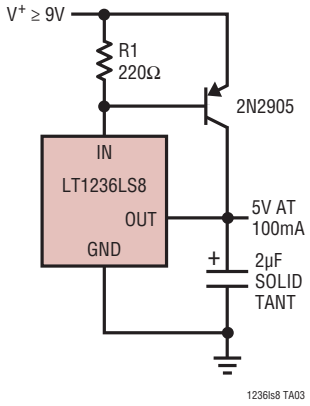
Figure 4. Output Voltage Shift Due to IR Reflow

Humidity Sensitivity

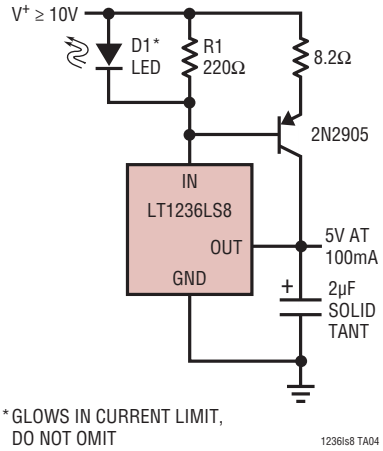
Plastic mold compounds absorb moisture. With changes in relative humidity, plastic packaging materials change the amount of pressure they apply to the die inside, which can cause slight changes in the output of a voltage reference, usually on the order of 100ppm. The LS8 package is hermetic, so it is not affected by humidity, and is therefore more stable in environments where humidity may be a concern. However, PC Board material may absorb moisture and apply mechanical stress to the LT1236LS8. Proper board materials and layout are essential.

TYPICAL APPLICATIONS

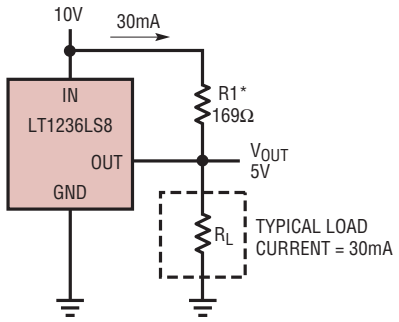
Boosted Output Current with No Current Limit



Boosted Output Current with Current Limit



Handling Higher Load Currents

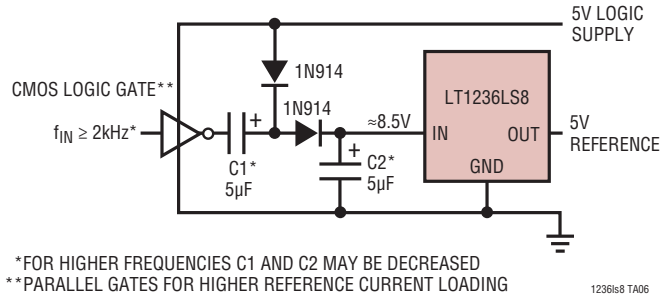


*SELECT R1 TO DELIVER TYPICAL LOAD CURRENT. LT1236 WILL THEN SOURCE OR SINK AS NECESSARY TO MAINTAIN PROPER OUTPUT. DO NOT REMOVE LOAD AS OUTPUT WILL BE DRIVEN UNREGULATED HIGH. LINE REGULATION IS DEGRADED IN THIS APPLICATION

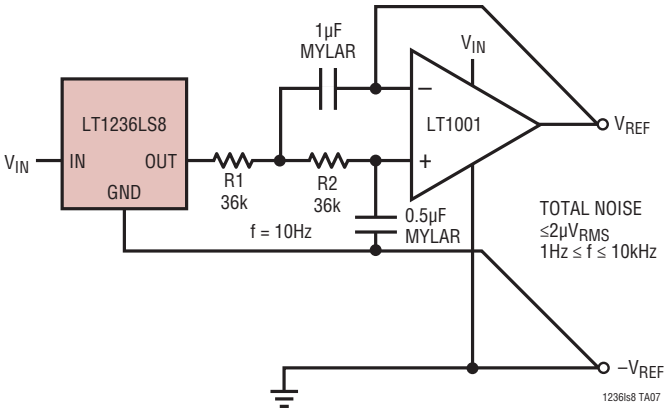
1236ls8 TA05

TYPICAL APPLICATIONS

Operating 5V Reference from 5V Supply

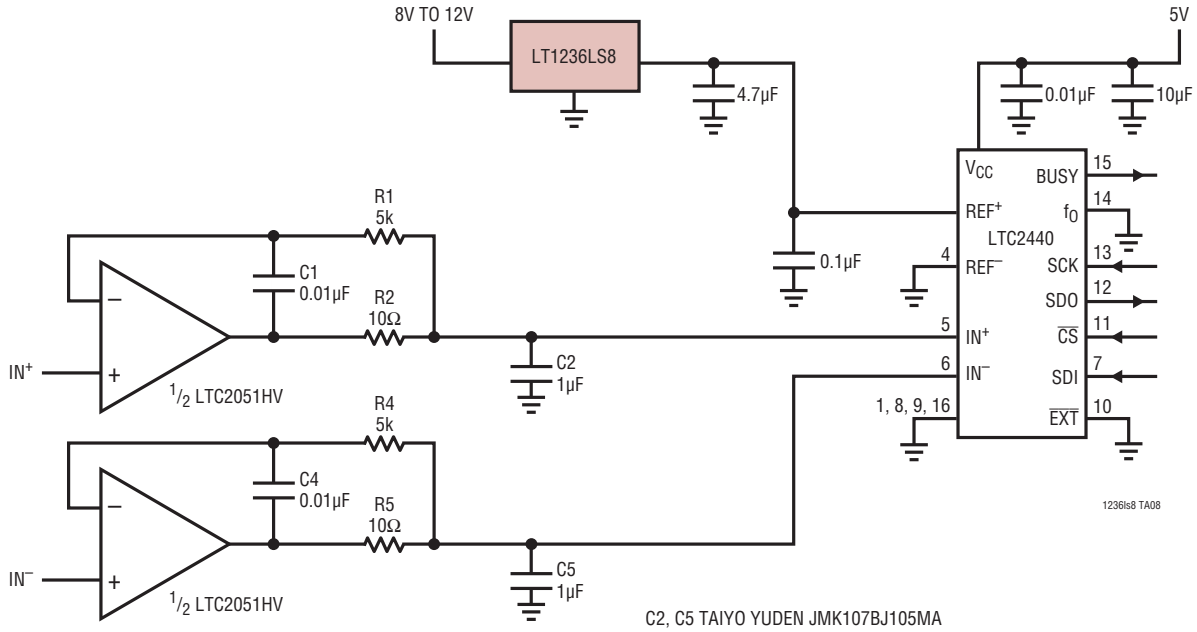


2-Pole Lowpass Filtered Reference



TYPICAL APPLICATIONS

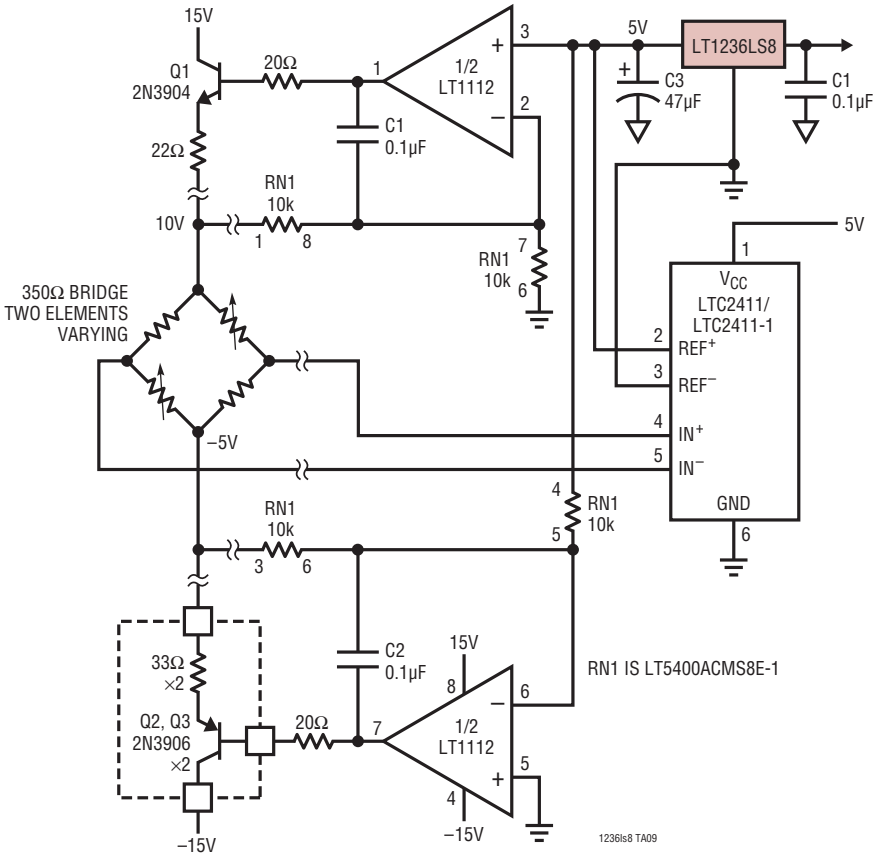
High Precision, High Stability, Differential Measurement System



C2, C5 TAIYO YUDEN JMK107BJ105MA

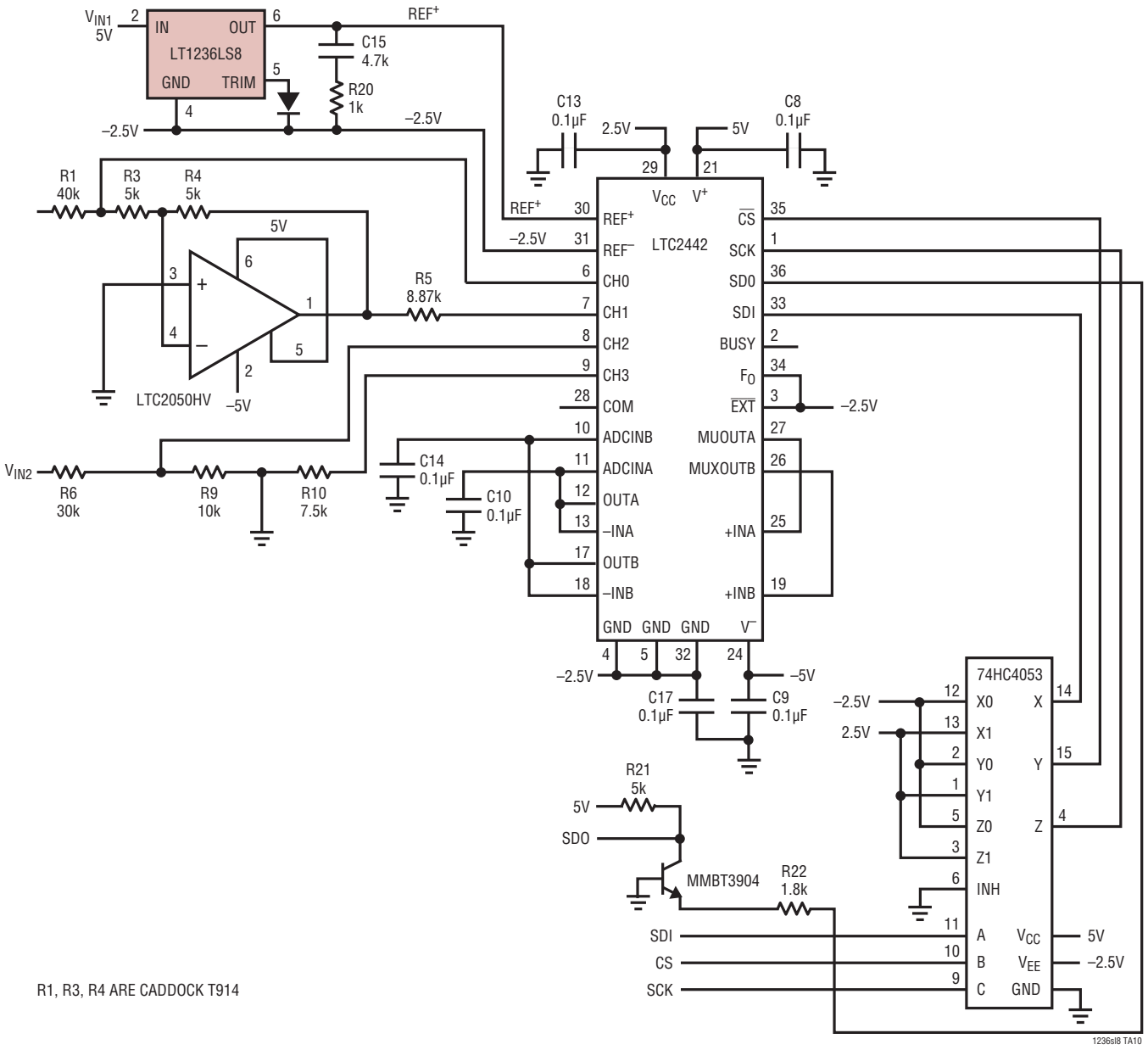
TYPICAL APPLICATIONS

Use Resistor Arrays to Provide Precise Matching in Excitation Amplifier



TYPICAL APPLICATIONS

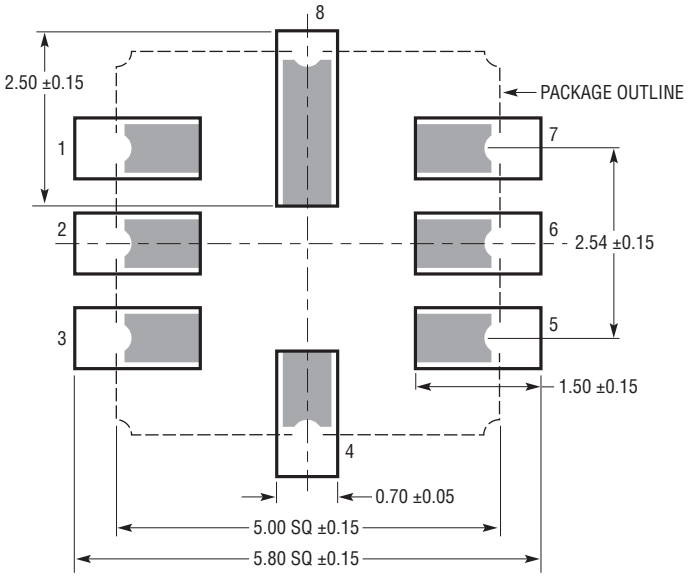
±10V Range Precision Measurement System



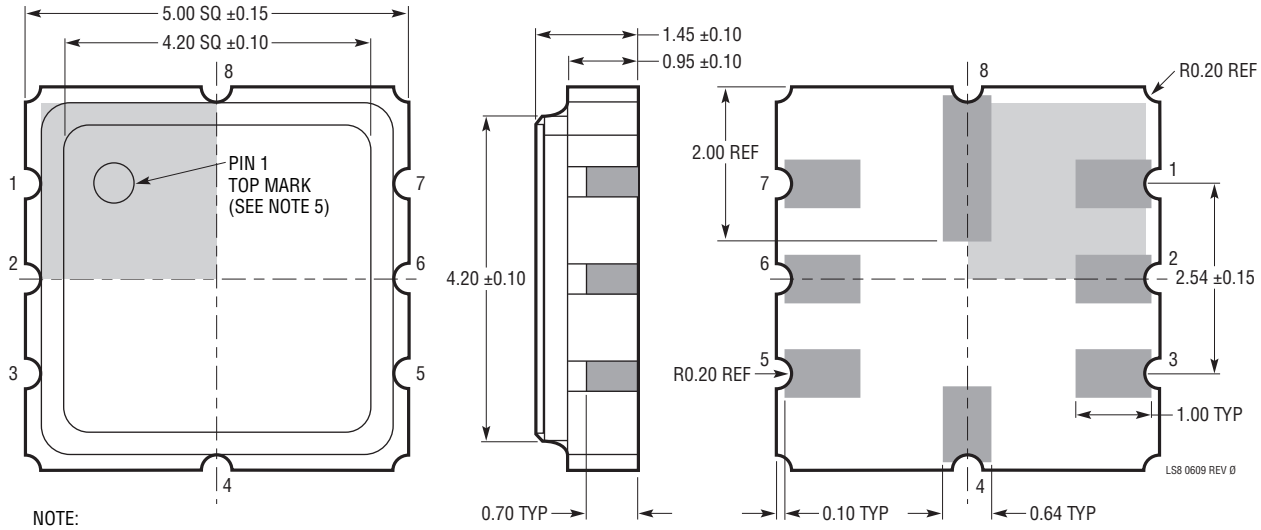
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

LS8 Package
8-Pin Leadless Chip Carrier (5mm × 5mm)
(Reference LTC DWG # 05-08-1852 Rev Ø)



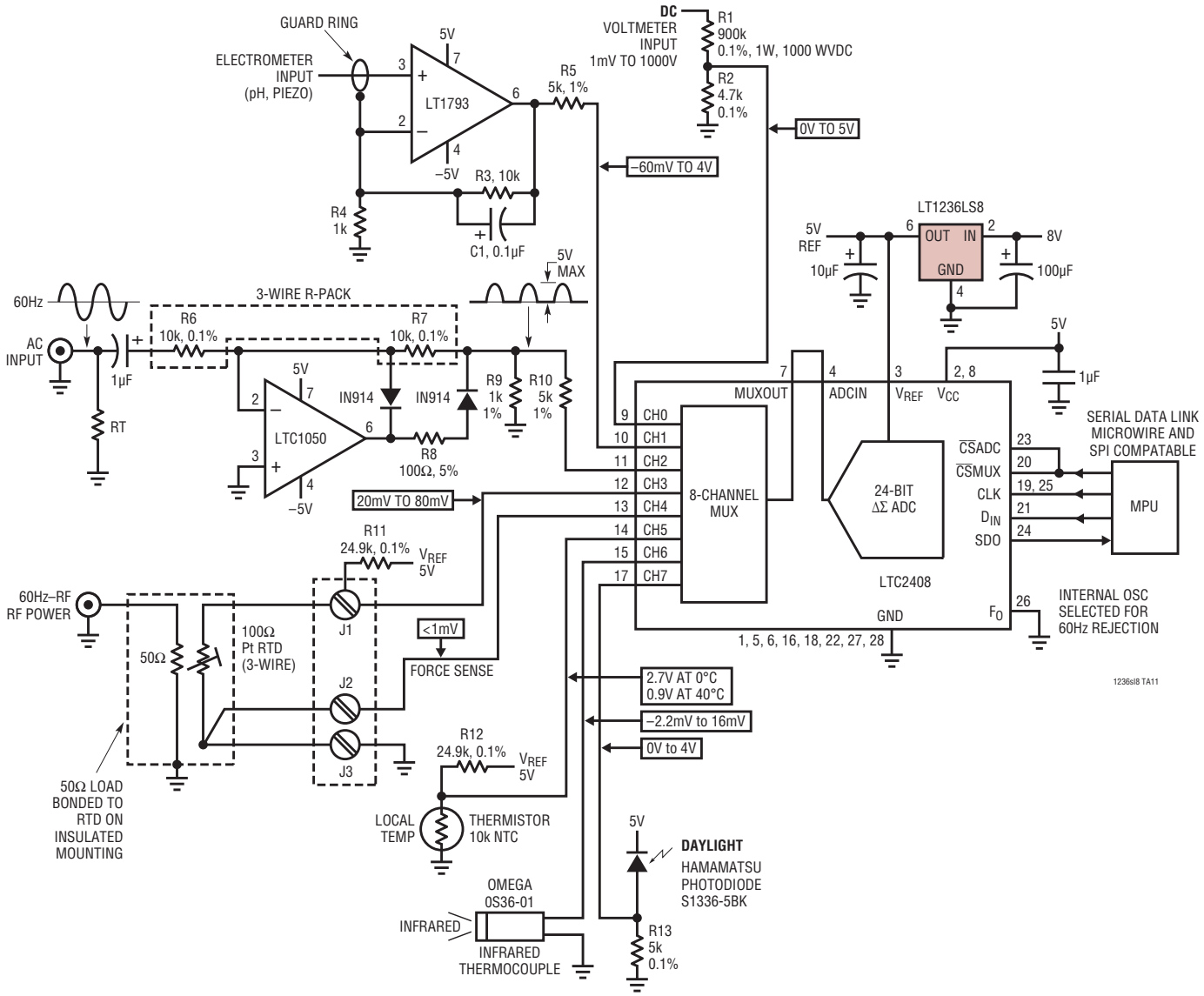
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS PACKAGE DO NOT INCLUDE PLATING BURRS
   PLATING BURRS, IF PRESENT, SHALL NOT EXCEED 0.30mm ON ANY SIDE
4. PLATING—ELECTO NICKEL MIN 1.25UM, ELECTRO GOLD MIN 0.30UM
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Measure DC to Daylight Using the LTC2408 and LT1236LS8



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1021	Precision References for Series or Shunt Operation in Hermetic TO-5, SOP-8, DIP-8 Package	0.05% Max Initial Error, 5ppm/°C Max Drift, 1ppm Peak-to-Peak Noise (0.1Hz to 10Hz), –55°C to 125°C (TO-5)
LT1236S8/ LT1236N8	Low Drift, Low Noise, 5V and 10V Voltage Reference in SO8, and DIP8 Package	0.05% Max Initial Error, 5ppm/°C Max Drift, 1ppm Peak-to-Peak Noise (0.1Hz to 10Hz), –40°C to 85°C
LTC6652LS8	High Precision, Buffered Voltage Reference Family in 5mm × 5mm Hermetic QFN Package	0.05% Max Initial Error, 5ppm/°C Max Drift, Shutdown Current <2µA, –40°C to 125°C Operation
LT6654LS8	Precision, Low Noise, High Output Drive Voltage Reference Family in 5mm × 5mm Hermetic QFN Package	1.6ppm Peak-to-Peak Noise (0.1Hz to 10Hz, Sink/Source ±10mA, 5ppm/°C Max Drift, –40°C to 125°C Operation

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