



# 8-Bit, 200 MSPS ADC

## AD9054A

### 1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at [www.analog.com/AD9054](http://www.analog.com/AD9054)

### 2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD9054-703J44	8-Bit, 200 MSPS ADC

#### 2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
J44	J	44-Lead ceramic JLCC

### 3.0 Terminal Connections:

Pin Number	Mnemonic	Pin Number	Mnemonic
1	AIN	23	GND
2	GND	24	VDD
3	VDD	25	DB <sub>0</sub>
4	$\overline{\text{DEMUX}}$	26	DB <sub>1</sub>
5	$\overline{\text{DS}}$	27	DB <sub>2</sub>
6	DS	28	DB <sub>3</sub>
7	ENCODE	29	DB <sub>4</sub>
8	$\overline{\text{ENCODE}}$	30	DB <sub>5</sub>
9	VDD	31	DB <sub>6</sub>
10	GND	32	DB <sub>7</sub>
11	VDD	33	GND
12	GND	34	VDD
13	DA <sub>7</sub>	35	GND
14	DA <sub>6</sub>	36	VDD
15	DA <sub>5</sub>	37	VDD
16	DA <sub>4</sub>	38	GND
17	DA <sub>3</sub>	39	VREF OUT
18	DA <sub>2</sub>	40	VREF IN
19	DA <sub>1</sub>	41	GND
20	DA <sub>0</sub>	42	VDD
21	VDD	43	GND
22	GND	44	$\overline{\text{AIN}}$

Figure 1 - Terminal connections.

ASD0015375

Rev. D

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective companies.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.

Tel: 781.329.4700

[www.analog.com](http://www.analog.com)

Fax: 781.326.8703 © 2008 Analog Devices, Inc. All rights reserved.

# AD9054A

## 4.0 Absolute Maximum Ratings. ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

$V_{DD}$ .....	6V
Analog Inputs.....	$V_{DD}$ to 0.0V
Digital Inputs.....	$V_{DD}$ to 0.0V
VREF IN, VREF OUT.....	$V_{DD}$ to 0.0V
Digital Output Current.....	20mA
Operating Temperature.....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Storage Temperature.....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Maximum Junction Temperature.....	$+150^\circ\text{C}$
Maximum Case Temperature .....	$+150^\circ\text{C}$

### NOTES

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

## 4.1 Thermal Characteristics:

Thermal Resistance, 44-lead JLCC Package

Junction-to-Case ( $\Theta_{JC}$ ) =  $10^\circ\text{C/W}$  Max

Junction-to-Ambient ( $\Theta_{JA}$ ) =  $49^\circ\text{C/W}$  Max

## 4.2 Electrical Table:

**Table I**

Parameter See notes at end of table	Symbol	Conditions 1/	Sub-group	Limit Min	Limit Max	Units
<b>DC Accuracy</b>						
Differential Nonlinearity	DNL		1 2,3	-1 -1	+1.5 +2.0	LSB
Integral Nonlinearity	INL		1 2,3		$\pm 1.5$ $\pm 2.0$	LSB
No Missing Codes		Guaranteed				
Gain Error	$A_e$	<u>2/</u> <u>8/</u>	1 2,3		$\pm 7.0$ $\pm 9.0$	%FS
<b>Analog Input</b>						
Input Offset Voltage	$V_{OS}$		1 2,3		$\pm 16$ $\pm 23$	mV
Input Resistance	$R_{in}$	<u>8/</u>	1 2,3	36 23		k $\Omega$
Input Bias Current	$I_b$		1 2,3		50 75	$\mu\text{A}$
<b>Reference Output</b>						
Output Voltage	$V_{REF}$	<u>8/</u>	1,2,3	2.4	2.6	V

Table I (Continued)

Parameter See notes at end of table	Symbol	Conditions <u>1/</u>	Sub-group	Limit Min	Limit Max	Units
<b>Switching Performance</b>						
Maximum Conversion Rate	$F_s$		1,2,3	200		MSPS
Output Valid Time	$t_v$	<u>3/</u> , <u>9/</u>	7	2.7		ns
Output Propagation Delay	$t_{PD}$	<u>3/</u> , <u>9/</u>	7		7.9	ns
<b>Digital Inputs</b>						
HIGH Level Current	$I_{IH}$	<u>4/</u> , <u>8/</u>	1,2,3		625	$\mu A$
LOW Level Current	$I_{IL}$	<u>4/</u> , <u>8/</u>	1,2,3		625	$\mu A$
<b>Digital Outputs</b>						
HIGH Output Voltage	$V_{OH}$	<u>9/</u>	1,2,3	2.4		V
LOW Output Voltage	$V_{OL}$	<u>9/</u>	1,2,3		0.4	V
<b>Power Supply</b>						
$V_{DD}$ Supply Current	$I_{DD}$	<u>8/</u>	1,2,3		156	mA
Power Dissipation	$P_D$	<u>5/</u>	1		781	mW
Power Dissipation Sensitivity	$P_{SS}$	<u>6/</u>	1		15	mV/V
<b>Dynamic Performance</b>						
Signal-to-Noise Ratio (Without Harmonics)	SNR	$f_{IN} = 49.7 \text{ MHz}$ $f_{IN} = 70.1 \text{ MHz}$	9 9	42 42		dB
Signal-to-Noise Ratio (With Harmonics)	SINAD	$f_{IN} = 49.7 \text{ MHz}$ $f_{IN} = 70.1 \text{ MHz}$	9 9	40 39		dB
Effective Number of Bits	ENOB	$f_{IN} = 49.7 \text{ MHz}$ $f_{IN} = 70.1 \text{ MHz}$	9 9	6.35 6.18		Bits
2 <sup>nd</sup> Harmonic Distortion	2HD	$f_{IN} = 49.7 \text{ MHz}$ $f_{IN} = 70.1 \text{ MHz}$	9 9	54 49		dBc
3 <sup>rd</sup> Harmonic Distortion	3HD	$f_{IN} = 49.7 \text{ MHz}$ $f_{IN} = 70.1 \text{ MHz}$	9 9	48 43		dBc

**TABLE I NOTES:**

- 1/  $V_{DD} = 5 \text{ V}$ , external reference,  $f_s = \text{max}$  unless otherwise noted.
- 2/ Gain error and gain temperature coefficient are based on the ADC only (with a fixed 2.5 V external reference)
- 3/  $t_v$  and  $t_{PD}$  are measured from the threshold crossing of the ENCODE input to valid TTL levels of the digital outputs. The output ac load during test is 5 pF.
- 4/  $I_{IH}$  and  $I_{IL}$  are valid for differential input voltages of less than 1.5V. At higher differential voltages, the input current will increase to a maximum of 1.5 mA at 25°C and 2.0 mA @ -55°C and 125°C
- 5/ Power dissipation is measured under the following conditions: analog input is -1 dBFS at 19.7 MHz.
- 6/ A change in input offset voltage with respect to a change in  $V_{DD}$ .
- 7/ SNR/harmonics based on an analog input voltage of -1.0 dBFS referenced to a 1.024 V full-scale input range.
- 8/ 100% production tested at 25°C; guaranteed by design and characterization testing for full mil temperature range.
- 9/ Go/No-Go parameter only, no read and record data available.

# AD9054A

## 4.3 Electrical Test Requirements:

Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 7, 9 <u>1/</u> <u>2/</u> <u>3/</u>
Group A Test Requirements	1, 2, 3, 7, 9 <u>3/</u>
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1

- 1/ PDA applies to subgroup 1 only. Delta's excluded from PDA.
- 2/ See Table III for delta parameters. See Table I for test conditions.
- 3/ Table I parameters with Note 8/ are 100% production tested at 25°C; guaranteed by design and characterization testing for full mil temperature range.

## 4.4 Table III - Life Test Endpoint and Delta Parameter (Product is tested in accordance with Table I with the following exceptions)

Parameter	Symbol	Sub-groups	Post Burn in Limit	Burn In Delta	Post Life Test Limit	Life Test Delta	Units
			Max		Max		
V <sub>DD</sub> Supply Current	I <sub>DD</sub>	1	156	-	171.6	±15.6	mA
Input Offset Voltage	V <sub>OS</sub>	1	±23	±7	±30	±7	mV
Gain Error	A <sub>e</sub>	1	±9	±2	±13	±4	%FS

## 5.0 MIL-STD-38535 QMLV exceptions:

- 5.1 Full WLA per MIL-STD-883 TM 5007 is not available for this product fabricated in a QMLQ wafer process facility. SEM Inspection only is available per MIL-STD-883, TM2018.

Rev	Description of Change	Date
A	Initiate	10/18/2004
B	Typical values for Dynamic Performance for subgroup 10 & 11 deleted	06/15/2005
C	Clarify SEM vs. WLA availability for QMLQ fab process	11/12/2007
D	Update header/footer and add to 1.0 Scope description.	March 17, 2008

