100V Half Bridge Driver with Floating Grounds and Adjustable Dead-Time

FEATURES

- **Unique Symmetric Floating Gate Driver Architecture**
- **High Noise Immunity,Tolerates ±10V Ground Difference**
- **100V Maximum Input Voltage Independent of IC Supply Voltage V_{CC}**
- **5V to 14V V_{CC} Operating Voltage**
- **4V to 14V Gate Driver Voltage**
- **0.8Ω Pull-Down, 1.5Ω Pull-Up for Fast Turn-On/Off**
- **Adaptive Shoot-Through Protection**
- **Adjustable Dead-Time**
- **TTL/CMOS Compatible Input**
- **V_{CC} UVLO/OVLO and Floating Supplies UVLO**
- Drives Dual N-Channel MOSFETs
- Open-Drain Fault Indicator (VCC UVLO/OVLO, Gate Driver UVLO and Thermal Shutdown)
- Available in Thermally Enhanced 12-LEAD MSOP
- AEC-Q100 Automotive Qualification in Progress

APPLICATIONS

- Automotive and Industrial Power Systems
- Telecommunication Power Systems
- Half-Bridge and Full-Bridge Converters

DESCRIPTION

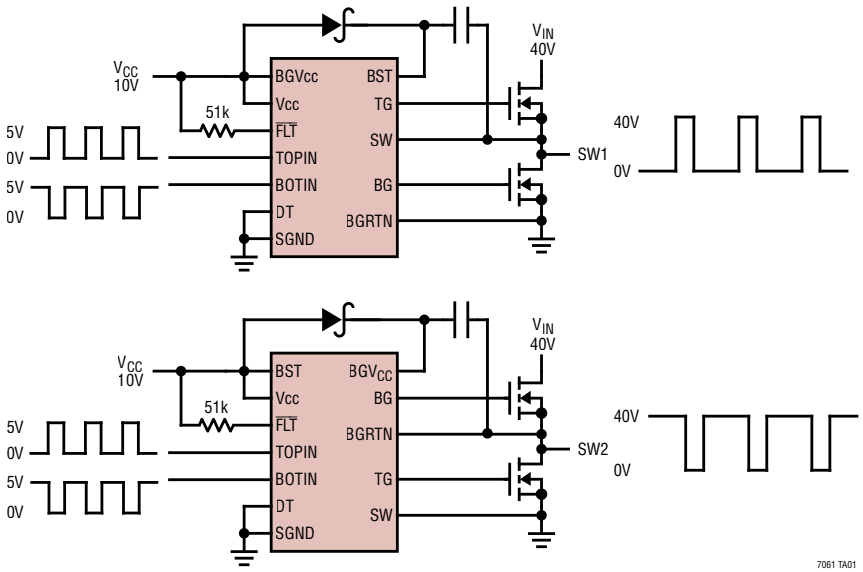
The LTC®7061 drives two N-Channel MOSFETs in a half-bridge configuration with supply voltages up to 100V. Both high-side and low-side drivers can drive the MOSFETs with a different ground reference, providing excellent noise and transient immunity.

Its powerful 0.8Ω pull-down and 1.5Ω pull-up MOSFET drivers allows the use of large gate capacitance high voltage MOSFETs. Additional features include UVLO, TTL/CMOS compatible inputs, adjustable turn-on/-off delays and shoot-through protection.

For a similar driver in this product family, please refer to chart below.

PARAMETER	LTC7060	LTC7061	LTC7062	LTC7063
Input Signal	Three-State PWM	CMOS/ TTL Logic	CMOS/ TTL Logic	Three-State PWM
Shoot-Through Protection	Yes	Yes	No	Yes
Absolute Max Voltage	115V	115V	115V	155V
V_{CC} Falling UVLO	5.3V	4.3V	4.3V	5.3V

TYPICAL APPLICATION



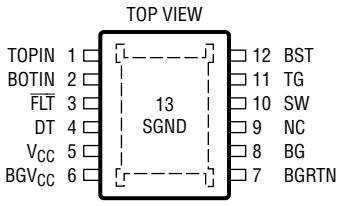
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Supply Voltage .....–0.3V to 15V
Top Side Driver Voltage (BST) .....–0.3V to 115V
Bottom Side Driver Voltage (BGV_{CC}).....–0.3V to 115V
SW, BGRTN .....–10V to 100V
(BST-SW).....–0.3V to 15V
(BGV_{CC} -BGRTN).....–0.3V to 15V
$\overline{FLT}$ ..... –0.3V to 15V
DT, BOTIN, TOPIN ..... –0.3V to 6V
Driver Output TG (With Respect to SW) .....–0.3V to 15V
Driver Output BG (With Respect to BGRTN)... –0.3V to 15V
Operating Junction Temperature Range
(Note 2, 3)..... .....–40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

Note: All voltages are referred to SGND unless otherwise noted.

PIN CONFIGURATION



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 13) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7061EMSE#PBF	LTC7061EMSE#TRPBF	LTC7061	12-Lead Plastic MSOP	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC7061IMSE#WPBF	LTC7061IMSE#WTRPBF	LTC7061	12-Lead Plastic MSOP	–40°C to 125°C
LTC7061JMSE#WPBF	LTC7061JMSE#WTRPBF	LTC7061	12-Lead Plastic MSOP	–40°C to 150°C
LTC7061HMSE#WPBF	LTC7061HMSE#WTRPBF	LTC7061	12-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{BGVCC} = V_{BST} =10V, V_{BGRTN} = V_{SW} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply and V_{CC} Supply							
V_{IN}	Input Supply Operating Range					100	V
V_{CC}	IC Supply Operating Range			5		14	V
I_{VCC}	V_{CC} Supply Current	V_{TOPIN} = V_{BOTIN} = 0V, R_{DT} = 100kΩ			0.3		mA
V_{UVLO_VCC}	V_{CC} Undervoltage Lockout Threshold	V_{CC} Falling			4.3		V
		Hysteresis			0.2		V
V_{OVLO_VCC}	V_{CC} OVLO Threshold	V_{CC} Rising			14.6		V
		Hysteresis			0.8		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{BGVCC} = V_{BST} =10V, V_{BGRTN} = V_{SW} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TG Gate Driver Supply (BST-SW)							
V_{BST-SW}	TG Driver Supply Voltage Range (With Respect to SW)			4		14	V
I_{BST}	Total BST Current (Note 4)	TG = Low			8.9		µA
		TG = High			146		µA
V_{UVLO_BST}	Undervoltage Lockout Threshold	BST Falling, With Respect to SW			3.4		V
		Hysteresis			0.3		V
BG Gate Driver Supply (BGV_{CC}-BGRTN)							
$V_{BGVCC-BGRTN}$	BG Driver Supply Voltage Range (With Respect to BGRTN)			4		14	V
I_{BGVCC}	Total BGV_{CC} Current (Note 4)	BG = Low			8.9		µA
		BG = High			146		µA
V_{UVLO_BGVCC}	Undervoltage Lockout Threshold	BGV_{CC} Falling, With Respect to BGRTN			3.4		V
		Hysteresis			0.3		V
Input Signal (TOPIN, BOTIN)							
$V_{IH(TOPIN)}$	TG Turn-On Input Threshold	TOPIN Rising				1.75	V
$V_{IL(TOPIN)}$	TG Turn-Off Input Threshold	TOPIN Falling		0.5			V
$V_{IH(BOTIN)}$	BG Turn-On Input Threshold	BOTIN Rising				1.75	V
$V_{IL(BOTIN)}$	BG Turn-Off Input Threshold	BOTIN Falling		0.5			V
R_{DOWN_TOPIN}	TOPIN Internal Pull-Down Resistor				1000		kΩ
R_{DOWN_BOTIN}	BOTIN Internal Pull-Down Resistor				1000		kΩ
Dead-Time and FAULT (DT, $\overline{FLT}$)							
$t_{PLH(BG)}$ / $t_{PLH(TG)}$	BG/TG Low to TG/BG High Propagation Delay (Dead-Time)	R_{DT} = 0Ω			31		ns
		R_{DT} = 24.9kΩ			43		ns
		R_{DT} = 64.9kΩ			62		ns
		R_{DT} = 100kΩ			76		ns
		R_{DT} = Open			250		ns
R_{FLTb}	$\overline{FLT}$ Pin Pull-down Resistor				60		Ω
t_{FLTb}	$\overline{FLT}$ Pin Delay	Low to High			100		µs
Gate Driver Output (TG)							
$V_{OH(TG)}$	TG High Output Voltage	I_{TG} = –100mA, $V_{OH(TG)}$ = V_{BST} – V_{TG}			150		mV
$V_{OL(TG)}$	TG Low Output Voltage	I_{TG} = 100mA, $V_{OL(TG)}$ = V_{TG} – V_{SW}			80		mV
R_{TG_UP}	TG Pull-Up Resistance	V_{BST-SW} = 10V			1.5		Ω
R_{TG_DOWN}	TG Pull-Down Resistance	V_{BST-SW} = 10V			0.8		Ω
Gate Driver Output (BG)							
$V_{OH(BG)}$	BG High Output Voltage	I_{BG} = –100mA, $V_{OH(BG)}$ = V_{BGVCC} – V_{BG}			150		mV
$V_{OL(BG)}$	BG Low Output Voltage	I_{BG} = 100mA, $V_{OL(BG)}$ = V_{BG} – V_{BGRTN}			80		mV
R_{BG_UP}	BG Pull-Up Resistance	$V_{BGVCC–BGRTN}$ =10V			1.5		Ω
R_{BG_DOWN}	BG Pull-Down Resistance	$V_{BGVCC–BGRTN}$ =10V			0.8		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{BGVCC} = V_{BST} =10V, V_{BGRTN} = V_{SW} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Time							
$t_{PDLH(TG)}$	TOPIN High to TG High Propagation Delay				20		ns
$t_{PDHL(TG)}$	TOPIN Low to TG Low Propagation Delay				20		ns
$t_{PDLH(BG)}$	BOTIN High to BG High Propagation Delay				21		ns
$t_{PDHL(BG)}$	BOTIN Low to BG Low Propagation Delay				21		ns
$t_{r(BG)}$	BG Output Rise Time	10% to 90%, C_{LOAD} = 3nF			18		ns
$t_{f(BG)}$	BG Output Fall Time	10% to 90%, C_{LOAD} = 3nF			14		ns
$t_{r(TG)}$	TG Output Rise Time	10% to 90%, C_{LOAD} = 3nF			18		ns
$t_{f(TG)}$	TG Output Fall Time	10% to 90%, C_{LOAD} = 3nF			14		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

Note 2: The LTC7061E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7061I is guaranteed over the –40°C to 125°C operation junction temperature range. The LTC7061J is guaranteed over the –40°C to 150°C operating junction temperature range. The LTC7061H is guaranteed over the –40°C to 150°C operation junction temperature range. High junction temperature degrades operation lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environment factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula

$T_J = T_A + (P_D \bullet 51\ °C/W)$ for LFCSP package; $T_J = T_A + (P_D \bullet 40\ °C/W)$ for MSOP package.

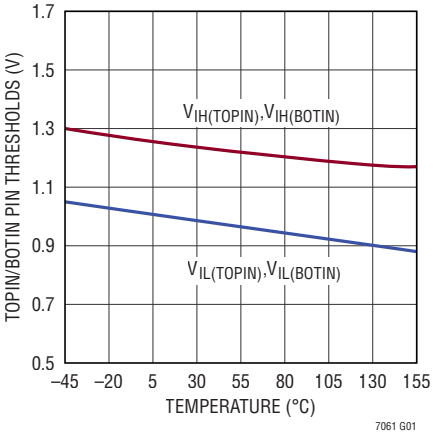
Note 4: The total current includes both the current from BGV_{CC}/BST to BGRTN/SW and the current to SGND. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: Rise and fall times are measured using 10% and 90% levels.

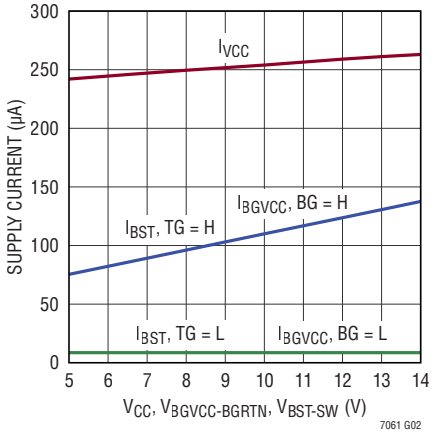
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

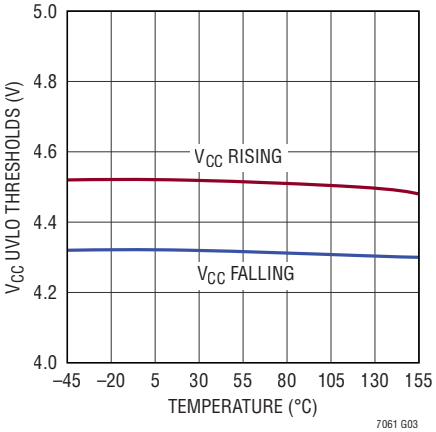
TOPIN/BOTIN Pin Thresholds Temperature



Quiescent Supply Current vs Supply Voltage

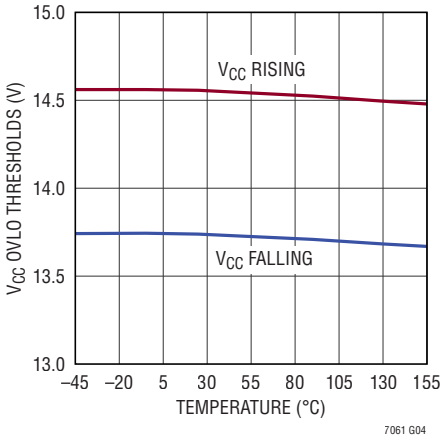


V_{CC} Undervoltage Lockout Thresholds vs Temperature

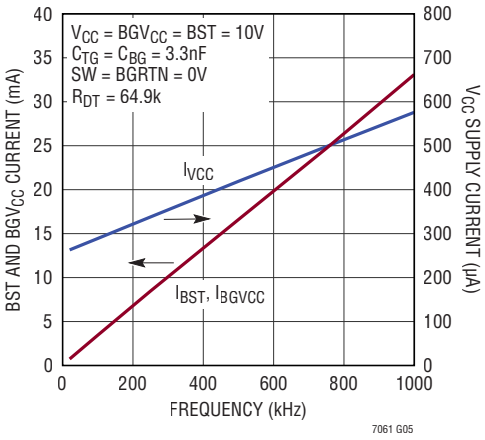


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

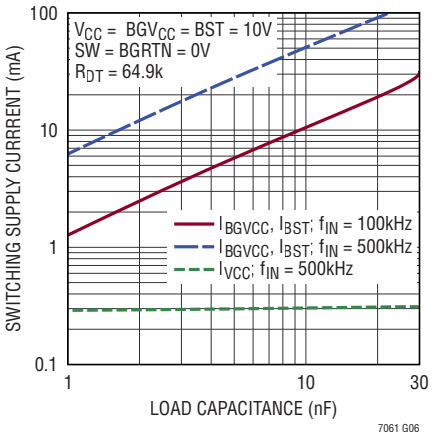
V_{CC} Overvoltage Lockout Thresholds vs Temperature



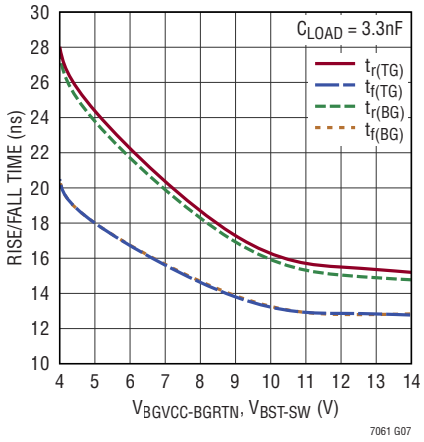
Supply Current vs Input Frequency



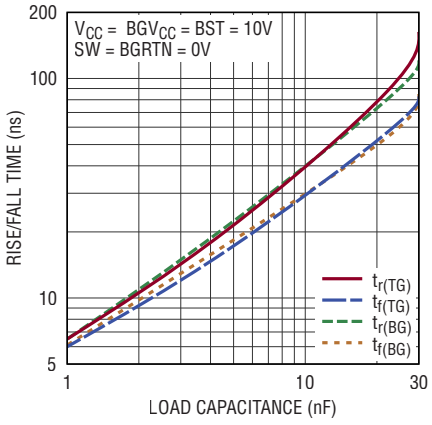
Switching Supply Current vs Load Capacitance



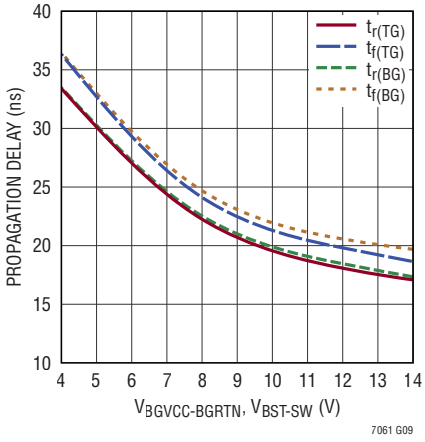
Rise and Fall Time vs Floating Supply Voltage



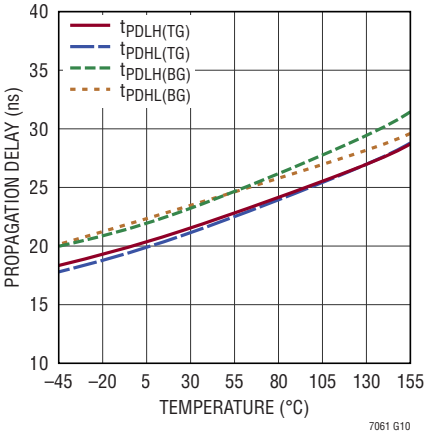
Rise and Fall Time vs Load Capacitance



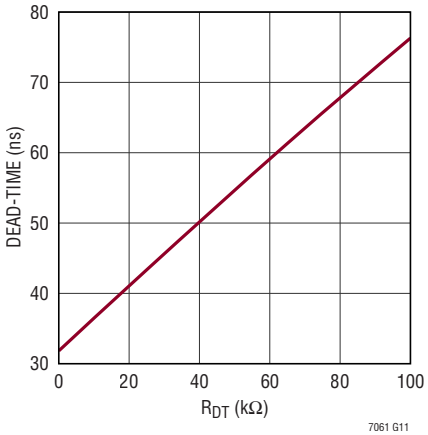
Propagation Delay vs Floating Supply Voltage



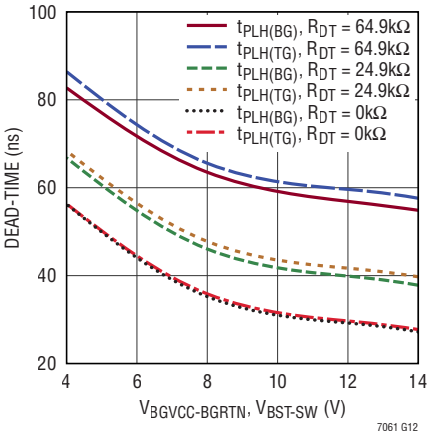
Propagation Delay vs Temperture



Dead-Time vs R_{DT}

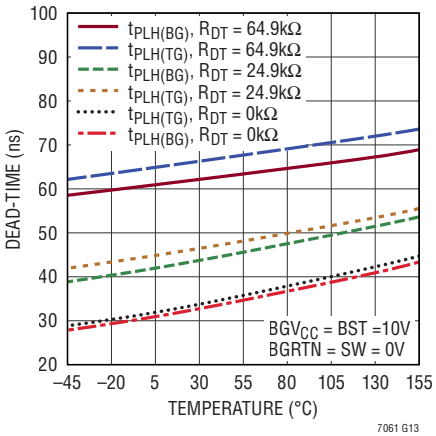


Dead-Time vs Floating Supply Voltage

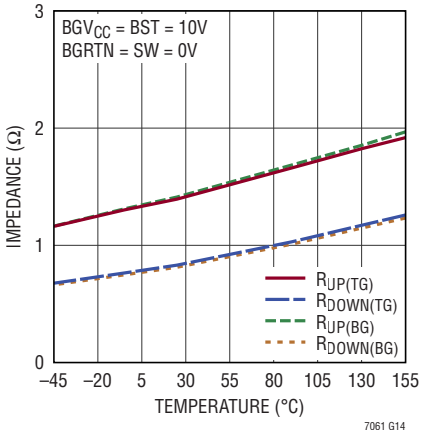


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

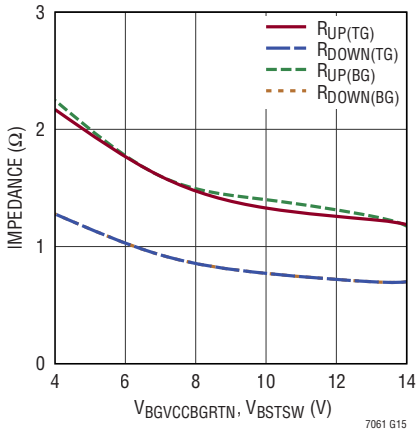
Dead-Time vs Temperature



TG/BG Pull-Up and Pull-Down Resistance vs Temperature



TG/BG Pull-Up and Pull-Down Resistance vs Floating Supply Voltage



PIN FUNCTIONS

V_{CC}: V_{CC} Supply. IC bias supply referred to the SGND pin. An internal 4.5V supply is generated from the V_{CC} supply to bias most of the internal circuitry. A bypass capacitor with a minimum value of 0.1µF should be tied between this pin and the SGND pin.

BGV_{CC}: Bottom MOSFET Driver Supply. The bottom MOSFET gate driver is biased between this pin and BGRTN pin. An external capacitor should be tied between this pin and BGRTN and placed close to the IC.

BGRTN: Bottom MOSFET Driver Return. The bottom gate driver is biased between BGV_{CC} and BGRTN. Kelvin connect BGRTN to the bottom MOSFET source pin for high noise immunity. The voltage difference between the BGRTN pin and the SGND can be –10V to 100V.

BG: Bottom MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between BGRTN and BGV_{CC}.

BST: Top MOSFET Driver Supply. The top MOSFET gate driver is biased between this pin and the SW pin. An external capacitor should be tied between this pin and SW pin and placed close to the IC.

SW: Top MOSFET Driver Return. The top gate driver is biased between BST and SW. Kelvin connect SW to the top MOSFET source pin for high noise immunity. The voltage difference between the SW pin and SGND can be –10V to 100V.

TG: Top MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between SW and BST.

DT: Dead-Time Program Pin Referred to the SGND Pin. A single resistor from this pin to SGND sets the BG/TG low to TG/BG high propagation delay. See the operation section for details.

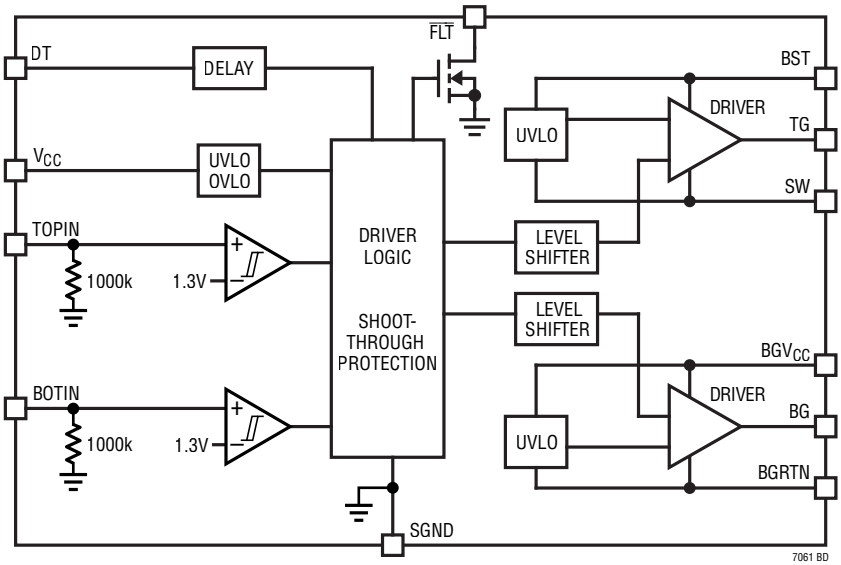
TOPIN: Logic input for top-side driver. If TOPIN is unbiased or floating, TG is held low.

BOTIN: Logic input for bottom-side driver. If BOTIN is unbiased or floating, BG is held low.

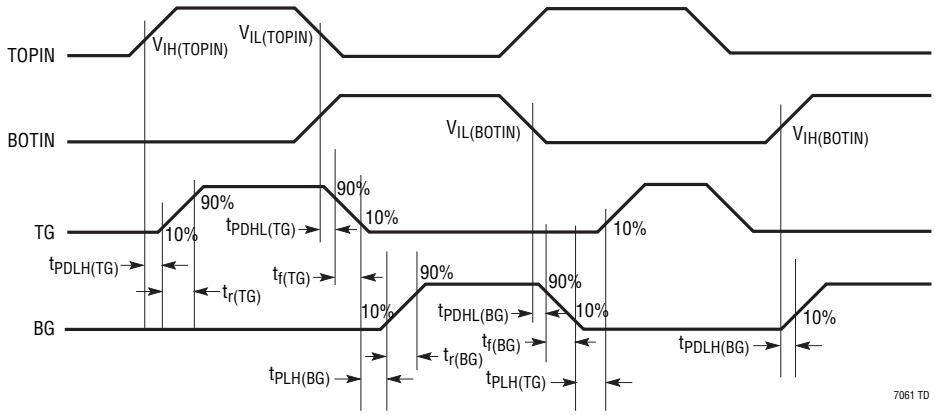
$\overline{FLT}$: Open Drain Fault Output Pin Referred to the SGND Pin. Open-drain output that pulls to SGND during V_{CC} UVLO/OVLO and floating supplies UVLO condition. The typical pull-down resistance is 60Ω.

SGND: Chip Ground. The exposed pad must be soldered to the PCB ground for electrical contact and for rated thermal performance.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

OVERVIEW

The LTC7061 has two ground-referenced, low voltage digital signal inputs to drive two N-channel power MOSFETs in a half bridge configuration. The output BG is driven high or low, swinging between BGV_{CC} and BGRTN, depending on the BOTIN pin. Similarly, the output TG is swinging between BST and SW. Each channel is controlled by its input pints (TOPIN and BOTIN), allowing independent flexibility to control on and off state of the output but does not allow TG and BG outputs to be turned high at the same time.

LTC7061 features robust drive with excellent noise and transient immunity, including large negative ground difference tolerance (–10V) on switch node (SW, BGRTN). The symmetric design allows the half bridge output to be inverting or non-inverting of the input logic.

V_{CC} SUPPLY

V_{CC} is the power supply for the LTC7061's internal circuitry. An internal 4.5V supply is generated from the V_{CC} supply to bias most of the internal circuits referred to SGND. The V_{CC} pin may be tied to the BGV_{CC} pin if SGND and BGRTN are at the same potential. V_{CC} is independent of V_{IN}.

INPUT STAGE (TOPIN, BOTIN)

The LTC7061 employs two logic inputs with fixed transition thresholds. When the voltage on TOPIN is greater than the threshold $V_{IH(TOPIN)}$, TG is pulled up to BST, turning the high side MOSFET on. This MOSFET will stay on until TOPIN falls below $V_{IL(TOPIN)}$. Similarly, when BOTIN is greater than $V_{IH(BOTIN)}$, BG is pulled up to BGV_{CC}, turning the low side MOSFET on. BG will stay high until BOTIN falls below the threshold $V_{IL(BOTIN)}$.

The hysteresis between the corresponding V_{IH} and V_{IL} voltage levels eliminates false triggering due to the noise during switch transitions. However, care should be taken to keep noise from coupling into the input pins (TOPIN, BOTIN), particularly in high frequency and high voltage applications.

When TOPIN/BOTIN pin is floating, there is an internal 1000kΩ pull-down resistor from the TOPIN/BOTIN pin to SGND, keeping the TG/BG default state low if the input is not driven.

PWM controller IC may utilize both TOPIN and BOTIN input pins to perform Discontinuous Conduction Mode (DCM) in switching regulator applications.

OUTPUT STAGE

A simplified version of the LTC7061's output stage is shown in Figure 1. Both TG and BG designs are symmetrical and have floating gate driver outputs. The pull-up device is a PMOS with a typical 1.5Ω $R_{DS(ON)}$ and the pull-down device is a NMOS with a typical 0.8Ω $R_{DS(ON)}$. The wide driver supply voltage ranging from 4V to 14V enables driving different power MOSFETs, such as logic level or higher threshold MOSFETs. However, LTC7061 is optimized for higher threshold MOSFETs (e.g. BST-SW = 10V and BGV_{CC}-BGRTN = 10V). The driver output pull-up and pull-down resistance may increase with lower driver supply voltage.

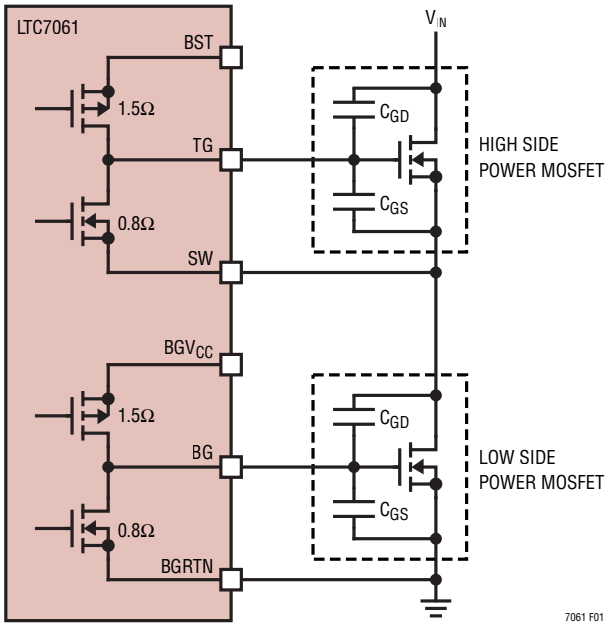


Figure 1. Simplified Output Stage in Half Bridge Configuration

OPERATION

Since power MOSFETs generally account for the majority of the power loss in a converter, it is important to turn them on and off quickly, thereby minimizing the transition time and power loss. The LTC7061's typical 1.5Ω pull-up resistance and 0.8Ω pull-down resistance are equivalent to 3A peak pull-up current and 6A peak pull down current at a 10V driver supply. Both BG and TG can produce a rapid turn-on for the MOSFETs with capability of driving a 3.3nF load with 18ns rise time.

Furthermore, a strong pull-down on the driver outputs prevents cross-conduction current. For example, in the half bridge configuration shown in Figure 1, when BG turns the low side power MOSFET off and TG turns the high side power MOSFET on, the voltage on the SW pin could rise to V_{IN} very rapidly. This high frequency positive voltage transient will couple through the C_{GD} capacitance of the low side power MOSFET to BG pin. If BG pin is not held down sufficiently, the voltage on the BG pin could rise above the threshold voltage of the low side power MOSFET, momentarily turning it back on. As a result, both the high side and low side MOSFETs would be conducting, which would cause significant cross-conduction current to flow through the MOSFETs from V_{IN} to ground, thereby incurring substantial power loss and potentially damaging the MOSFETs. For this reason, short PCB traces for BG and TG pins, minimizing parasitic inductances, are recommended.

PROTECTION CIRCUITRY

When using the LTC7061, care must be taken not to exceed any of the Absolute Maximum Ratings. As an added safeguard, the LTC7061 incorporates overtemperature shutdown feature. If the junction temperature reaches approximately 180°C, the LTC7061 will enter thermal shutdown mode and BG will be pulled to BGRTN; TG will be pulled to SW. Normal operation will resume when the junction temperature cools down below 165°C. The overtemperature level is not production tested. The LTC7061 is guaranteed to operate below 150°C.

The LTC7061 contains both undervoltage and overvoltage lockout detectors that monitor the V_{CC} supply. When V_{CC} falls below 4.3V or rises above 14.6V, the output pins BG and TG are pulled to BGRTN and SW, respectively. This turns off both the external MOSFETs. When V_{CC} reaches adequate supply voltage but less than the overvoltage threshold, normal operation will resume.

Additional undervoltage lockout circuitry is included in each floating driver supply. BG will be pulled down to BGRTN when the floating voltage from BGV_{CC} to BGRTN falls below 3.3V. Similarly, TG will be pulled down to SW when the floating voltage from BST to SW is less than 3.3V.

Both V_{CC}, BST-SW, and BGV_{CC} - BGRTN protection functions are provided with a hysteresis feature. This hysteresis prevents chatter when there is ground noise from the power supply. This also allows the device to accept a small drop in the bias voltage when the device starts switching and quiescent current consumption increases instantly, as well as when the boot-strap circuit charges the boot-strap capacitor during the first instance of BG turn-on causing a drop in V_{CC} voltage.

The normal operation and undervoltage/overvoltage logic table is shown in Table 1.

Table 1. Normal Operation and Undervoltage/Overvoltage Logic

TOPIN	BOTIN	V_{CC} UVLO or OVLO	(BST-SW) UVLO	(BGV_{CC}-BGRTN) UVLO	THERMAL SHUTDOWN	TG	BG	FLTB
X	X	X	X	X	Yes	L	L	L
X	X	Yes	X	X	No	L	L	L
X	H	No	Yes	N	No	L	H	L
H	X	No	No	Yes	No	H	L	L
L	H	No	No	No	No	L	H	H
H	L	No	No	No	No	H	L	H
High-Z	High-Z	No	No	No	No	L	L	H

Note: "X" means "Don't Care", "H" means "High", and "L" means "Low".

ADAPTIVE SHOOT-THROUGH PROTECTION

Internal adaptive shoot-through protection circuitry monitors external MOSFETs to ensure that they do not conduct simultaneously. The LTC7061 does not allow bottom MOSFET to turn on until the gate-source voltage of top MOSFET is sufficiently low, and vice-versa. This feature improves efficiency and reliability by eliminating potential shoot-through current through the MOSFETs during switching transitions.

OPERATION

ADJUSTABLE DEAD-TIME

To ensure robust shoot-through protection in high voltage half bridge configuration and switched capacitor converter applications, LTC7061 provides a DT pin which can be used to program the propagation delay during BG/TG low to TG/BG high transition (Dead-Time). An external resistor (R_{DT}) from the DT pin to the SGND equally sets both BG low to TG high propagation delay and TG low to BG high propagation delay. Their relationship can be seen in Figure 2. The Dead-Time can be estimated by the following equation when the R_{DT} is less than 100kΩ:

$$\text{Dead-Time} = R_{DT} \bullet 0.44\text{ns/k}\Omega + 32\text{ns}$$

If DT pin is shorted to SGND, the Dead-Time is 32ns. If DT Pin is floating, the Dead-Time is around 250ns.

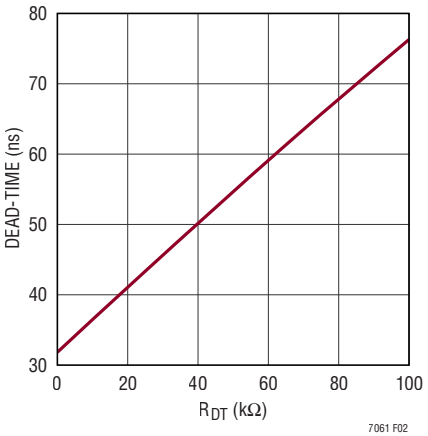


Figure 2. Dead-Time vs R_{DT}

INPUT AND OUTPUT LOGIC RELATIONSHIP

LTC7061 output signal's dead time is always set to the longer of either the driver's minimum dead time, t_{dt}, or the input signal's own dead time. If BOTIN is turned high while TOPIN is still high, TOPIN will mute BOTIN rising edge. BG is allowed to go high after TOPIN goes low plus t_{dt}, and vice versa. This feature eliminates cross conduction and prevents output being disturbed by the other input, in the case of incorrect timing from the controller. It does not affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in Figure 3.

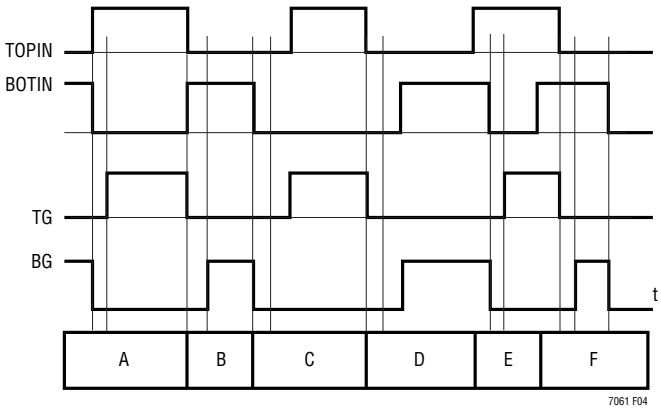


Figure 3. LTC7061 Input and Output Logic Relationship

Condition A: TOPIN goes high, BOTIN goes low. BOTIN sets BG low immediately, TG is allowed to go high after t_{dt}.

Condition B: TOPIN goes low, BOTIN goes high. TOPIN sets TG low immediately, BG is allowed to go high after t_{dt}.

Condition C: TOPIN rising and BOTIN falling own dead time is longer than t_{dt}. Thus when TOPIN goes high, TG is set high immediately.

Condition D: TOPIN falling and BOTIN rising own dead time is longer than t_{dt}. Thus when BOTIN goes high, BG is set high immediately.

Condition E: TOPIN goes high, while BOTIN is still high. BOTIN mutes TOPIN rising edge. TG is allowed to go high after BOTIN goes low plus t_{dt}.

Condition F: BOTIN goes high, while TOPIN is still high. TOPIN mutes BOTIN rising edge. BG is allowed to go high after TOTIN goes low plus t_{dt}.

Note: TG refers to SW and BG refers to BGRTN.

OPERATION

FAULT FLAG

$\overline{FLT}$ pin is connected to the open-drain of an internal N-channel MOSFET. It needs a pull-up resistor (e.g. 51kΩ) tied to a supply such as V_{CC} or any other bias voltage up to 15V. The $\overline{FLT}$ pin is pulled low to SGND immediately if any of these conditions are met:

a. The V_{CC} is below its UVLO threshold or above its OVLO threshold.

b. (BGV_{CC}-BGRTN) is below its UVLO threshold.

c. (BST-SW) is below its UVLO threshold.

d. The junction temperature reaches approximately 180°C.

When all the faults are cleared, $\overline{FLT}$ pin is pulled up by the external resistor after a built-in 100µs delay.

APPLICATIONS INFORMATION

BOOTSTRAPPED SUPPLY (BGV_{CC}-BGRTN, BST-SW)

Either or both of the BGV_{CC}-BGRTN and BST-SW supplies can be bootstrapped supplies. An external boost capacitor, C_B, connected between BGV_{CC} and BGRTN, or between BST and SW, supplies the gate driver voltage for its respective MOSFET driver. When the external MOSFET is turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the MOSFET and turns it on.

The charge to turn on the external MOSFET is referred to gate charge, Q_G, and is typically specified in the external MOSFET datasheet. The boost capacitor, C_B, needs to have at least 10 times the gate capacitance to turn on the external MOSFET fully. Gate charge can range from 5nC to hundreds of nC and is influenced by the gate drive level and type of external MOSFET used. For most applications, a capacitor value of 0.1µF for C_B will be sufficient. However, if multiple MOSFETs are paralleled and driven by the LTC7061, C_B capacitance needs to be increased correspondingly and the following relationship for the CB should be maintained:

$$C_B > \frac{10 \bullet \text{External MOFSET } Q_G}{1V}$$

An external supply, typically V_{CC} connected through a Schottky diode, is required to keep the C_B charged. The LTC7061 does not charge the C_B and always discharges the C_B. When the BG/TG is high, the total current from BGV_{CC}/BST to BGRTN/SW and SGND is typically 146µA; when the BG/TG is low, the total current from BGV_{CC}/BST is typically 9µA.

POWER DISSIPATION

To ensure proper operation and long-term reliability, the LTC7061 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + (P_D)(\theta_{JA})$$

where:

T_J = junction temperature

T_A = ambient temperature

P_D = power dissipation

θ_{JA} = junction-to-ambient thermal resistance

Power dissipation consists of standby, switching and capacitive load power losses:

$$P_D = P_{DC} + P_{AC} + P_{QG}$$

where:

P_{DC} = quiescent power loss

P_{AC} = internal switching loss at input frequency f_{IN}

P_{QG} = loss due to turning on and off external MOSEFT with gate charge Q_G at frequency f_{IN}

The LTC7061 consumes very little quiescent current. The DC power loss at V_{CC} = 10V is only (10V)(0.3mA) = 3mW.

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal nodal capacitances and cross-conduction currents in internal logic gates. The sum of the

APPLICATIONS INFORMATION

quiescent current and internal switching current with no load are shown in the Typical Performance Characteristics plot of Switching Supply Current vs Input Frequency.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads C_{LOAD} on BG and TG at switching frequency f_{IN}, the load losses would be:

$$P_{CLOAD} = (C_{LOAD})(f_{IN})[(V_{BST-SW})^2 + (V_{BGVCC-BGRTN})^2]$$

In a typical synchronous buck configuration, the V_{CC} is connected to the power for the bottom MOSFET driver, BGV_{CC}. V_{BST-SW} is equal to V_{CC} -V_D, where V_D is the forward voltage drop of the external Schottky diode between V_{CC} and BST. If this drop is small relative to V_{CC}, the load losses can be approximated as:

$$P_{CLOAD} \approx 2(C_{LOAD})(f_{IN})(V_{CC})^2$$

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its V_{GS} voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge, Q_G. The Q_G value corresponding to the MOSFET's V_{GS} value (V_{CC} in this case) can be readily obtained from the manufacturer's Q_G vs V_{GS} curves. For identical MOSFETs on BG and TG:

$$P_{QG} \approx 2(Q_G)(f_{IN})(V_{CC})$$

BYPASSING AND GROUNDING

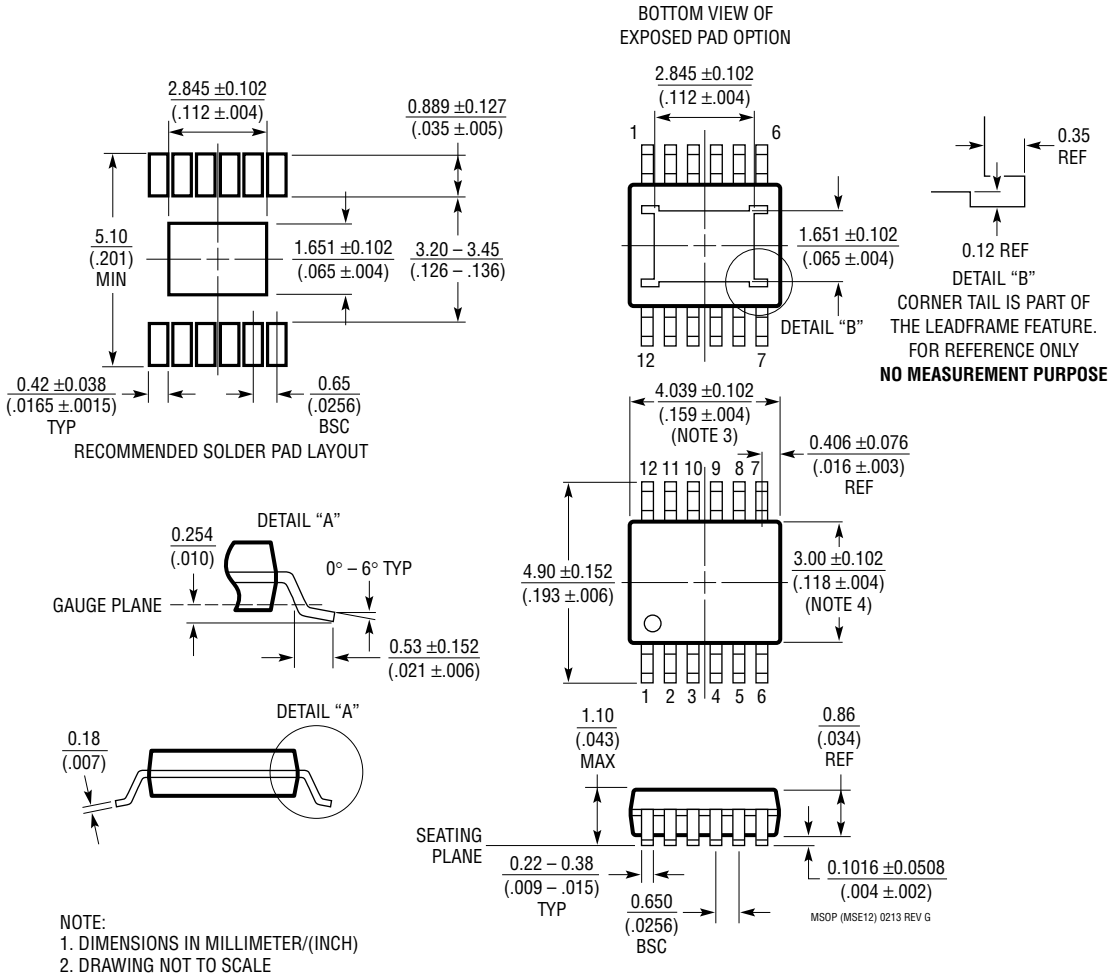
The LTC7061 requires proper bypassing on the V_{CC}, V_{BST-SW}, and $V_{BGVCC-BGRTN}$ supplies due to its high speed switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimum performance form the LTC7061:

- Mount the bypass capacitors as close as possible between the V_{CC} and SGND pins, the BGV_{CC} and BGRTN pins, and the BST and SW pins. The leads should be shortened as much as possible to reduce lead inductance.
- Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC7061 switches greater than 5A peak currents and any significant ground drop will degrade signal integrity.
- Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- Kelvin connect the TG pin to the top MOSFET gate and SW pin to the top MOSFET source. Kelvin connect the BG pin to the bottom MOSFET gate and BGRTN to the bottom MOSFET source. Keep the copper trace between the driver output pin and load short and wide.
- Be sure to solder the Exposed Pad on the back side of the LTC7061 packages to the board. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than specified for the packages.

PACKAGE DESCRIPTION

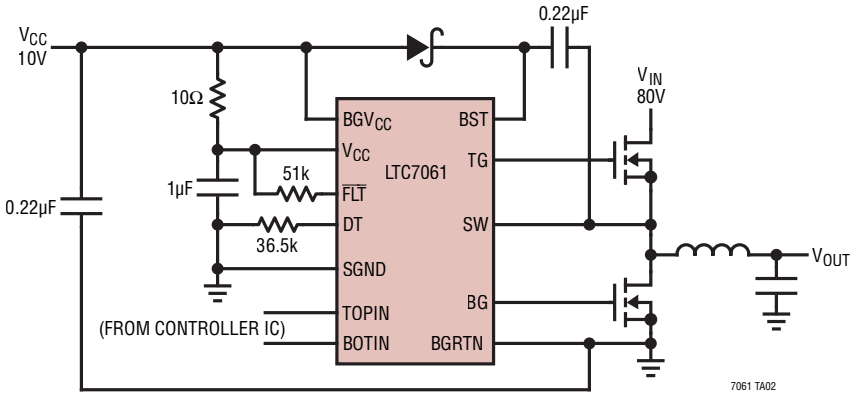
MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

High Input Voltage Buck Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7060	100V Half Bridge Driver with Floating Grounds and Programmable Dead-Time	Up to 100V Supply Voltage, 6V ≤ V_{CC} ≤ 14V, 0.8Ω Pull-Down, 1.5Ω Pull-Up, Symmetric Floating Gate Driver Architecture, Adjustable Dead-Time from 31ns to 76ns
LTC7062	100V Dual High-Side MOSFET Gate Driver	Up to 100V Supply Voltage, 5V ≤ V_{CC} ≤ 14V, 0.8Ω Pull-Down, 1.5Ω Pull-Up for Fast Turn-On/Off, Symmetric Floating Gate Driver Architecture
LTC7063	150V Half Bridge Driver with Floating Grounds and Programmable Dead-Time	Up to 150V Supply Voltage, 6V ≤ V_{CC} ≤ 14V, 0.8Ω Pull-Down, 1.5Ω Pull-Up, Symmetric Floating Gate Driver Architecture, Adjustable Dead-Time from 31ns to 76ns
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 4V≤V_{CC}≤6.5V, Adaptive Shoot-Through Protection, 2mm x 3mm DFN-8
LTC4442/ LTC4442-1	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 6V≤V_{CC}≤9.5V, 2.4A Peak Pull-Up/5A Peak Pull-Down
LTC4444/ LTC4444-5	High Voltage Synchronous N-Channel MOSFET driver with Shoot-Through Protection	Up to 100V Supply Voltage, 4.5V/7.2V≤ V_{CC}≤13.5V, 3A Peak Pull-Up/0.55Ω Peak Pull-Down
LTC7851	Quad Output, Multiphase, Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing	Operates with Power Block, DrMOS or External Drivers and MOSFETs, 3V ≤V_{IN}≤24V
LTC3861	Dual, Multiphase, Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing	Operates with Power Block, DrMOS or External Gate Driver and MOSFETs, 3V ≤V_{IN}≤24V
LTC3774	Dual, Multiphase, Current Mode Synchronous Step-Down DC/DC Controller for Sub-Milliohm DCR Sensing	Operates with DrMOS, Power Blocks or External Drivers/MOSFETs, 4.5V ≤V_{IN}≤38V, 0.6V ≤V_{OUT}≤3.5V