

FEATURES

Ultrawideband frequency range: 9 kHz to 44 GHz

Reflective design

Low insertion loss with impedance match

0.9 dB typical to 18 GHz

1.4 dB typical to 40 GHz

1.6 dB typical to 44 GHz

Low insertion loss without impedance match

0.9 dB typical to 18 GHz

1.7 dB typical to 40 GHz

2.2 dB typical to 44 GHz

High input linearity

P1dB: 27.5 dBm typical

IP3: 50 dBm typical

High RF input power handling

Through path: 27 dBm

Hot switching: 27 dBm

No low frequency spurious

RF settling time (50% V_{CTL} to 0.1 dB final RF output): 3.4 μ s

12-terminal, 2.25 mm \times 2.25 mm LGA package

Pin compatible with the [ADRF5024](#) fast switching version

APPLICATIONS

Industrial scanners

Test and instrumentation

Cellular infrastructure: 5G mmWave

Military radios, radars, electronic counter measures (ECMs)

Microwave radios and very small aperture terminals (VSATs)

GENERAL DESCRIPTION

The ADRF5025 is a reflective single-pole double-throw (SPDT) switch, manufactured in silicon process.

This switch operates from 9 kHz to 44 GHz with better than 1.6 dB of insertion loss and 35 dB of isolation. The ADRF5025 has an radio frequency (RF) input power handling capability of 27 dBm for both the through path and hot switching.

The ADRF5025 draws a low current of 14 μ A on the positive supply of +3.3 V and 120 μ A on negative supply of -3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)/low voltage transistor to transistor logic (LVTTL)-compatible controls.

FUNCTIONAL BLOCK DIAGRAM

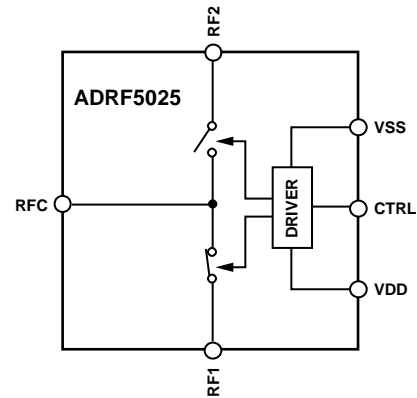


Figure 1.

The ADRF5025 is pin compatible with the [ADRF5024](#), low frequency cutoff version, which operates from 100 MHz to 44 GHz.

The ADRF5025 RF ports are designed to match a characteristic impedance of 50 Ω . For ultrawideband products, impedance matching on the RF transmission lines can further optimize high frequency insertion loss and return loss characteristics. Refer to the Electrical Specifications section, Typical Performance Characteristics section, and Applications Information section for more details.

The ADRF5025 comes in a 2.25 mm \times 2.25 mm, 12-terminal, RoHS-compliant, land grid array (LGA) package and can operate from -40°C to +105°C.

Rev. B

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REVISION HISTORY

5/2020—Rev. A to Rev. B

Changes to Return Loss Parameter, Table 1	3
Changes to Table 2	5
Changes to Insertion Loss, Return Loss, and Isolation Section, Figure 7, and Figure 10	7
Changes to Theory of Operation Section.....	9

5/2018—Rev. 0 to Rev. A

Change to Input Linearity Parameter, Table 1.....	4
Change to RF Input Power Parameter, Table 2	5
Updated Outline Dimensions	13
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5/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = -3.3 V, V_{CTL} = 0 V or 3.3 V, and case temperature (T_{CASE}) = 25°C for a 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.009		44,000	MHz
INSERTION LOSS						
Between RFC and RF1/RF2 (On) With Impedance Match		See Figure 24 9 kHz to 18 GHz 18 GHz to 26 GHz 26 GHz to 35 GHz 35 GHz to 40 GHz 40 GHz to 44 GHz		0.9 1.2 1.3 1.4 1.6		dB dB dB dB dB
Without Impedance Match		See Figure 25 9 kHz to 18 GHz 18 GHz to 26 GHz 26 GHz to 35 GHz 35 GHz to 40 GHz 40 GHz to 44 GHz		0.9 1.0 1.4 1.7 2.2		dB dB dB dB dB
RETURN LOSS						
RFC and RF1/RF2 (On) With Impedance Match		See Figure 24 9 kHz to 18 GHz 18 GHz to 26 GHz 26 GHz to 35 GHz 35 GHz to 40 GHz 40 GHz to 44 GHz		17 13 12 13 18		dB dB dB dB dB
Without Impedance Match		See Figure 25 9 kHz to 18 GHz 18 GHz to 26 GHz 26 GHz to 35 GHz 35 GHz to 40 GHz 40 GHz to 44 GHz		20 20 13 11 10		dB dB dB dB dB
ISOLATION						
Between RFC and RF1/RF2		9 kHz to 18 GHz 18 GHz to 26 GHz 26 GHz to 35 GHz 35 GHz to 40 GHz 40 GHz to 44 GHz		42 41 39 36 35		dB dB dB dB dB
Between RF1 and RF2		9 kHz to 18 GHz 18 GHz to 26 GHz 26 GHz to 35 GHz 35 GHz to 40 GHz 40 GHz to 44 GHz		48 46 44 43 40		dB dB dB dB dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t _{RISE} , t _{FALL}	10% to 90% of RF output		0.6		μs
On and Off Time	t _{ON} , t _{OFF}	50% V _{CTL} to 90% of RF output		1.7		μs
RF Settling Time 0.1 dB		50% V _{CTL} to 0.1 dB of final RF output		3.4		μs
0.05 dB		50% V _{CTL} to 0.05 dB of final RF output		4.2		μs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT LINEARITY ¹		5 MHz to 40 GHz				
1 dB Power Compression	P1dB			27.5		dBm
Third-Order Intercept	IP3	Two tone input power = 12 dBm each tone, $\Delta f = 1$ MHz		50		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I _{DD}			14		μ A
Negative Supply Current	I _{SS}			120		μ A
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V _{INL}		0		0.8	V
High	V _{INH}		1.2		3.3	V
Current						
Low and High	I _{INL} , I _{INH}			<1		μ A
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V _{DD}		3.15		3.45	V
Negative	V _{SS}		-3.45		-3.15	V
Digital Control Voltage	V _{CTL}		0		V _{DD}	V
RF Input Power ²	P _{IN}	f = 5 MHz to 40 GHz, T _{CASE} = 85°C ³				
Through Path		RF signal is applied to RFC or through connected RF1/RF2			27	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			27	dBm
Case Temperature	T _{CASE}		-40		+105	°C

¹ For input linearity performance over frequency, see Figure 13 to Figure 16.

² For power derating over frequency, see Figure 2 and Figure 3.

³ For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Positive Supply Voltage	-0.3 V to +3.6 V
Negative Supply Voltage	-3.6 V to +0.3 V
Digital Control Input Voltage	
Voltage	-0.3 V to VDD + 0.3 V
Current	3 mA
RF Input Power ¹ (f = 5 MHz to 40 GHz, T _{CASE} = 85°C ²)	
Through Path	27.5 dBm
Hot Switching	27.5 dBm
RF Input Power Under Unbiased Condition ¹ (V _{DD} , V _{SS} = 0 V)	21 dBm
Temperature	
Junction, T _J	135°C
Storage Range	-65°C to +150°C
Reflow	260°C
ESD Sensitivity	
Human Body Model (HBM)	
RFC, RF1, and RF2 Pins	1000 V
Digital Pins	2000 V
Charged Device Model (CDM)	1250 V

¹ For power derating vs. frequency, see Figure 2 and Figure 3. This power derating is applicable for insertion loss path and hot switching power specifications.

² For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-12-3, Through Path	352	°C/W

POWER DERATING CURVES

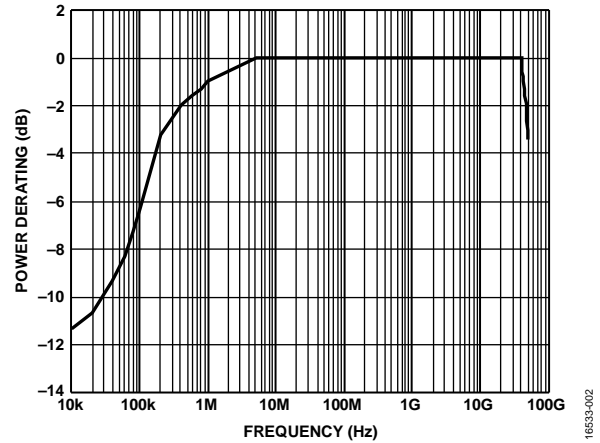


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

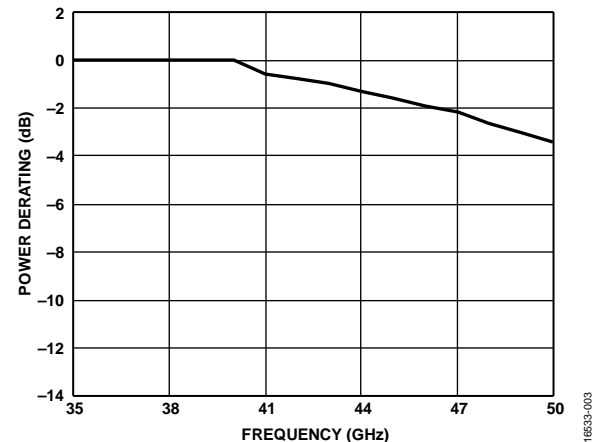


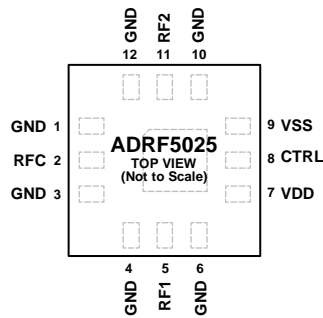
Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND OF THE PCB.
 Figure 4. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 6, 10, 12	GND	Ground. These pins must be connected to the RF/dc ground of the PCB.
2	RFC	RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
5	RF1	RF Port 1. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
7	VDD	Positive Supply Voltage.
8	CTRL	Control Input Voltage. See Figure 6 for the interface schematic.
9	VSS	Negative Supply Voltage.
11	RF2	RF Port 2. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

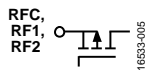


Figure 5. RFx Pins Interface Schematic

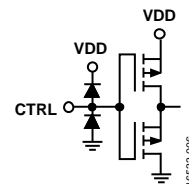


Figure 6. CTRL Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 3.3 V, VSS = -3.3 V, VCTL = 0 V or VDD, and TCASE = 25°C for a 50 Ω system, unless otherwise noted.

Insertion loss and return loss are measured on the probe matrix board using ground-signal-ground (GSG) probes close to the RFx pins. See the Applications Information section for details on the evaluation and probe matrix boards.

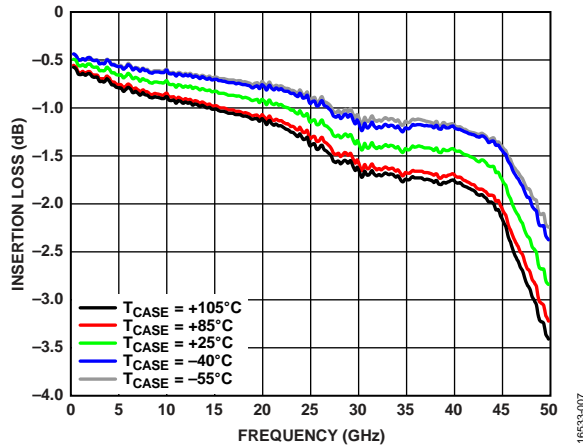


Figure 7. Insertion Loss vs. Frequency with Impedance Match

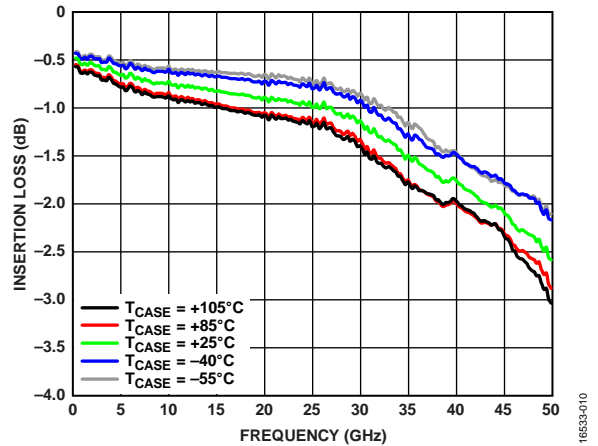


Figure 10. Insertion Loss vs. Frequency Without Impedance Match

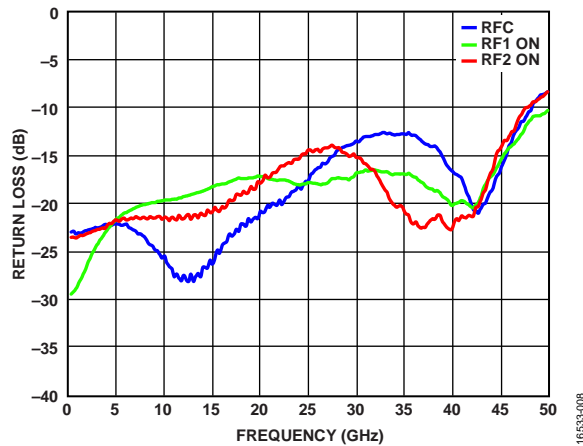


Figure 8. Return Loss vs. Frequency for RFC and RFx (On) with Impedance Match

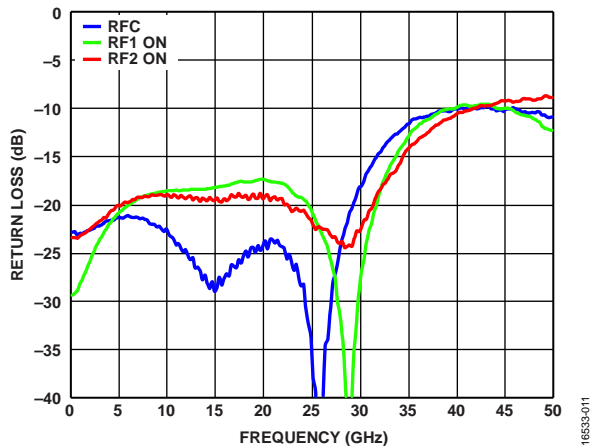


Figure 11. Return Loss vs. Frequency for RFC and RFx (On) Without Impedance Match

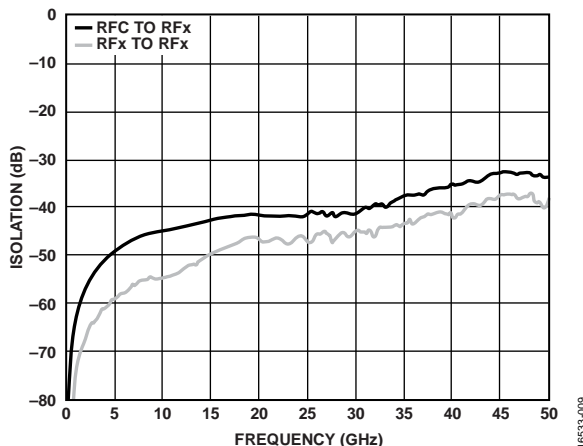


Figure 9. Isolation vs. Frequency with Impedance Match

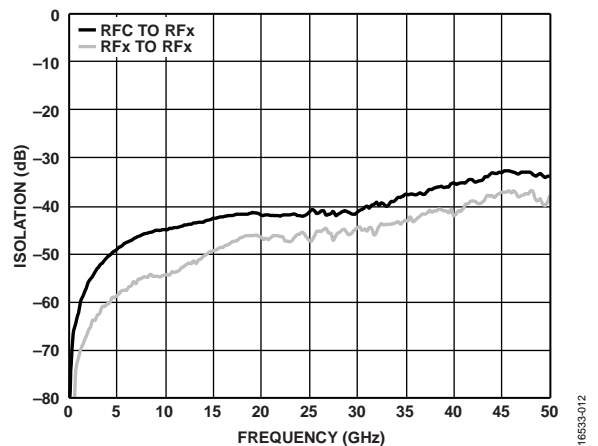


Figure 12. Isolation vs. Frequency Without Impedance Match

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 3.3 V, VSS = -3.3 V, VCTL = 0 V or VDD, and TCASE = 25°C for a 50 Ω system, unless otherwise noted. All of the large signal performance parameters were measured on the evaluation board.

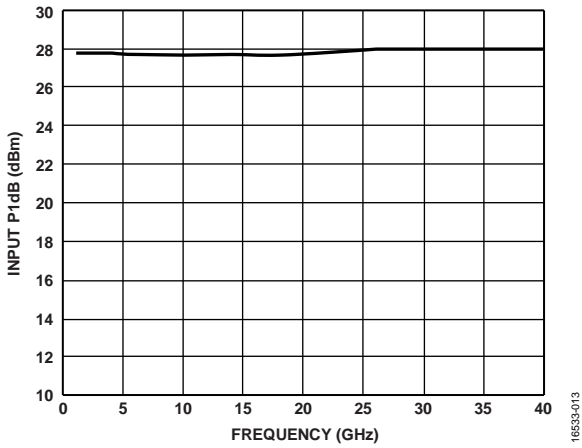


Figure 13. Input P1dB vs. Frequency

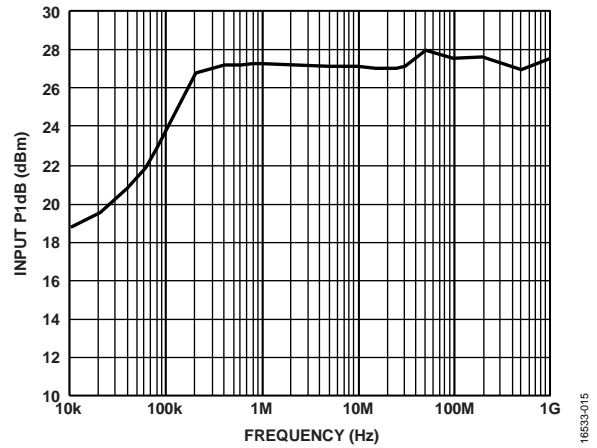


Figure 15. Input P1dB vs. Frequency (Low Frequency Detail)

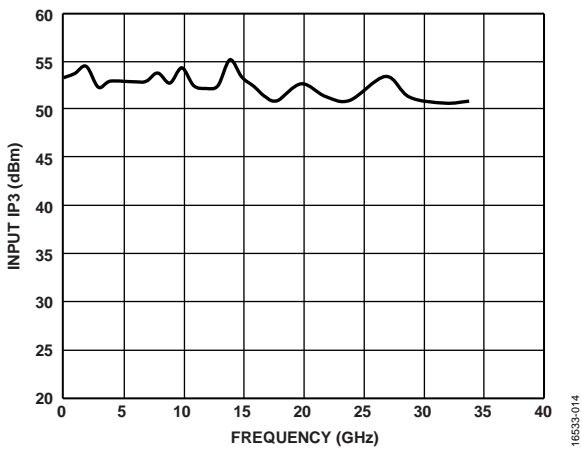


Figure 14. Input IP3 vs. Frequency over Temperature

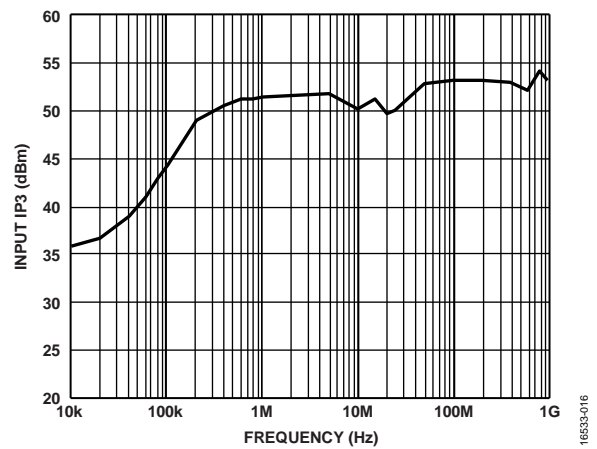


Figure 16. Input IP3 vs. Frequency over Temperature (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5025 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

All of the RF ports (RFC, RF1, and RF2) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω . Therefore, external matching networks are not required. However, impedance matching on transmission lines can be used to improve insertion loss and return loss performance at high frequencies.

The ADRF5025 integrates a driver to perform logic functions internally and provides the user with the advantage of a simplified CMOS/LVTTL-compatible control interface. This driver features a single digital control input pin, CTRL. The logic level applied to the CTRL pin determines which RF port is in the insertion loss state and in the isolation state (see Table 5).

The unselected RF port of the ADRF5025 is reflective. The isolation path provides high isolation between the unselected port and the insertion loss path.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Apply the digital control inputs. The relative order of the control inputs is not important. However, powering the digital control inputs before the VDD supply may inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 k Ω resistor to limit the current flowing in to the control pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 5. Control Voltage Truth Table

Digital Control Input (V_{CTRL})	RF Path	
	RF1 to RFC	RF2 to RFC
Low	Isolation (off)	Insertion loss (on)
High	Insertion loss (on)	Isolation (off)

APPLICATIONS INFORMATION

EVALUATION BOARD

The [ADRF5025-EVALZ](#) is a 4-layer evaluation board. The outer copper (Cu) layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) and are separated by dielectric materials. Figure 17 shows the evaluation board stackup.

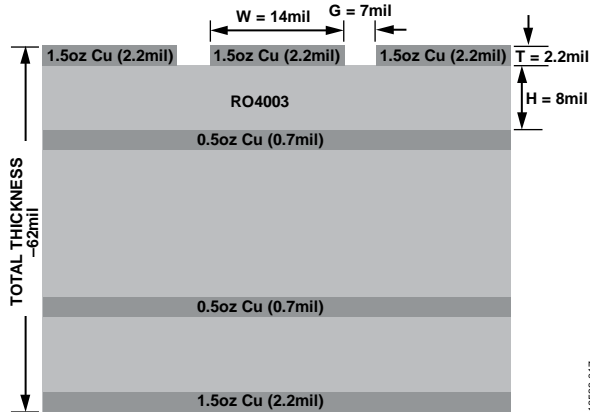


Figure 17. Evaluation Board (Cross Section View)

All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges.

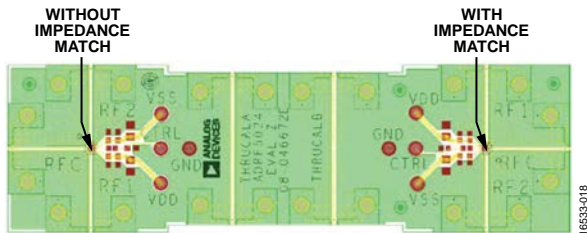


Figure 18. Evaluation Board Layout, Top View

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with trace width of 14 mil and ground clearance of 7 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

The [ADRF5025-EVALZ](#) has two layouts implemented; with and without impedance matching. By default, the impedance matched circuit is populated. For more details on the impedance matched circuit, refer to Impedance Matching in the Probe Matrix Board section.

THRU CAL can be used to calibrate out the board loss effects from the [ADRF5025-EVALZ](#) evaluation board measurements to determine the device performance at the pins of the IC. Figure 19 shows the typical board loss for the [ADRF5025-EVALZ](#) evaluation board at room temperature, the embedded insertion loss, and the de-embedded insertion loss for ADRF5025.

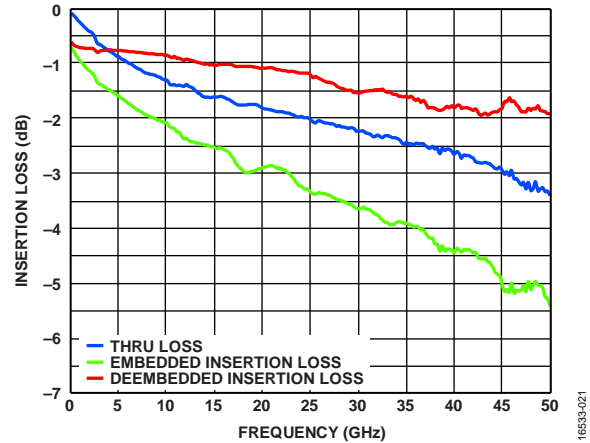


Figure 19. Insertion Loss vs. Frequency

Figure 20 shows the actual [ADRF5025-EVALZ](#) with its component placement.

Two power supply ports are connected to the VDD and VSS test points, TP7 and TP5 (or TP3 and TP1 if using without the impedance match circuit), and the ground reference is connected to the GND test point, TP4 or TP8. On the supply traces, VDD and VSS, a 100 pF bypass capacitor filters high frequency noise. Additionally, unpopulated components positions are available for applying extra bypass capacitors.

A control port is connected to the CTRL test point, TP6 (or TP2 for without the impedance match circuit). There are provisions for the resistor capacitor (RC) filter to eliminate dc-coupled noise, if needed, by the application. The resistor can also improve the isolation between the RF and the control signal.

The RF input and output ports (RFC, RF1, and RF2) are connected through 50 Ω transmission lines to the 2.4 mm RF launchers, J10, J9, and J8 (or J2, J3, and J1 for the without impedance match circuit), respectively. These high frequency RF launchers are by contact and are not soldered to the board. A THRU cal line connects the unpopulated J6 and J7 launchers (or J4 and J5 for without the impedance match circuit). This transmission line is used to estimate the loss due to the PCB over the environmental conditions being evaluated.

The schematic of the [ADRF5025-EVALZ](#) evaluation board is shown in Figure 21.

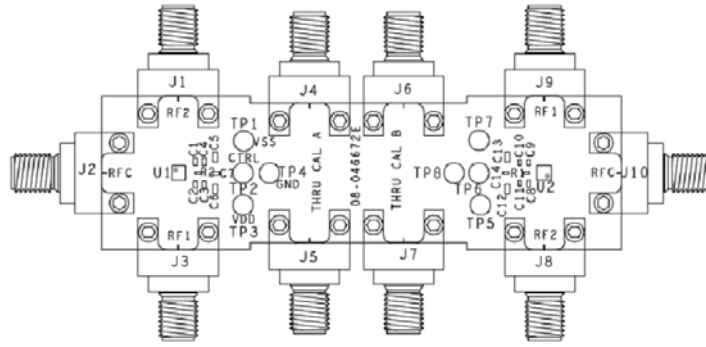


Figure 20. Evaluation Board Component Placement

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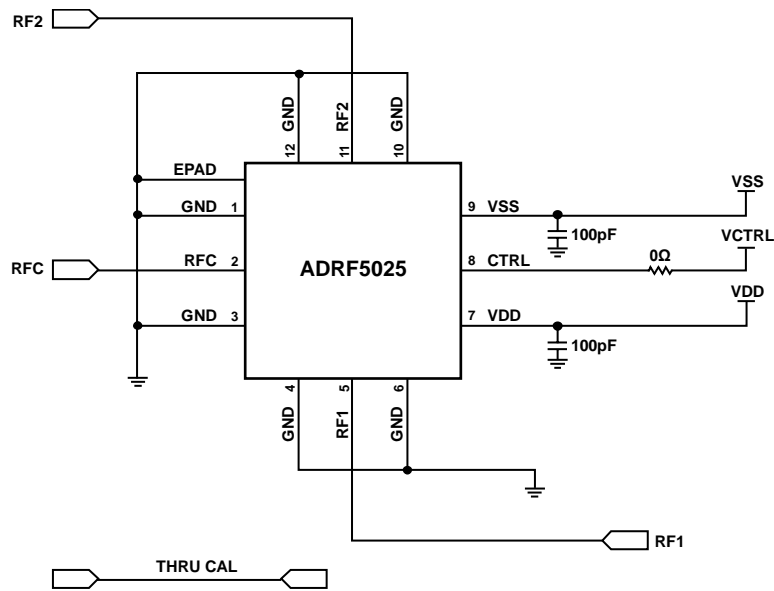


Figure 21. Simplified Evaluation Board Schematic

16633-020

Table 6. Evaluation Board Components

Component	Default Value	Description
C8, C9	100 pF	Capacitors, C0402 package
J8 to J10	Not applicable	2.4 mm end launch connectors (Southwest Microwave: 1492-04A-5)
R2	0 Ω	Resistor, 0402 package
TP5 to TP8	Not applicable	Through hole mount test points
U2	ADRF5025	ADRF5025 SPDT switch, Analog Devices, Inc.
PCB	08-046672E	Evaluation PCB, Analog Devices

PROBE MATRIX BOARD

The probe matrix board is a 4-layer board. Similar to the evaluation board, this board also uses a 8 mil Rogers RO4003 dielectric. The outer copper layers are 0.5 oz (0.7 mil) copper plated to 1.5 oz (2.2 mil). The RF transmission lines were designed using a CPWG model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω.

Figure 22 and Figure 23 show the cross section and top view of the board, respectively. Measurements are made using GSG probes at close proximity to the RFX pins. Unlike the evaluation board, probing reduces reflections caused by mismatch arising from connectors, cables, and board layout, resulting in a more accurate measurement of the device performance.



Figure 22. Probe Matrix Board (Cross Section View)

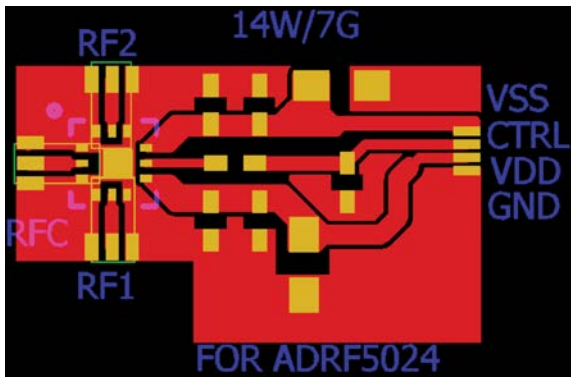


Figure 23. Probe Board Layout (Top View)

The probe matrix board includes a through reflect line (TRL) calibration kit allowing board loss deembedding. The actual board duplicates the same layout in matrix form to assemble multiple devices at one time. All S parameters were measured on this board.

Impedance Matching

Impedance matching at the RFX pins can improve the insertion loss and return loss at high frequencies. Figure 24 and Figure 25 show the difference in the transmission lines at the RFC, RF1, and RF2 pins. This same circuit is implemented on the probe matrix boards and the evaluation boards.

The dimensions of the 50 Ω lines are 14 mil trace width and 7 mil gap. To implement this impedance matched circuit, a 5 mil trace with a width of 5 mils was inserted between the pin pad and the 50 Ω trace. The calibration kit reference kit does not include the 5 mil matching line, and therefore, the measured insertion loss includes the losses of the matching circuit.

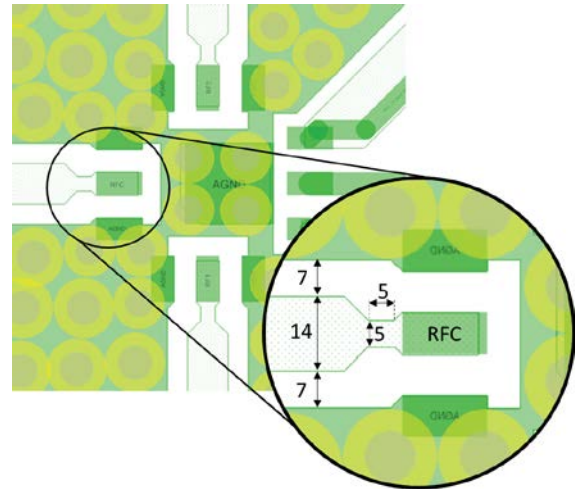


Figure 24. With Impedance Match

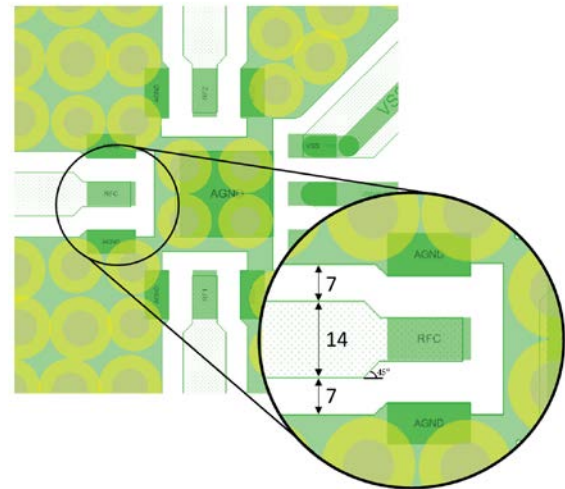


Figure 25. Without Impedance Match

OUTLINE DIMENSIONS

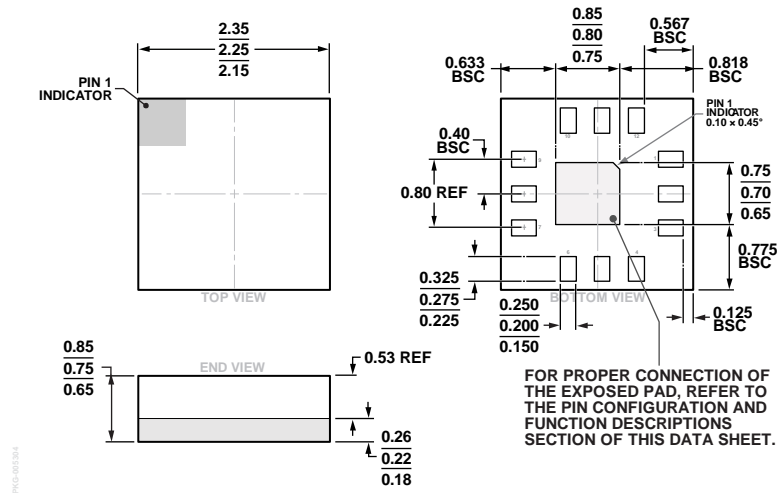


Figure 26. 12-Terminal Land Grid Array [LGA]
 2.25 mm × 2.25 mm Body and 0.75 mm Package Height
 (CC-12-3)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Marking Code
ADRF5025BCCZN	-40°C to +105°C	12-Terminal Land Grid Array [LGA]	CC-12-3	25
ADRF5025BCCZN-R7	-40°C to +105°C	12-Terminal Land Grid Array [LGA]	CC-12-3	25
ADRF5025-EVALZ		Evaluation Board		

¹ Z = RoHS Compliant Part.