



64K (8K x 8) Static RAM

Features

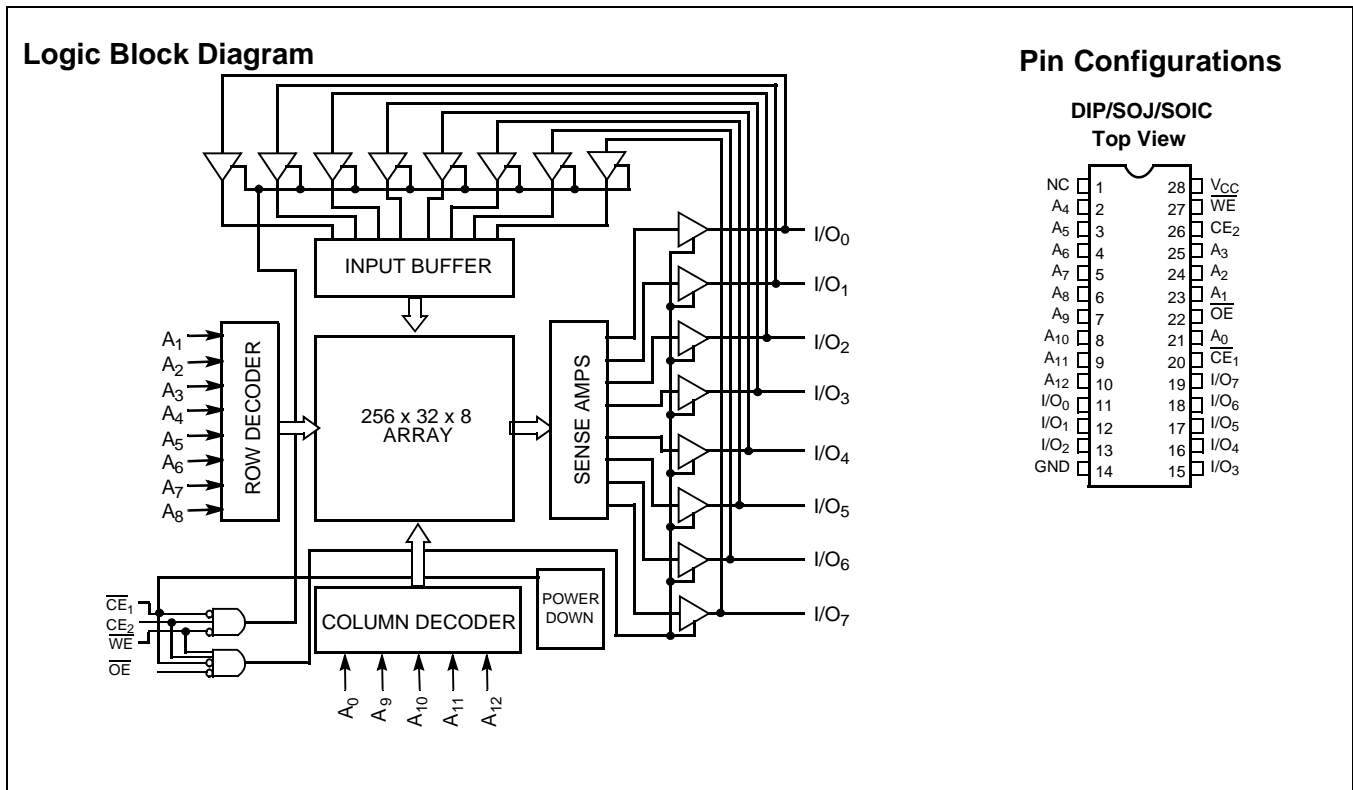
- Pin- and function-compatible with CY7C185
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 60 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
 - $I_{SB2} = 3 \text{ mA}$
- CMOS for optimum speed/power
- Data Retention at 2.0V
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- Available in Lead (Pb)-Free Packages

Functional Description^[1]

The CY7C185D is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), and active LOW output enable (\overline{OE}) and three-state drivers. This device has an automatic power-down feature (\overline{CE}_1 or CE_2), reducing the power consumption when deselected.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE}_1 and \overline{WE} inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE}_1 and \overline{OE} active LOW, CE_2 active HIGH, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH. The CY7C185D is in a standard 28-pin 300-mil-wide DIP, SOJ, or SOIC Pb-Free package.



Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Selection Guide

	CY7C185D-10	CY7C185D-12	CY7C185D-15	Unit
Maximum Access Time	10	12	15	ns
Maximum Operating Current	60	50	40	mA
Maximum Standby Current	3	3	3	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs in High-Z State^[2] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[2]..... -0.5V to $V_{CC} + 0.5V$
 Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C185D-10		7C185D-12		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3V$	2.0	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	µA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1	+1	-1	+1	µA
I_{OS}	Output Short Circuit Current ^[3]	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}$		60		50	mA
I_{SB1}	Automatic Power-down Current	Max. V_{CC} , $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ Min. Duty Cycle = 100%		10		10	mA
I_{SB2}	Automatic Power-down Current	Max. V_{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		3.0		3.0	mA
Parameter	Description	Test Conditions	7C185D-15		Unit		
			Min.	Max.			
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$		2.4		V	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$			0.4	V	
V_{IH}	Input HIGH Voltage			2.0	$V_{CC} + 0.3V$	V	
V_{IL}	Input LOW Voltage ^[2]			-0.5	0.8	V	
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		-1	+1	µA	
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled		-1	+1	µA	
I_{OS}	Output Short Circuit Current ^[3]	$V_{CC} = \text{Max.}, V_{OUT} = GND$			-300	mA	
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}$			40	mA	
I_{SB1}	Automatic Power-down Current	Max. V_{CC} , $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ Min. Duty Cycle = 100%			10	mA	
I_{SB2}	Automatic Power-down Current	Max. V_{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$			3.0	mA	

Capacitance^[4]

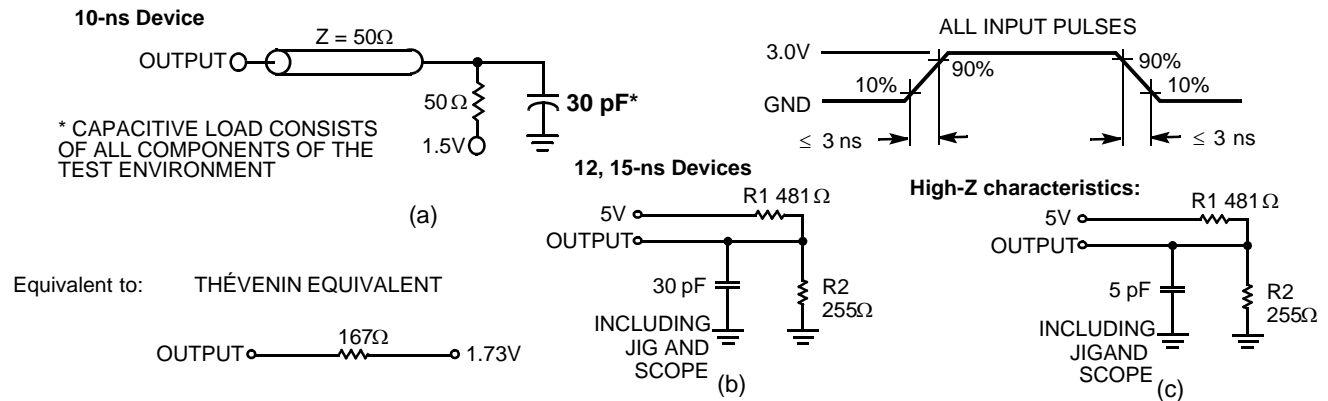
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 5.0V$	7	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

- V_{IL} (min.) = -2.0V and V_{IH} (max) = $V_{CC} + 2V$ for pulse durations of less than 20 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance^[4]

Parameter	Description	Test Conditions	All-Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient) ^[4]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case) ^[4]		TBD	°C/W

AC Test Loads and Waveforms

Switching Characteristics Over the Operating Range^[6]

Parameter	Description	7C185D-10		7C185D-12		7C185D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
$t_{power}^{[5]}$	V_{CC} (typical) to the first access	100		100		100		μ s
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE1}	\overline{CE}_1 LOW to Data Valid		10		12		15	ns
t_{ACE2}	CE_2 HIGH to Data Valid		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5		6		8	ns
t_{LZOE}	\overline{OE} LOW to Low Z	3		3		3		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7]		5		6		7	ns
t_{LZCE1}	\overline{CE}_1 LOW to Low Z ^[8]	3		3		3		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		ns
t_{HZCE}	\overline{CE}_1 HIGH to High Z ^[7, 8] CE_2 LOW to High Z		5		6		7	ns
t_{PU}	\overline{CE}_1 LOW to Power-Up CE_2 to HIGH to Power-Up	0		0		0		ns
t_{PD}	\overline{CE}_1 HIGH to Power-Down CE_2 LOW to Power-Down		10		12		15	ns

Notes:

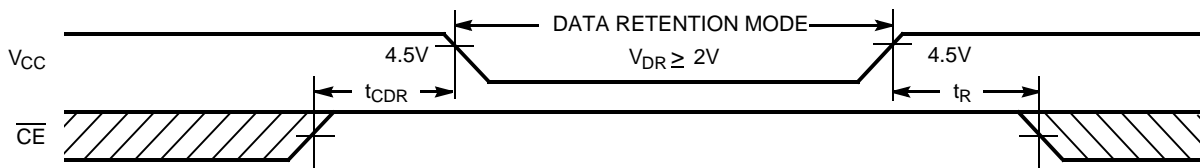
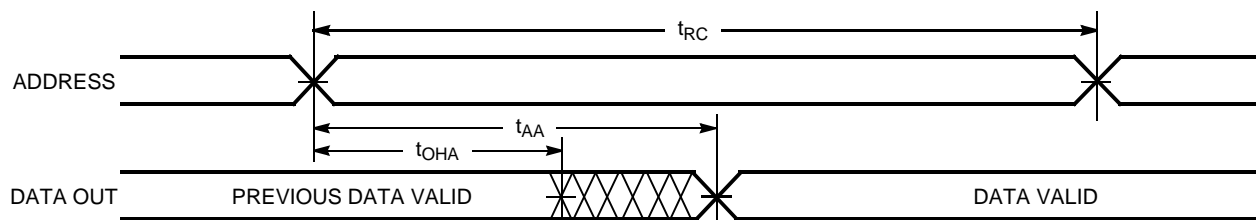
- t_{power} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE1} and t_{LZCE2} for any given device.

Switching Characteristics Over the Operating Range (continued)^[6]

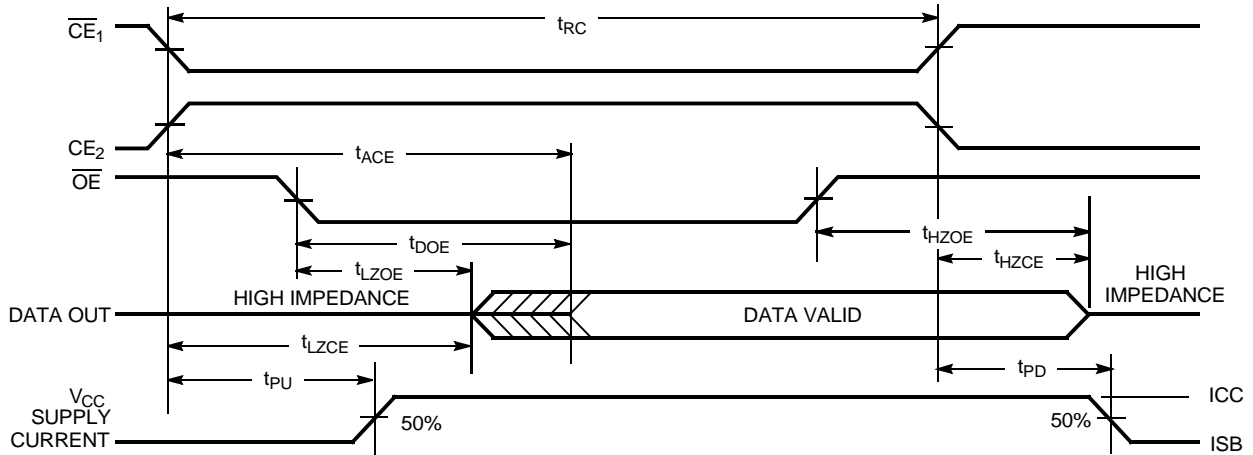
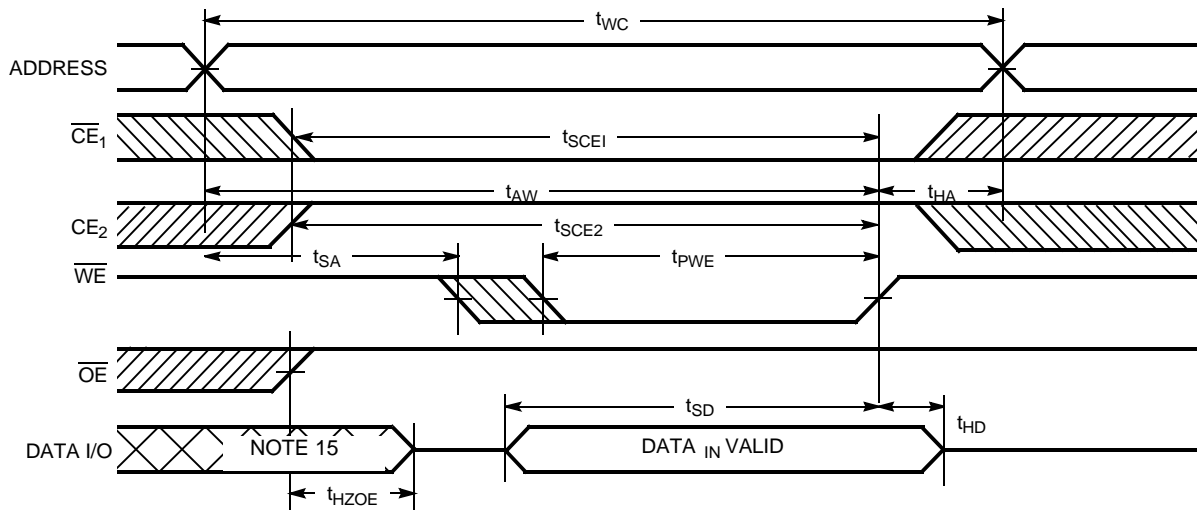
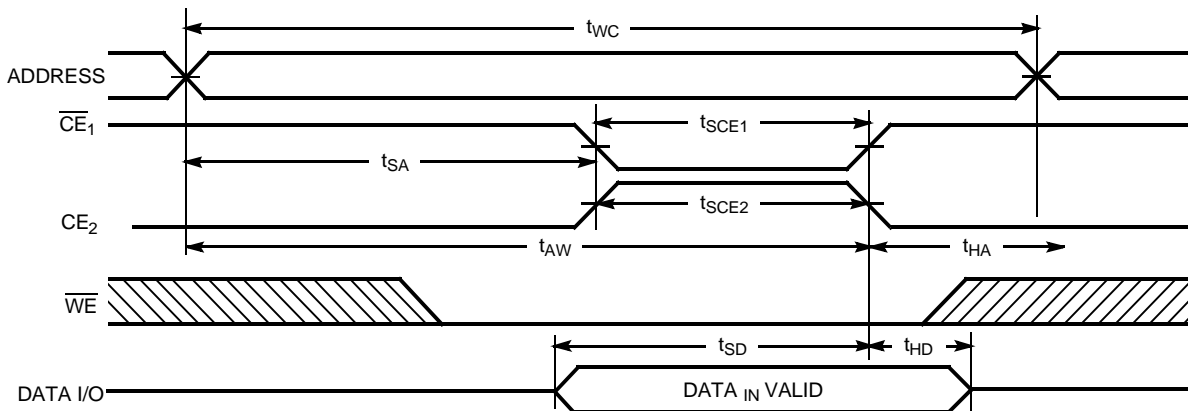
Parameter	Description	7C185D-10		7C185D-12		7C185D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle^[9]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE1}	\overline{CE}_1 LOW to Write End	8		10		12		ns
t_{SCE2}	CE_2 HIGH to Write End	8		10		12		ns
t_{AW}	Address Set-up to Write End	7		10		12		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	7		10		12		ns
t_{SD}	Data Set-up to Write End	6		7		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7]		6		6		7	ns
t_{LZWE}	\overline{WE} HIGH to Low Z	3		3		3		ns

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	Non-L, Com'l / Ind'l	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	3	mA
		L-Version Only		1.2	mA
t_{CDR} ^[4]	Chip Deselect to Data Retention Time		0		ns
t_R ^[10]	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

Switching Waveforms
Read Cycle No.1^[11,12]

Notes:

9. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. All 3 signals must be active to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50 \mu s$ or stable at $V_{CC(min.)} \geq 50 \mu s$.
11. Device is continuously selected. OE , $CE_1 = V_{IL}$. $CE_2 = V_{IH}$.
12. \overline{WE} is HIGH for read cycle.

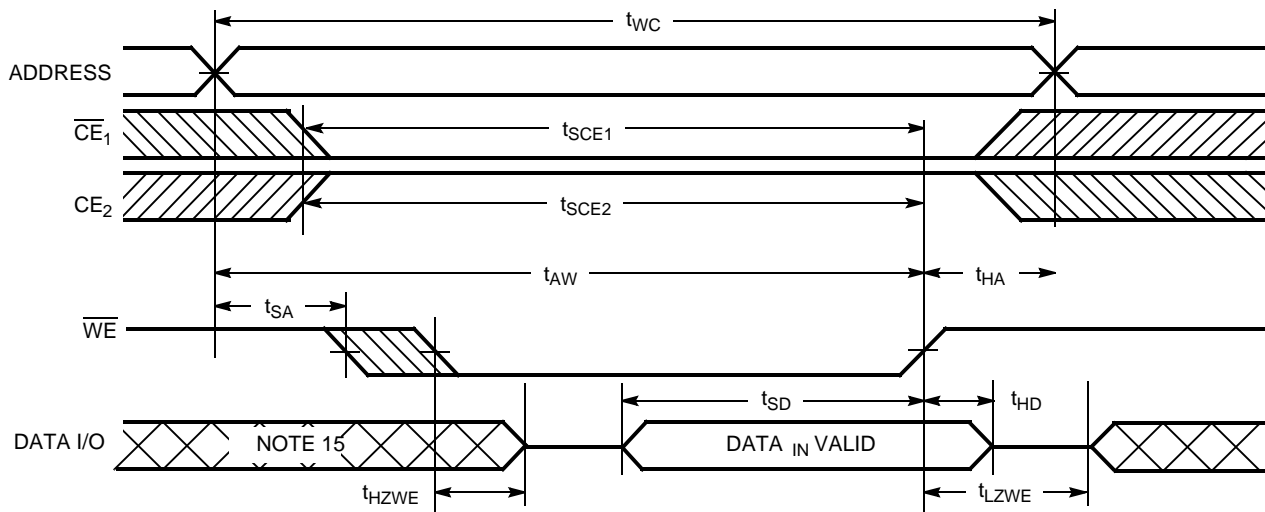
Switching Waveforms (continued)
Read Cycle No.2^[13,14]

Write Cycle No. 1 (WE Controlled)^[12,14]

Write Cycle No. 2 (CE Controlled)^[14,15,16]

Notes:

13. Data I/O is High Z if $\overline{OE} = V_{IH}$, $\overline{CE}_1 = V_{IH}$, $\overline{WE} = V_{IL}$, or $CE_2 = V_{IL}$.

14. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and CE_2 must be HIGH to initiate write. A write can be terminated by \overline{CE}_1 or \overline{WE} going HIGH or CE_2 going LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

15. During this period, the I/Os are in the output state and input signals should not be applied.

16. The minimum write cycle time for write cycle #3 (WE controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms (continued)
Write Cycle No. 3 (WE Controlled, OE LOW)^[14,15,16,17]

Truth Table

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-down
X	L	X	X	High Z	Deselect/Power-down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

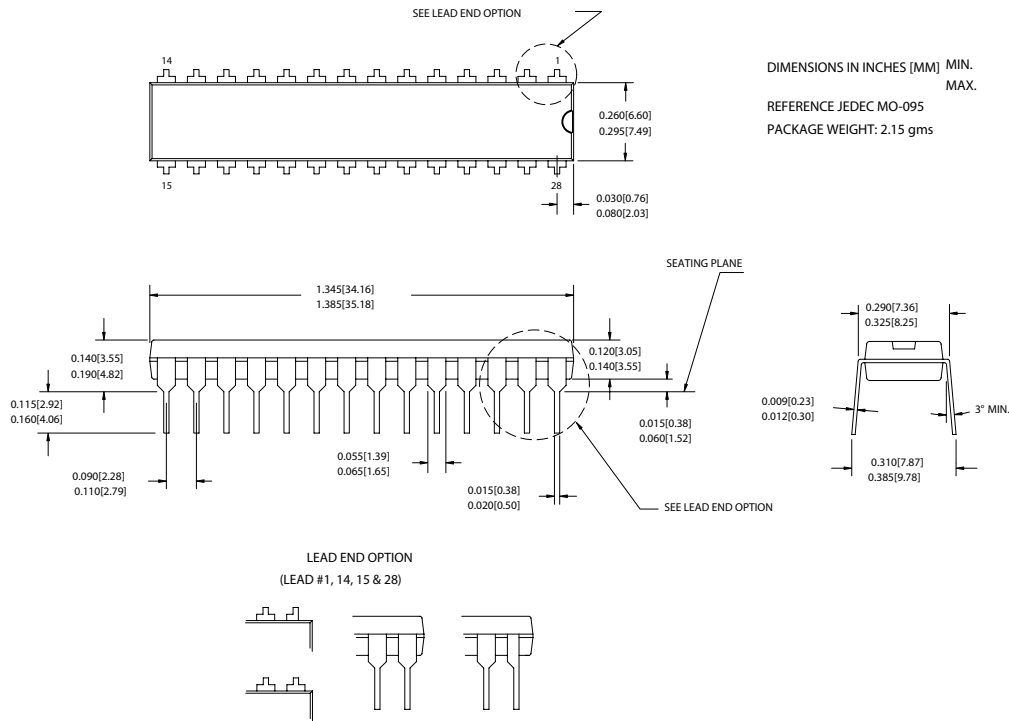
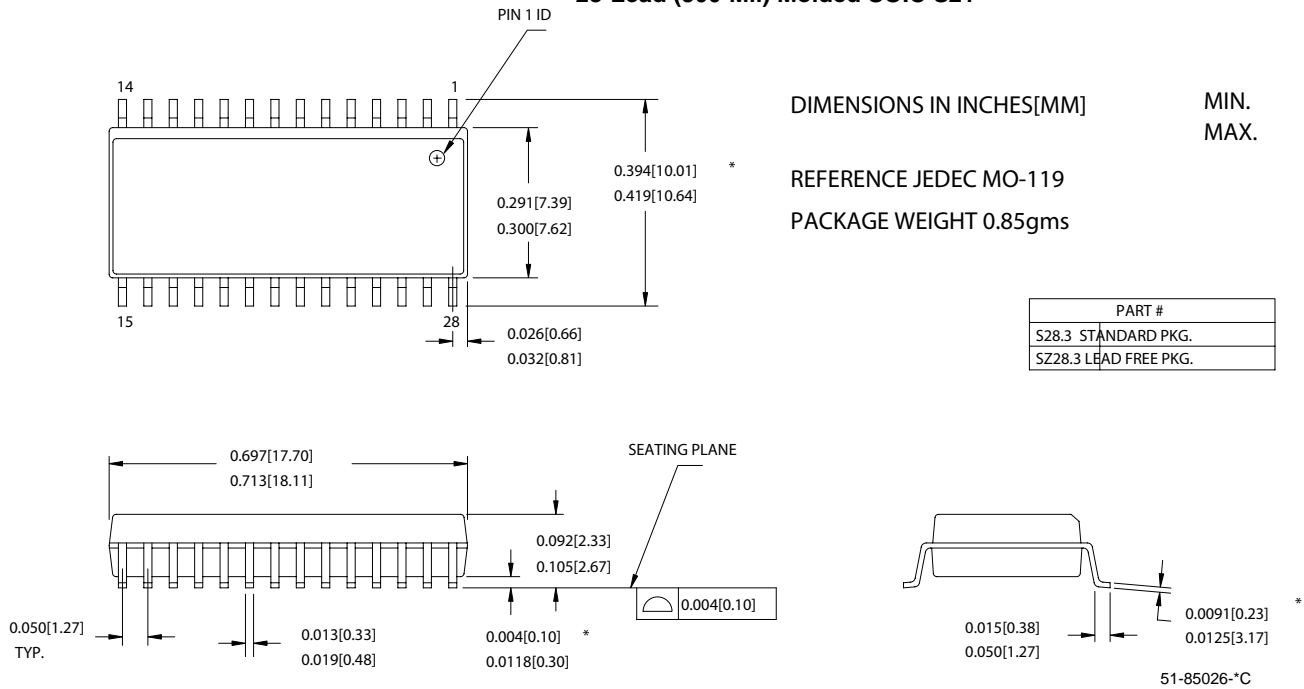
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C185D-10PXC	P21	28-Lead (300-Mil) Molded DIP (Pb-Free)	Commercial
	CY7C185D-10SXC	S21	28-Lead Molded SOIC (Pb-Free)	
	CY7C185D-10VXC	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C185D-10VXI	V21	28-Lead Molded SOJ (Pb-Free)	
12	CY7C185D-12PXC	P21	28-Lead (300-Mil) Molded DIP (Pb-Free)	Commercial
	CY7C185D-12SXC	S21	28-Lead Molded SOIC (Pb-Free)	
	CY7C185D-12VXC	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C185D-12VXI	V21	28-Lead Molded SOJ (Pb-Free)	
15	CY7C185D-15PXC	P21	28-Lead (300-Mil) Molded DIP (Pb-Free)	Commercial
	CY7C185D-15SXC	S21	28-Lead Molded SOIC (Pb-Free)	
	CY7C185D-15VXC	V21	28-Lead Molded SOJ (Pb-Free)	Industrial
	CY7C185D-15VXI	V21	28-Lead Molded SOJ (Pb-Free)	

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

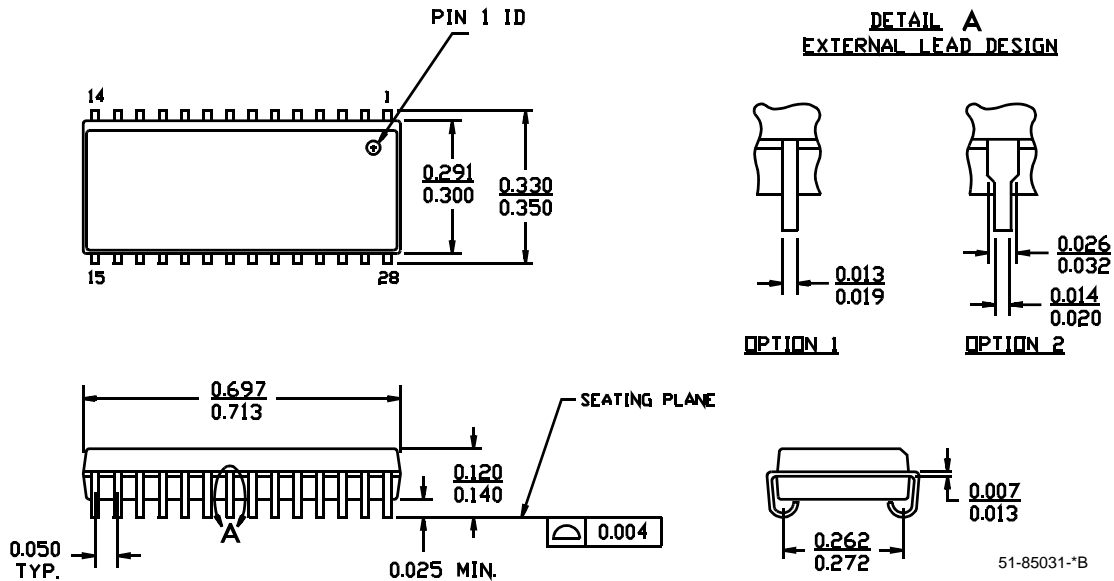
Note:

 17. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Package Diagrams
28-Lead (300-Mil) PDIP P21

28-Lead (300-Mil) Molded SOIC S21


Package Diagrams (continued)

28-Lead (300-Mil) Molded SOJ V21
 DIMENSIONS IN INCHES MIN.
MAX.



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Document History Page

Document Title: CY7C185D 64K (8K x 8) Static RAM (Preliminary)				
Document Number: 38-05466				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Datasheet for C9 IPP
*A	233715	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in Ordering Information
*B	262950	See ECN	RKF	Added T _{power} Spec in Switching Characteristics table Added Data Retention Characteristics table and waveforms Shaded Ordering Information
*C	307593	See ECN	RKF	1) Reduced Speed bins to -10, -12 and -15 ns 2) Added 'Industrial' grade parts to the Ordering Info on Page #6