REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Delete device class M references. - ro	12-11-28	C. SAFFLE

REV																				
SHEET																				
REV	A	A	A	A	A	A														
SHEET	15	16	17	18	19	20														
REV STATUS				REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
11-03-21

REVISION LEVEL
A

MICROCIRCUIT, LINEAR, RADIATION HARDENED, DUAL 2:1, WIDE BANDWIDTH, ACTIVE MULTIPLEXER, MONOLITHIC SILICON

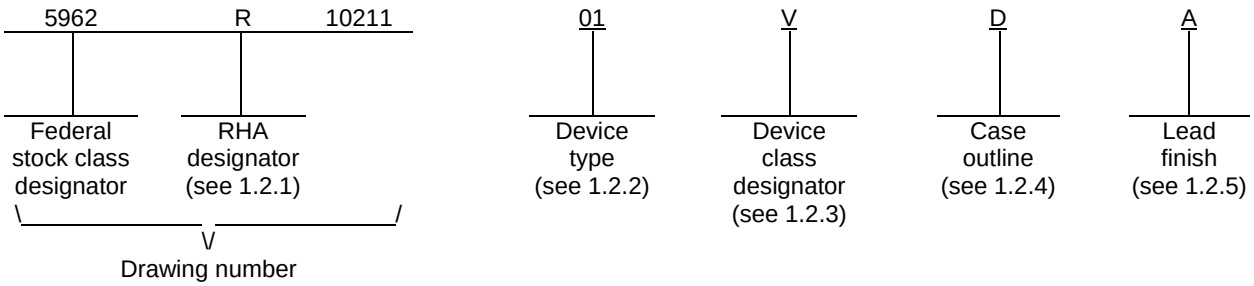
SIZE	CAGE CODE	
A	**67268**	**5962-10211**

SHEET 1 OF 20

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD8182	Radiation hardened, dual 2:1, wide bandwidth, active multiplexer
02	AD8182	Radiation hardened, dual 2:1, wide bandwidth, active multiplexer

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
D	GDFP1-F14	14	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage ($+V_S$ to $-V_S$) ..... 12.6 V
Input voltage (V_{IN}) ..... $\pm V_S$
Power dissipation (P_D) ..... 227 mW 2/
Junction temperature (T_J) ..... +175°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Storage temperature range ..... -65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 60°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 220°C/W 4/

1.4 Recommended operating conditions.

Supply voltages (symmetrical operation recommended): ($+V_S$) ..... +4 V to +6 V
($-V_S$) ..... -4 V to -6 V
Ambient operating temperature range (T_A) ..... -55°C to +125°C

1.4.1 Operating performance characteristics. T_A = +25°C.

Switching characteristics: R_L = 1 kΩ.
Channel switching time 50% logic to 10% output settling ..... 5 ns 5/
Channel switching time 50% logic to 90% output settling ..... 10 ns 5/
$\overline{\text{ENABLE}}$ to channel on time 50% logic to 90% output settling IN0 = +1 V, -1 V or IN1 = -1 V, +1 V ..... 10.5 ns 6/
$\overline{\text{ENABLE}}$ to channel off time 50% logic to 90% output settling IN0 = +1 V, -1 V or IN1 = -1 V, +1 V ..... 11 ns 6/

Distortion / noise performance:
Voltage noise, f = 10 kHz - 30 MHz, R_L = 2 kΩ ..... 4.5 nV / $\sqrt{\text{Hz}}$
Total harmonic distortion, f_C = 10 MHz, V_O =2 V_{PP}, R_L = 1 kΩ ..... -78 dBc

Output characteristics:
Disabled output capacitance ..... 1.9 pF

Input characteristics:
Disabled input capacitance ..... 1.7 pF
Enabled input capacitance ..... 1.7 pF

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum internal power dissipation is specified so that T_J does not exceed +175°C with T_A = +125°C. In product application, additional power dissipation created by output load current must not allow T_J to exceed +175°C with $T_A \leq$ +125°C.
3/ Measurement taken under absolute worst case condition. Data taken with thermal camera at highest power density location. See MIL-STD-1835 for average package thermal numbers.
4/ Measurement taken under absolute worst case conditions. Data taken with thermal camera at highest power density location.
5/ $\overline{\text{ENABLE}}$ pin is grounded. IN0 = +1 V dc, IN1 = -1 V dc. SELECT input is driven with 0 V to +5 V pulse. Measure transition time from 50% of the SELECT input value (+2.5 V) and 10% (or 90%) of the total output voltage transition from IN0 channel voltage (+1 V) to IN1 (-1 V), or vice versa. See figures 3 and 4.
6/ $\overline{\text{ENABLE}}$ pin is driven with 0 V to +5 V pulse (with 3 ns edges). State of SELECT input determines which channel is activated (for example, if SELECT = Logic 0, IN0 is selected). Set IN0 = +1 V dc, and measure transition time from 50% of $\overline{\text{ENABLE}}$ pulse (+2.5 V) to 90% of the total output voltage change. See figures 3 and 4.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
Device type 01 ..... 100 krads(Si) 7/
Maximum total dose available (dose rate ≤ 10 mrads(Si)/s):
Device type 02 ..... 50 krads(Si) 8/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections and block diagram. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

7/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.
8/ Device type 02 radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883 method 1019, condition D.

3.2.4 Timing diagrams. The timing diagrams shall be as specified on figures 3 and 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Digital inputs section.								
Logic “1’ voltage	V_{IH}	SELECT and $\overline{\text{ENABLE}}$ inputs		1,2,3	01,02	2.0		V
			M, D, P, L, R	1	01	2.0		
			M, D, P, L		02	2.0		
Logic “0’ voltage	V_{IL}	SELECT and $\overline{\text{ENABLE}}$ inputs		1,2,3	01,02		0.8	V
			M, D, P, L, R	1	01		0.8	
			M, D, P, L		02		0.8	
Logic “1” input current	I_{IH}	SELECT, $\overline{\text{ENABLE}}$ = +4 V		1,2,3	01,02		200	nA
			M, D, P, L, R	1	01		200	
			M, D, P, L		02		200	
Logic “0” input current	I_{IL}	SELECT, $\overline{\text{ENABLE}}$ = +0.4 V		1,2,3	01,02	-3		µA
			M, D, P, L, R	1	01	-3		
			M, D, P, L		02	-3		
DC transfer / Input characteristics section.								
Voltage gain 4/	Gain	$V_{IN} = \pm 1$ V, $R_L = 10$ kΩ		1,2,3	01,02	0.986		V/V
			M, D, P, L, R	1	01	0.986		
			M, D, P, L		02	0.986		
Input offset voltage	V_{OS}			1	01,02	-12	12	mV
				2,3		-15	15	
			M, D, P, L, R	1	01	-15	15	
			M, D, P, L		02	-15	15	
Input offset voltage matching	V_{OS} match	Channel to channel		1,2,3	01,02	-4	4	mV
			M, D, P, L, R	1	01	-8	8	
			M, D, P, L		02	-8	8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
DC transfer / Input characteristics section – continued.								
Input bias current	IBIAS			1	01,02	-5	5	µA
				2,3		-7	7	
			M, D, P, L, R	1	01	-5	5	
			M, D, P, L		02	-5	+5	
Input resistance	R_{IN}			1,2,3	01,02	1		MΩ
			M, D, P, L, R	1	01	1		
			M, D, P, L		02	1		
Output characteristics section.								
Output voltage swing 4/	V_{OUT4}	$+V_S$ = +4 V and $-V_S$ = -4 V,		1	01,02	2.0	-2.0	V
		$I_L = \pm 3.5$ mA		2		2.2	-2.2	
				3		1.8	-1.8	
			M, D, P, L, R	1	01	2.0	-2.0	
			M, D, P, L		02	2.0	-2.0	
	V_{OUT5}	$+V_S$ = +5 V and $-V_S$ = -5 V,		1	01,02	3.0	-3.0	
		$I_L = \pm 3.5$ mA		2		3.2	-3.2	
				3		2.8	-2.8	
			M, D, P, L, R	1	01	3.0	-3.0	
			M, D, P, L		02	3.0	-3.0	
	V_{OUT6}	$+V_S$ = +6 V and $-V_S$ = -6 V,		1	01,02	4.0	-4.0	
		$I_L = \pm 3.5$ mA		2		4.2	-4.2	
				3		3.8	-3.8	
			M, D, P, L, R	1	01	4.0	-4.0	
			M, D, P, L		02	4.0	-4.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output characteristics section – continued.								
Output resistance ON	R_{OUT-ON}			1,2,3	01,02		40	Ω
			M, D, P, L, R	1	01		40	
			M, D, P, L		02		40	
Output resistance OFF	$R_{OUT-OFF}$	$\overline{ENABLE}$ A = $\overline{ENABLE}$ B = 2.0 V		1,2,3	01,02	1		MΩ
			M, D, P, L, R	1	01	1		
			M, D, P, L		02	1		
Power supply rejection section.								
Power supply rejection ratio	+PSRR4	$+V_S$ = +3.5 V to +4.5 V, $-V_S$ = -4 V		1	01,02	54		dB
				2		52		
			M, D, P, L, R	1	01	54		
			M, D, P, L		02	54		
		$+V_S$ = +3.8 V to +4.8 V, $-V_S$ = -4 V		3	01,02	54		
	-PSRR4	$-V_S$ = -3.5 V to -4.5 V, $+V_S$ = +4 V		1,2,3	01,02	45		
			M, D, P, L, R	1	01	45		
			M, D, P, L		02	45		
	+PSRR5	$+V_S$ = +4.5 V to +5.5 V, $-V_S$ = -5 V		1,3	01,02	54		
				2		52		
			M, D, P, L, R	1	01	54		
			M, D, P, L		02	54		
	-PSRR5	$-V_S$ = -4.5 V to -5.5 V, $+V_S$ = +5 V		1,2,3	01,02	45		
			M, D, P, L, R	1	01	45		
			M, D, P, L		02	45		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power supply rejection section – continued.								
Power supply rejection ratio	+PSRR6	$+V_S$ = +5.5 V to +6.5 V,		1,3	01,02	54		dB
		$-V_S$ = -6 V		2		52		
			M, D, P, L, R	1	01	54		
			M, D, P, L		02	54		
	-PSRR6	$-V_S$ = -6.5 V to -6.5 V,		1,2,3	01,02	45		
		$+V_S$ = +6 V	M, D, P, L, R	1	01	45		
			M, D, P, L		02	45		
Power supply current section.								
Quiescent current (All channels "ON")	$+IS_{ON}$	$\overline{ENABLE}$ A = $\overline{ENABLE}$ B = 0.8 V, SELECT A = SELECT B = 0.8 V, IN0 A = IN1 A = 0 V, IN0 B = IN1 B = 0 V		1	01,02		8	mA
				2,3			8.5	
			M, D, P, L, R	1	01		8	
			M, D, P, L		02		8	
	$-IS_{ON}$	$\overline{ENABLE}$ A = $\overline{ENABLE}$ B = 0.8 V, SELECT A = SELECT B = 0.8 V, IN0 A = IN1 A = 0 V, IN0 B = IN1 B = 0 V		1	01,02	-8		
				2,3		-8.5		
			M, D, P, L, R	1	01	-8		
			M, D, P, L		02	-8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current section.							
Quiescent current (All channels "OFF")	$+IS_{OFF}$	$\overline{ENABLE}$ A = $\overline{ENABLE}$ B = 2 V, SELECT A = SELECT B = 0.8 V, IN0 A = IN1 A = 0 V, IN0 B = IN1 B = 0 V	1,2,3	01,02		3	mA
		M, D, P, L, R	1	01		3	
		M, D, P, L		02		3	
	$-IS_{OFF}$	$\overline{ENABLE}$ A = $\overline{ENABLE}$ B = 2 V, SELECT A = SELECT B = 0.8 V, IN0 A = IN1 A = 0 V, IN0 B = IN1 B = 0 V	1,2,3	01,02	-3		
		M, D, P, L, R	1	01	-3		
		M, D, P, L		02	-3		
Dynamic performance section. 5/ 6/							
Settling time to 7/ 0.2 %	t_S	1 V step: -1 V to 0 V and +1 V to 0 V	9,10,11	01,02		14	ns
Slew rate	SR	2 V step: +1 V to -1 V and -1 V to +1 V	4	01,02	650		V/µs
			5,6		550		
-3 dB large signal bandwidth	BW_{-3dB}	V_{IN} = 0.5 Vrms	4,5,6	01,02	110		MHz
0.1 dB large signal bandwidth	$BW_{0.1dB}$	V_{IN} = 0.5 Vrms	4,5,6	01,02	40		MHz
Distortion / noise performance section. 5/ 6/							
All hostile crosstalk 8/	$XTLK_{5MHz}$	f = 5 MHz, RL = 1 kΩ, V_{IN} = 0.707 Vrms	4	01,02		-71	dB
			5			-69	
			6			-70	
	$XTLK_{30MHz}$	f = 30 MHz, RL = 1 kΩ, V_{IN} = 0.707 Vrms	4,6			-55	
			5			-54	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Distortion / noise performance section – continued. 5/ 6/							
OFF isolation	$ISOdis_{5MHz}$	f = 5 MHz, R_L = 30 Ω, V_{IN} = 0.446 Vrms, $\overline{ENABLE}$ A = $\overline{ENABLE}$ B > 2 V	4	01,02		-96	dB
			5			-89	
			6			-91	
	$ISOdis_{30MHz}$	f = 5 MHz, R_L = 30 Ω, V_{IN} = 0.446 Vrms, $\overline{ENABLE}$ A = $\overline{ENABLE}$ B > 2 V	4			-80	
			5			-77	
			6			-79	
	ISO_{5MHz}	f = 5 MHz, R_L = 30 Ω, V_{IN} = 0.446 Vrms, $\overline{ENABLE}$ A > 2 V, $\overline{ENABLE}$ B < 0.8 V; $\overline{ENABLE}$ A < 0.8 V, $\overline{ENABLE}$ B > 2 V	4,5,6			-87	
	ISO_{30MHz}	f = 30 MHz, R_L = 30 Ω, V_{IN} = 0.446 Vrms, $\overline{ENABLE}$ A > 2 V, $\overline{ENABLE}$ B < 0.8 V; $\overline{ENABLE}$ A < 0.8 V, $\overline{ENABLE}$ B > 2 V	4,5,6			-72	

1/ Device type 01 supplied to this drawing has been characterized through all levels P, L, and R of irradiation. Device type 02 supplied to this drawing has been characterized through levels P and L of irradiation. However, device type 01, is only tested at the "R" level and device type 02 is only tested at the "L" level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Device type 01 may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A for device type 01 and condition D for device type 02. Device type 02 is tested at low dose rate.

3/ Unless otherwise specified, R_L = 2 kΩ, $\overline{ENABLE}$ A = $\overline{ENABLE}$ B = 0.8 V, $+V_S$ = +4 V and $-V_S$ = -4 V; $+V_S$ = +5 V and $-V_S$ = -5 V; $+V_S$ = +6 V and $-V_S$ = -6 V. Refer to section 6.7 for detailed application notes.

4/ Larger values of R_L provide wider output voltage swings, as well as better gain accuracy.

5/ Subgroups 4, 5, 6, 9, 10, and 11 are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

6/ Not tested post irradiation.

7/ $+V_S$ = +5 V and $-V_S$ = -5 V.

8/ XTLK measured on both inputs of each mux with the other mux in all four possible states of $\overline{ENABLE}$ and SELECT.

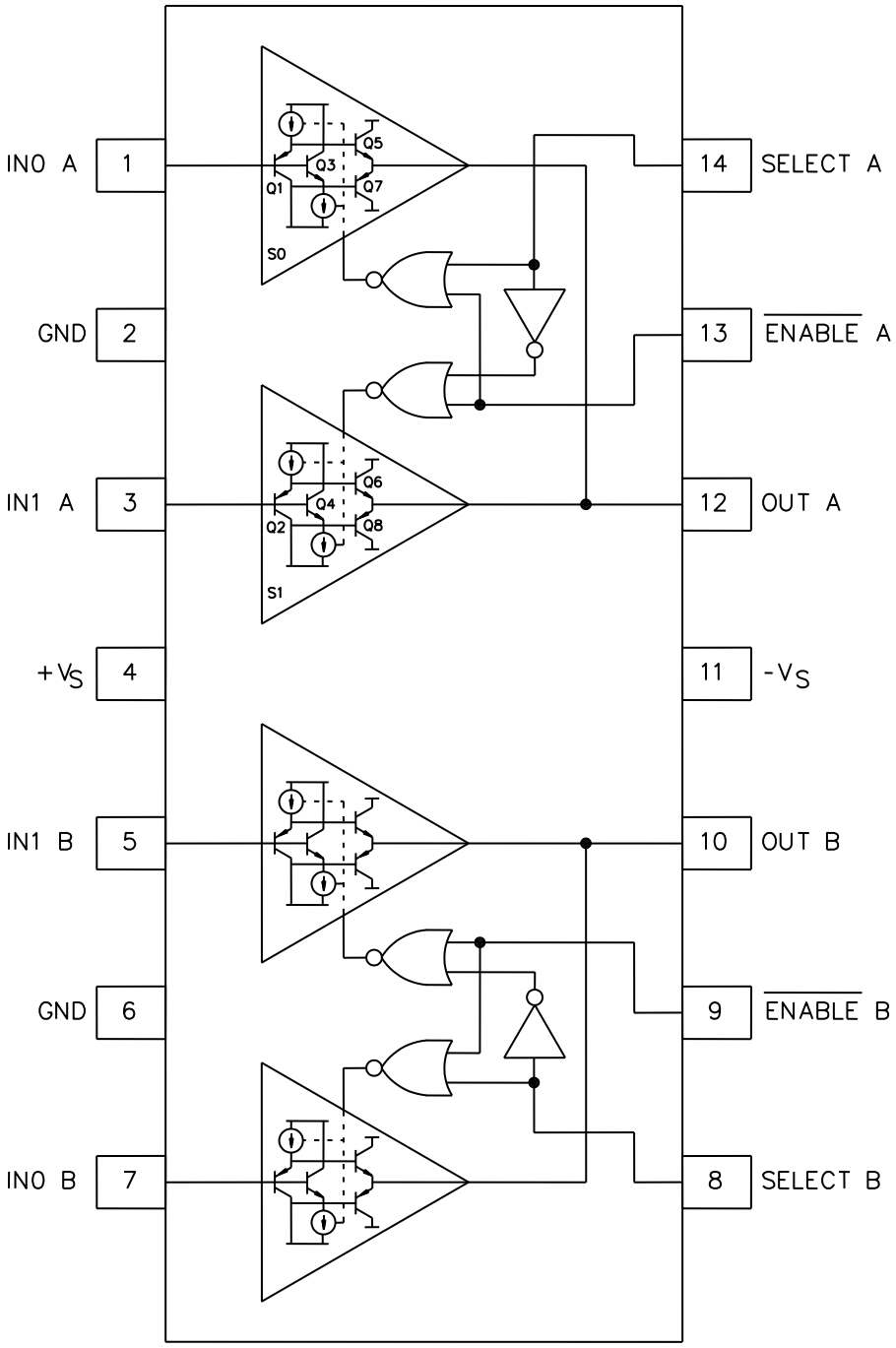


FIGURE 1. Terminal connections and block diagram.

Terminal symbol	Description
IN0	One of two inputs to each multiplexer.
GND	Analog, digital, and power ground.
IN1	One of two inputs to each multiplexer.
$+V_S$	Positive power supply.
$-V_S$	Negative power supply.
OUT	Multiplexer output.
$\overline{\text{ENABLE}}$	Enables multiplexer output when logic low. Multiplexer output is high impedance when logic high.
SELECT	Selects IN0 to multiplexer output when logic low. Selects IN1 to multiplexer output when logic high.

FIGURE 1. Terminal connections and block diagram - continued.

SELECT	$\overline{\text{ENABLE}}$	OUTPUT
0	0	IN0
1	0	IN1
0	1	High Z
1	1	High Z

FIGURE 2. Truth table.

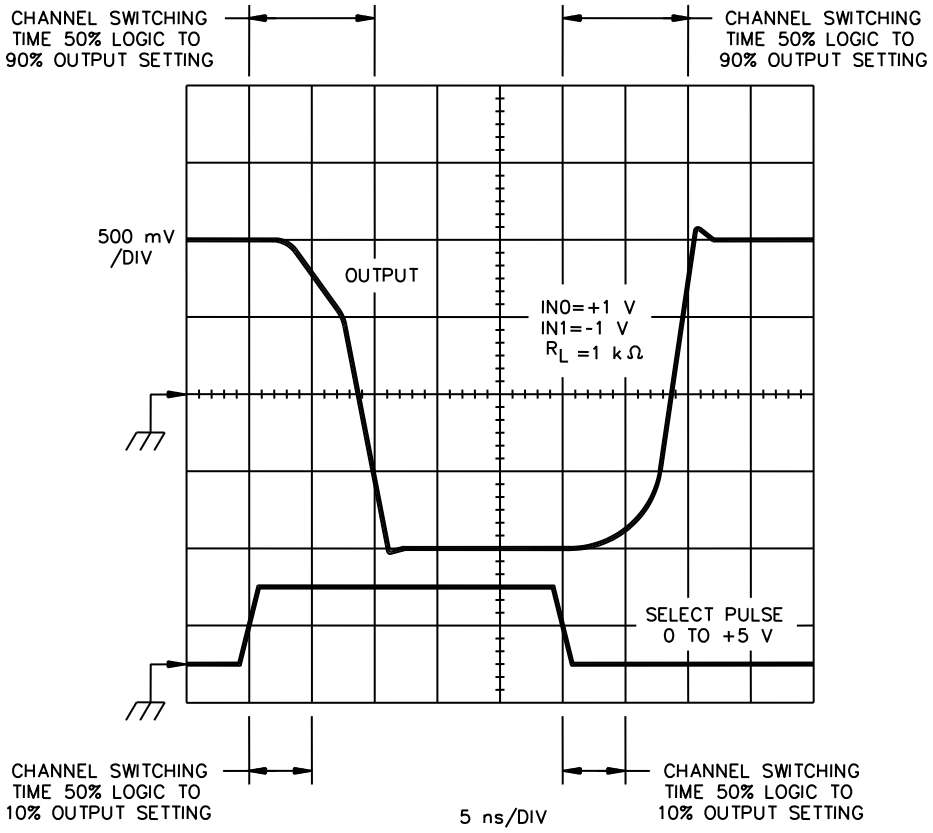


FIGURE 3. SELECT timing diagram.

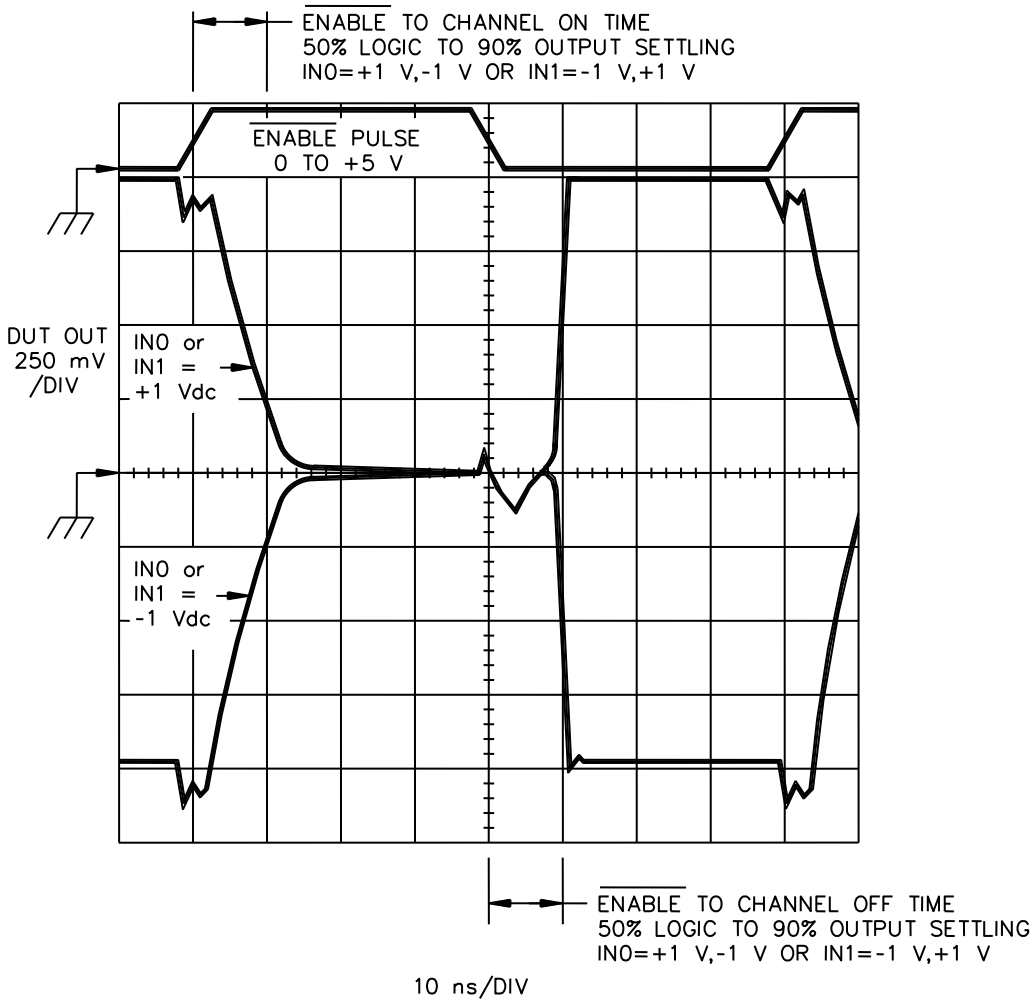


FIGURE 4. $\overline{\text{ENABLE}}$ timing diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 4, 5, 6, 9, 10, and 11 are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3,4, 1/ 2/ 5,6,9,10,11	1,2,3, 1/ 2/ 3/ 4,5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6, 2/ 9,10,11	1,2,3,4,5,6, 2/ 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3, 2/ 3/ 4,5,6,9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1.
2/ Subgroups 4, 5, 6, 9, 10, and 11 are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous interim electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/ 3/

Parameters	Symbol	Delta limits		Units
		Min	Max	
Quiescent current all channels “ON”	$+IS_{ON}$	-0.7	0.7	mA
Quiescent current all channels “ON”	$-IS_{ON}$	-0.7	0.7	mA
Quiescent current all channels “OFF”	$+IS_{OFF}$	-0.4	0.4	mA
Quiescent current all channels “OFF”	$-IS_{OFF}$	-0.4	0.4	mA
Input offset voltage	V_{OS}	-2.0	2.0	mV
Input bias current	I_{BIAS}	-1.0	1.0	µA

1/ Deltas are performed at room temperature.
2/ 240 hour burn-in and 1,000 hour operating group C life test.
3/ $+V_S$ = +4 V and $-V_S$ = -4 V; $+V_S$ = +5 V and $-V_S$ = -5 V; $+V_S$ = +6 V and $-V_S$ = -6 V.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 01 and condition D for device type 02 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Application notes.

Theory of operation

The active multiplexer is designed for fast-switching and wide bandwidth. This performance is attained with low power dissipation (3.8 mA per active channel) through the use of proprietary circuit techniques and a dielectrically-isolated complementary bipolar process. This device has a fast disable function that allows the outputs of several muxes to be wired in parallel to form a larger mux with little degradation in switching time. The low disabled output capacitance of these muxes helps to preserve the system bandwidth in larger matrices. Unlike earlier complementary metal oxide semiconductor (CMOS) switches, the switched open loop architecture of the device provides a unidirectional signal path with minimal switching glitches and constant, low input capacitance. Since the input impedance of these muxes is nearly independent of the load impedance and the state of the mux, the frequency response of the ON channels in a large switch matrix is not affected by fanout.

Figure 1 shows a block diagram and simplified schematic of the device, which contains two muxes, each of which contains two switched buffers (S0 and S1) that share a common output. The decoder logic translates transistor-transistor logic (TTL) - compatible logic inputs (SELECT and $\overline{\text{ENABLE}}$) to internal, differential emitter coupled logic (ECL) levels for fast, low-glitch switching. The SELECT input determines which of the two buffers is enabled, unless the $\overline{\text{ENABLE}}$ input is high, in which case both buffers are disabled and the output is switched to a high impedance state.

Each open-loop buffer is implemented as a complementary emitter follower that provides high input impedance, symmetric slew rate and load drive, and high output-to-input isolation due to its beta squared (β^2) current gain. The selected buffer is biased ON by fast switched current sources that allow the buffer to turn on quickly. Dedicated flatness circuits, combined with the open-loop architecture of the device, keep peaking low (normally $<$ 1 dB) when driving high capacitive loads, without the need for external series resistors at the input or output. If better flatness response is desired, an input series resistance (R_S) may be used, although this will increase crosstalk. The dc gain of the device is almost independent of load for $R_L > 10\ k\Omega$. For heavier loads, the dc gain is approximately that of the voltage divider formed by the output impedance of the mux (normally 27 Ω) and R_L.

High speed disable clamps circuits at the bases of Q5-Q8 (not shown in figure 1) allow the buffers to turn off quickly and cleanly without dissipating much power once off. Moreover, these clamps shunt displacement currents flowing through the junction capacitances of Q1-Q4 away from the bases of Q5-Q8 and to ac ground through low impedances. The two-pole high pass frequency response of the T switch formed by these clamps is a significant improvement over the one-pole high pass response of a simple series CMOS switch. As a result, board and package parasitics, especially stray capacitance between inputs and outputs may limit the achievable crosstalk and isolation.

6.7 Application notes - continued.

Layout considerations

Realizing the high speed performance attainable with the device requires careful attention to board layout and component selection. Proper radio frequency (RF) design techniques and low parasitic component selection are mandatory.

Wire wrap boards, prototype boards, and sockets are not recommended because of their high parasitic inductance and capacitance. Instead, surface mount components should be soldered directly to a printed circuit board (PCB). The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input and output pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing. One end of the capacitor should be connected to the ground plane and the other end within a 1/4 inch of each power pin. An additional large (4.7 µF – 10 µF) tantalum capacitor should be connected in parallel with each of the smaller capacitors for low impedance supply bypassing over a broad range of frequencies.

Signal traces should be as short as possible. Stripline or microstrip techniques should be used for long signal traces (longer than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end using surface mount components.

Careful layout is imperative to minimize crosstalk. Guards (ground or supply traces) must be run between all signal traces to limit direct capacitive coupling. Input and output signal lines should fan out away from the mux as much as possible. If multiple signal layers are available, a buried stripline structure having ground plane above, below, and between signal traces will have the best crosstalk performance.

Return currents flowing through termination resistors can also increase crosstalk if these currents flow in sections of the finite-impedance ground circuit that is shared between more than one input or output. Minimizing the inductance and resistance of the ground plane can reduce this effect, but further care should be taken in positioning the terminations. Terminating cables directly at the connectors will minimize the return current flowing on the board, but the signal trace between the connector and the mux will look like an open stub and will degrade the frequency response. Moving the termination resistors close to the input pins will improve the frequency response, but the terminations from the neighboring inputs should not have a common ground return.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-11-28

Approved sources of supply for SMD 5962-10211 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1021101VDA	24355	AD8182AM/QMLR
5962L1021102VDA	24355	AD8182AM/QMLL

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605

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