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# 16-Mbit (1M × 16) Static RAM

## Features

- High speed
  - $t_{AA} = 10$  ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active power
  - $I_{CC} = 90$  mA typical
- Low CMOS standby power
  - $I_{SB2} = 20$  mA typical
- Operating voltages of  $3.3 \pm 0.3$  V
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 54-pin TSOP II package

## Functional Description

The CY7C10612G and CY7C10612GE are high performance CMOS fast static RAM devices with embedded ECC. These devices are offered in single chip enable option. The CY7C10612GE device includes an error indication pin that signals an error-detection and correction event during a read cycle.

To write to the device, take Chip Enables ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See [Truth Table on page 14](#) for a complete description of Read and Write modes.

The input or output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

On the CY7C10612GE devices the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = high). See the [Truth Table on page 14](#) for a complete description of read and write modes.

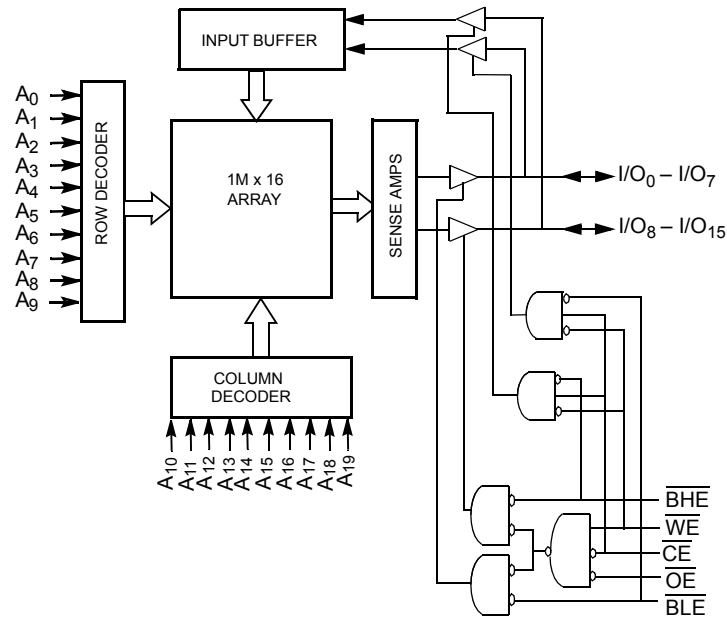
The CY7C10612G and CY7C10612GE are available in a 54-pin TSOP II package.

For a complete list of related documentation, click [here](#).

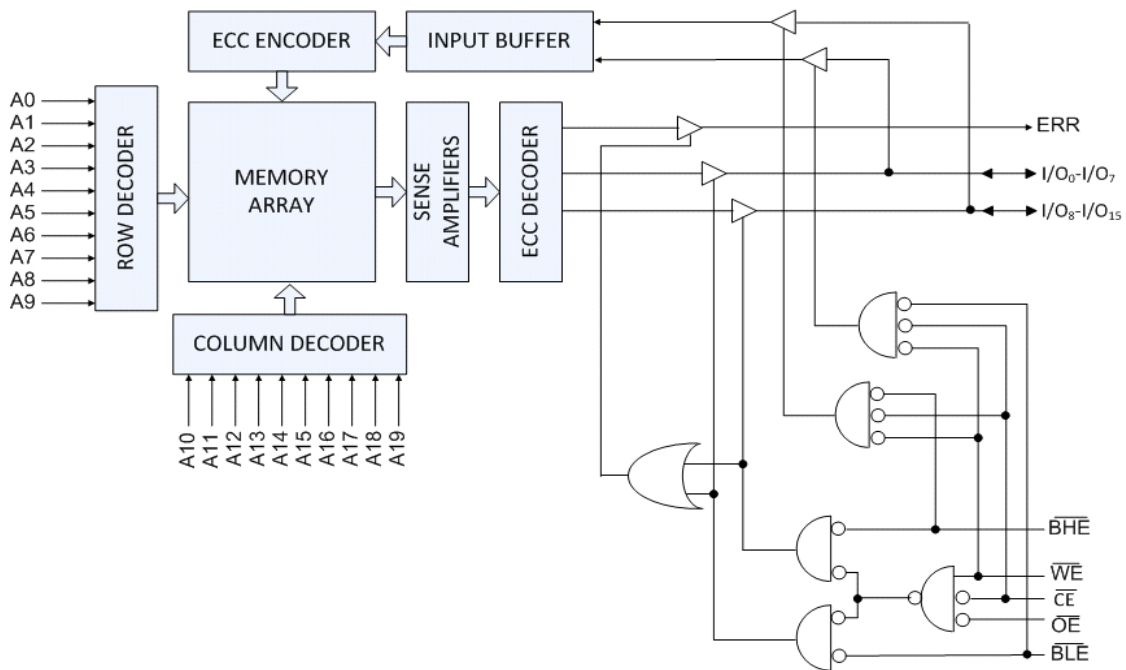
## Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	110	mA
Maximum CMOS Standby Current	30	mA

**Logic Block Diagram – CY7C10612G**



**Logic Block Diagram – CY7C10612GE**

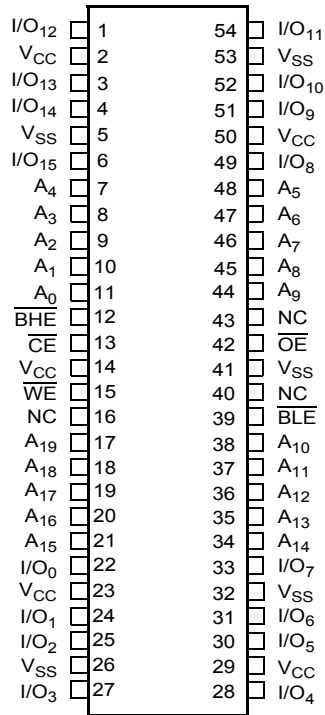


## Contents

<b>Pin Configurations</b> .....	<b>4</b>	<b>Ordering Information</b> .....	<b>15</b>
<b>Maximum Ratings</b> .....	<b>6</b>	Ordering Code Definitions .....	15
<b>Operating Range</b> .....	<b>6</b>	<b>Package Diagrams</b> .....	<b>16</b>
<b>DC Electrical Characteristics</b> .....	<b>6</b>	<b>Acronyms</b> .....	<b>17</b>
<b>Capacitance</b> .....	<b>7</b>	<b>Document Conventions</b> .....	<b>17</b>
<b>Thermal Resistance</b> .....	<b>7</b>	Units of Measure .....	17
<b>AC Test Loads and Waveforms</b> .....	<b>7</b>	<b>Document History Page</b> .....	<b>18</b>
<b>Data Retention Characteristics</b> .....	<b>8</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>19</b>
<b>Data Retention Waveform</b> .....	<b>8</b>	Worldwide Sales and Design Support .....	19
<b>AC Switching Characteristics</b> .....	<b>9</b>	Products .....	19
<b>Switching Waveforms</b> .....	<b>10</b>	PSoC® Solutions .....	19
<b>Truth Table</b> .....	<b>14</b>	Cypress Developer Community .....	19
<b>ERR Output – CY7C10612GE</b> .....	<b>14</b>	Technical Support .....	19

## Pin Configurations

**Figure 1. 54-pin TSOP II pinout (Top View) <sup>[1]</sup>**  
**CY7C10612G**



**Note**

1. NC pins are not connected on the die.

**Pin Configurations** (continued)

**Figure 2. 54-pin TSOP II pinout with ERR (Top View)** [2, 3]  
**CY7C10612GE**

I/O <sub>12</sub>	1	54	I/O <sub>11</sub>
V <sub>CC</sub>	2	53	V <sub>SS</sub>
I/O <sub>13</sub>	3	52	I/O <sub>10</sub>
I/O <sub>14</sub>	4	51	I/O <sub>9</sub>
V <sub>SS</sub>	5	50	V <sub>CC</sub>
I/O <sub>15</sub>	6	49	I/O <sub>8</sub>
A <sub>4</sub>	7	48	A <sub>5</sub>
A <sub>3</sub>	8	47	A <sub>6</sub>
A <sub>2</sub>	9	46	A <sub>7</sub>
A <sub>1</sub>	10	45	A <sub>8</sub>
A <sub>0</sub>	11	44	A <sub>9</sub>
$\overline{\text{BHE}}$	12	43	ERR
$\overline{\text{CE}}$	13	42	$\overline{\text{OE}}$
V <sub>CC</sub>	14	41	V <sub>SS</sub>
$\overline{\text{WE}}$	15	40	NC
NC	16	39	$\overline{\text{BLE}}$
A <sub>19</sub>	17	38	A <sub>10</sub>
A <sub>18</sub>	18	37	A <sub>11</sub>
A <sub>17</sub>	19	36	A <sub>12</sub>
A <sub>16</sub>	20	35	A <sub>13</sub>
A <sub>15</sub>	21	34	A <sub>14</sub>
I/O <sub>0</sub>	22	33	I/O <sub>7</sub>
V <sub>CC</sub>	23	32	V <sub>SS</sub>
I/O <sub>1</sub>	24	31	I/O <sub>6</sub>
I/O <sub>2</sub>	25	30	I/O <sub>5</sub>
V <sub>SS</sub>	26	29	V <sub>CC</sub>
I/O <sub>3</sub>	27	28	I/O <sub>4</sub>

**Note**

2. NC pins are not connected on the die.
3. ERR is an Output pin. If not used, this pin should be left floating.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....	-65 °C to +150 °C
Ambient Temperature with Power Applied .....	-55 °C to +125 °C
Supply Voltage on $V_{CC}$ Relative to GND <sup>[4]</sup> .....	-0.5 V to $V_{CC} + 0.5$ V
DC Voltage Applied to Outputs in High Z State <sup>[4]</sup> .....	-0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage <sup>[4]</sup> .....	-0.5 V to $V_{CC} + 0.5$ V
Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015) .....	> 2001 V
Latch Up Current .....	> 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

## DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns			Unit	
			Min	Typ <sup>[5]</sup>	Max		
$V_{OH}$	Output HIGH Voltage	2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.2	-	-	V
		2.7 V to 3.0 V	$V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.4	-	-	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min}, I_{OL} = 8$ mA	-	-	0.4	V	
$V_{IH}$ <sup>[4]</sup>	Input HIGH Voltage	-	2.0	-	$V_{CC} + 0.3$	V	
$V_{IL}$ <sup>[4]</sup>	Input LOW Voltage	-	-0.3	-	0.8	V	
$I_{IX}$	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	-1.0	-	+1.0	μA	
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1.0	-	+1.0	μA	
$I_{CC}$	Operating Supply Current	$V_{CC} = \text{Max}, I_{OUT} = 0$ mA, CMOS levels	f = 100 MHz	-	90.0	110.0	mA
			f = 66.7 MHz	-	70.0	80.0	
$I_{SB1}$	Automatic CE Power-down Current – TTL Inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ <sup>[5]</sup> , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , f = $f_{MAX}$	-	-	40.0	mA	
$I_{SB2}$	Automatic CE Power-down Current – CMOS Inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.2$ V <sup>[5]</sup> , $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0	-	20.0	30.0	mA	

### Notes

- $V_{IL(\text{min})} = -2.0$  V and  $V_{IH(\text{max})} = V_{CC} + 2$  V for pulse durations of less than 20 ns.
- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8$  V (for a  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3$  V (for a  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC} = 5$  V (for a  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25$  °C.

### Capacitance

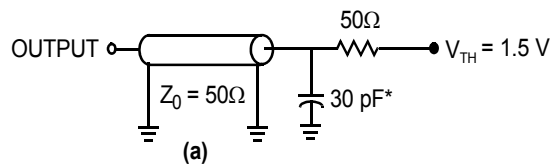
Parameter [6]	Description	Test Conditions	54-pin TSOP II	Unit
$C_{IN}$	Input Capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$	10	pF
$C_{OUT}$	I/O Capacitance			

### Thermal Resistance

Parameter [6]	Description	Test Conditions	54-pin TSOP II	Unit
$\Theta_{JA}$	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	93.63	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (junction to case)		21.58	

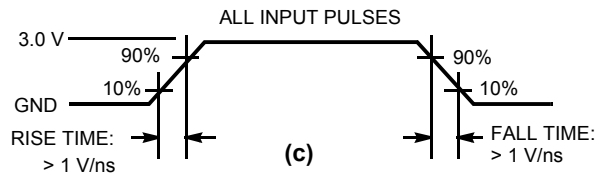
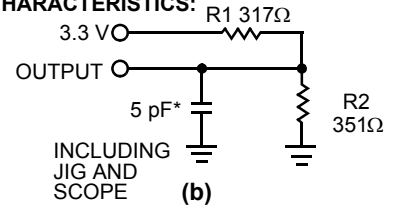
### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [7]



\* CAPACITIVE LOAD CONSISTS OF ALL COMPONENTS OF THE TEST ENVIRONMENT

HIGH Z CHARACTERISTICS:



**Notes**

6. Tested initially and after any design or process changes that may affect these parameters.
7. Full-device AC operation assumes a 100- $\mu\text{s}$  ramp time from 0 to  $V_{CC}$  (min) and 100- $\mu\text{s}$  wait time after  $V_{CC}$  stabilizes to its operational value.



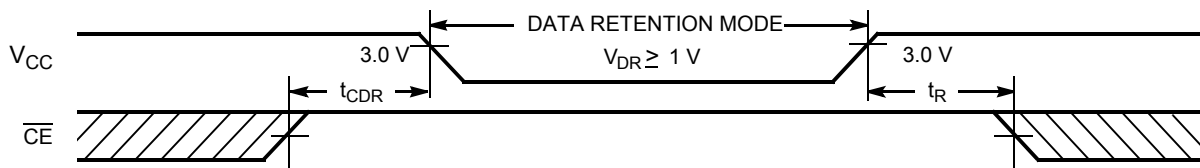
## Data Retention Characteristics

Over the Operating Range  $-45\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Typ <sup>[8]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	–	1.0	–	–	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 2\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	30.0	mA
$t_{CDR}^{[9]}$	Chip Deselect to Data Retention Time	–	0.0	–	–	ns
$t_R^{[9, 10]}$	Operation Recovery Time	–	10.0	–	–	ns

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ})}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ .
9. This parameter is guaranteed by design and is not tested.
10. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min.})} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(\text{min.})} \geq 100\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Over the Operating Range

Parameter <sup>[11]</sup>	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{POWER}$	$V_{CC}$ to the first access <sup>[12]</sup>	100.0	–	$\mu$ s
$t_{RC}$	Read cycle time	10.0	–	ns
$t_{AA}$	Address to data valid	–	10.0	ns
$t_{OHA}$	Data hold from address change	3.0	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	10.0	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	5.0	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[13, 14, 15]</sup>	0.0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[13, 14, 15]</sup>	–	5.0	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[13, 14, 15]</sup>	3.0	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[13, 14, 15]</sup>	–	5.0	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up <sup>[16]</sup>	0.0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down <sup>[16]</sup>	–	10.0	ns
$t_{DBE}$	Byte enable to data valid	–	5.0	ns
$t_{LZBE}$	Byte enable to low Z	1.0	–	ns
$t_{HZBE}$	Byte disable to high Z	–	6.0	ns
<b>Write Cycle <sup>[17, 18]</sup></b>				
$t_{WC}$	Write cycle time	10.0	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	7.0	–	ns
$t_{AW}$	Address setup to write end	7.0	–	ns
$t_{HA}$	Address hold from write end	0.0	–	ns
$t_{SA}$	Address setup to write start	0.0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7.0	–	ns
$t_{SD}$	Data setup to write end	5.0	–	ns
$t_{HD}$	Data hold from write end	0.0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[13, 14, 15]</sup>	3.0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[13, 14, 15]</sup>	–	5.0	ns
$t_{BW}$	Byte enable to end of write	7.0	–	ns

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of Figure 3 on page 7, unless specified otherwise.
- $t_{POWER}$  gives the minimum amount of time that the power supply is at typical  $V_{CC}$  values until the first memory access is performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ , and  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 7. Transition is measured  $\pm 200$  mV from steady state voltage.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
- Tested initially and after any design or process changes that may affect these parameters.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . Chip enable must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) for CY7C10612G [19, 20]

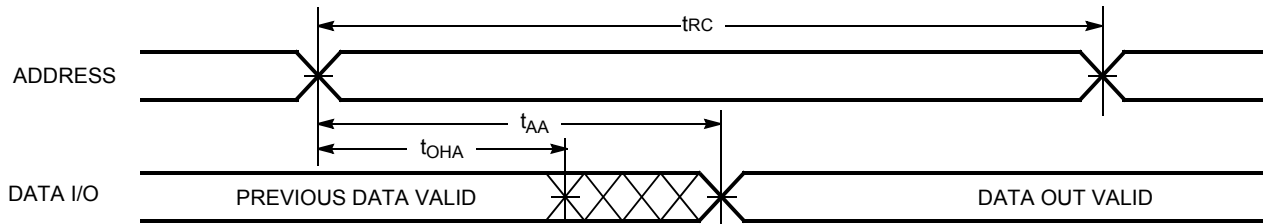
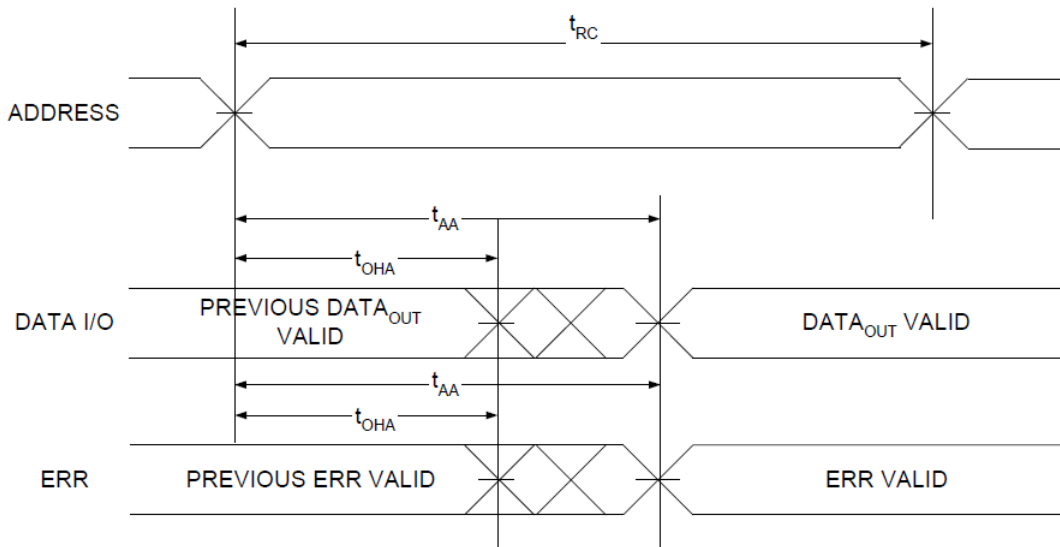


Figure 6. Read Cycle No. 1 (Address Transition Controlled) for CY7C10612GE [20, 21]



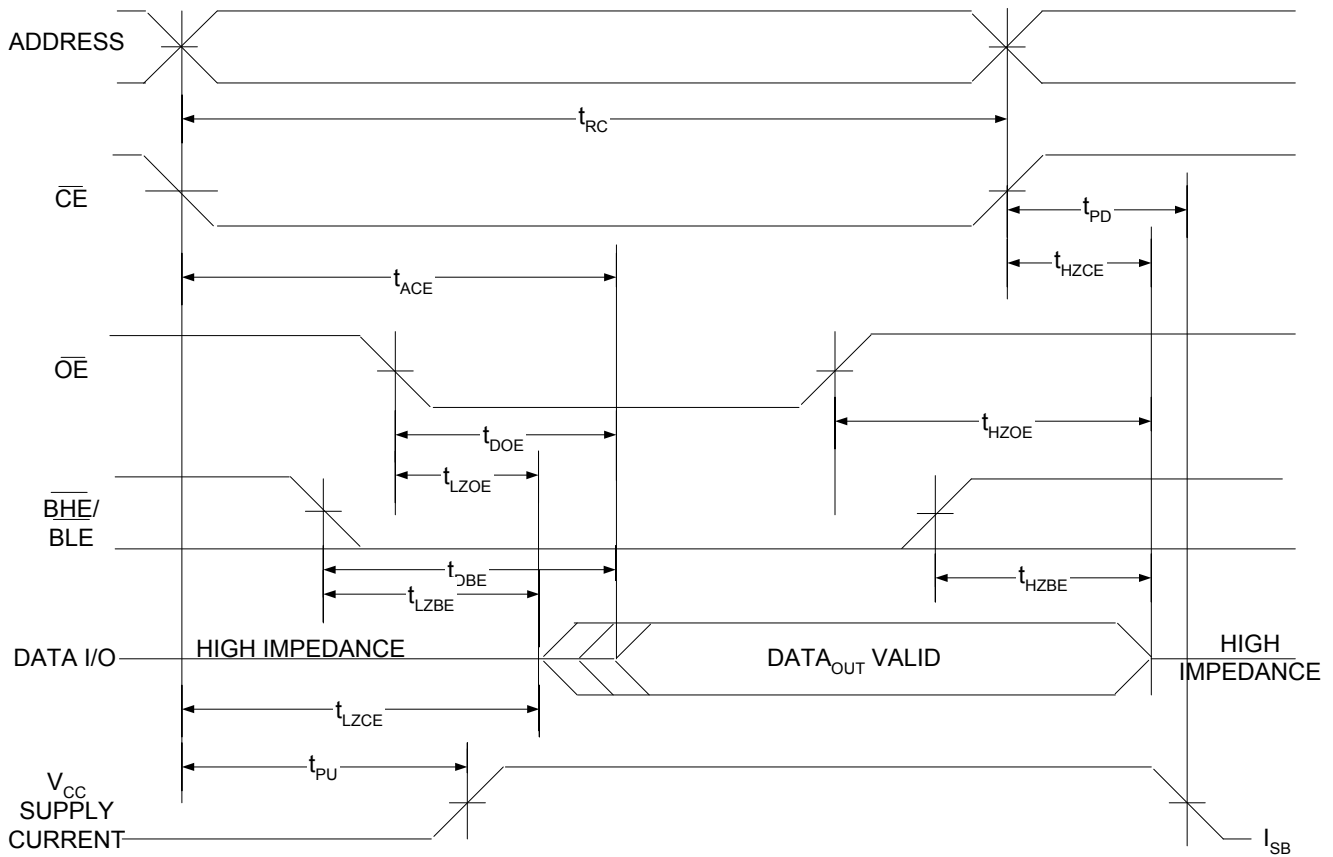
### Notes

19. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ .

20.  $\overline{WE}$  is HIGH for read cycle.

21. Address valid before or similar to  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)

**Figure 7. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [22, 23]

**Notes**

22.  $\overline{WE}$  is HIGH for read cycle.  
 23. Address valid before or similar to  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [24, 25, 26]

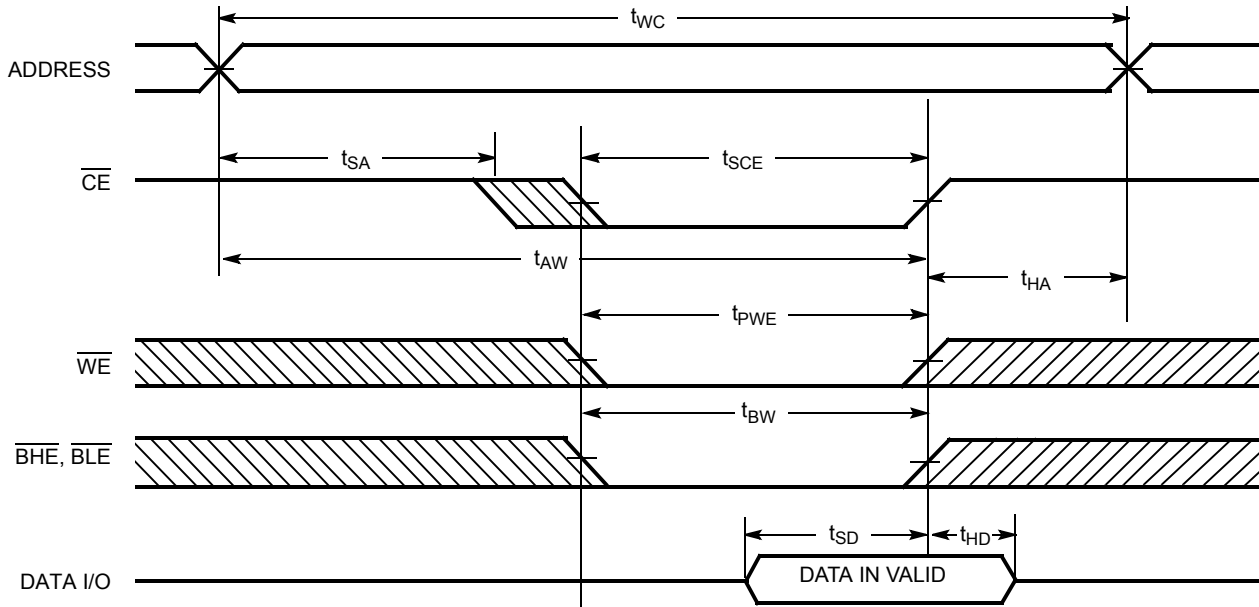
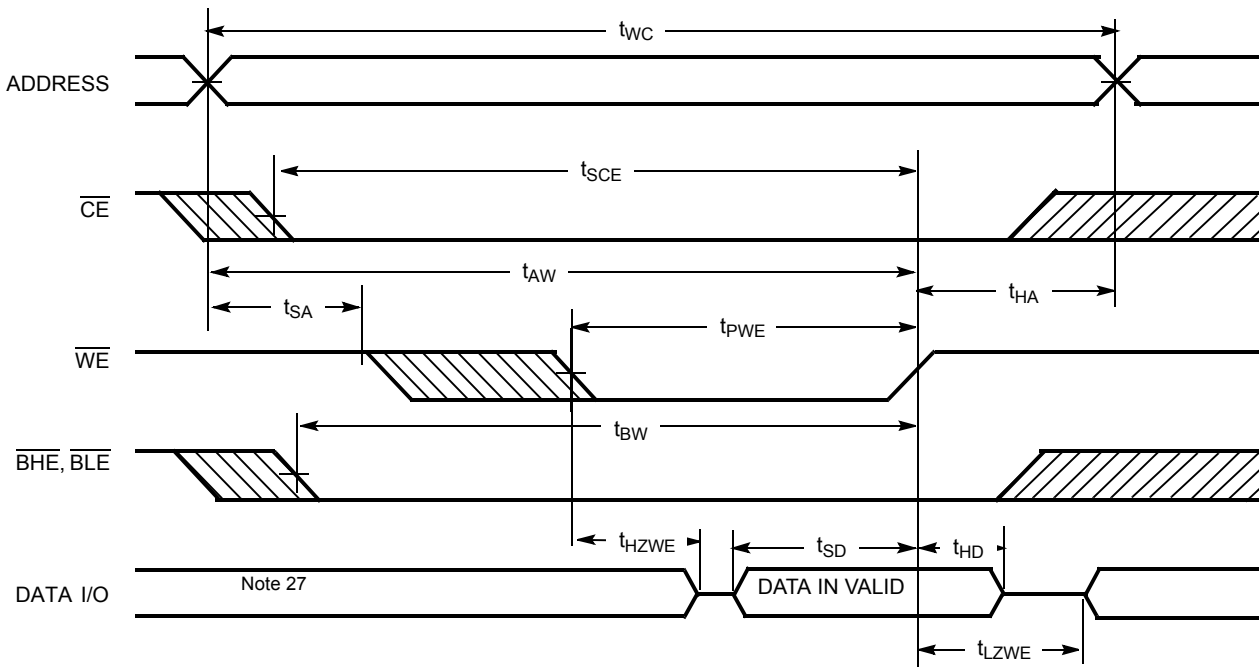


Figure 9. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [24, 25, 26]



Notes

24. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

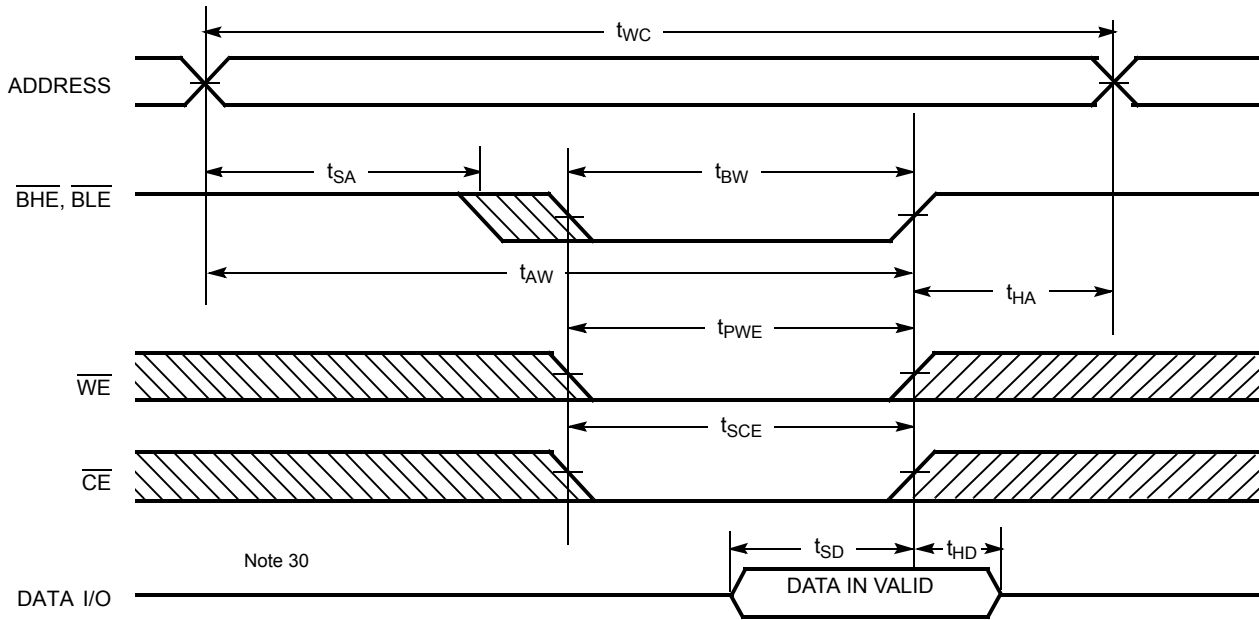
25. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$  and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

26. The minimum write cycle pulse width should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .

27. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 (BLE or BHE Controlled) [28, 29]



Notes

28. Data I/O is high impedance if  $\overline{OE}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .

29. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

30. During this period, the I/Os are in output state. Do not apply input signals.

**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data Out	High Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	High Z	Data Out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data In	High Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	High Z	Data In	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

**ERR Output – CY7C10612GE**

Output <sup>[31]</sup>	Mode
0	Read Operation, no error in the stored data.
1	Read Operation, single-bit error detected and corrected.
High-Z	Device deselected or Outputs disabled or Write Operation.

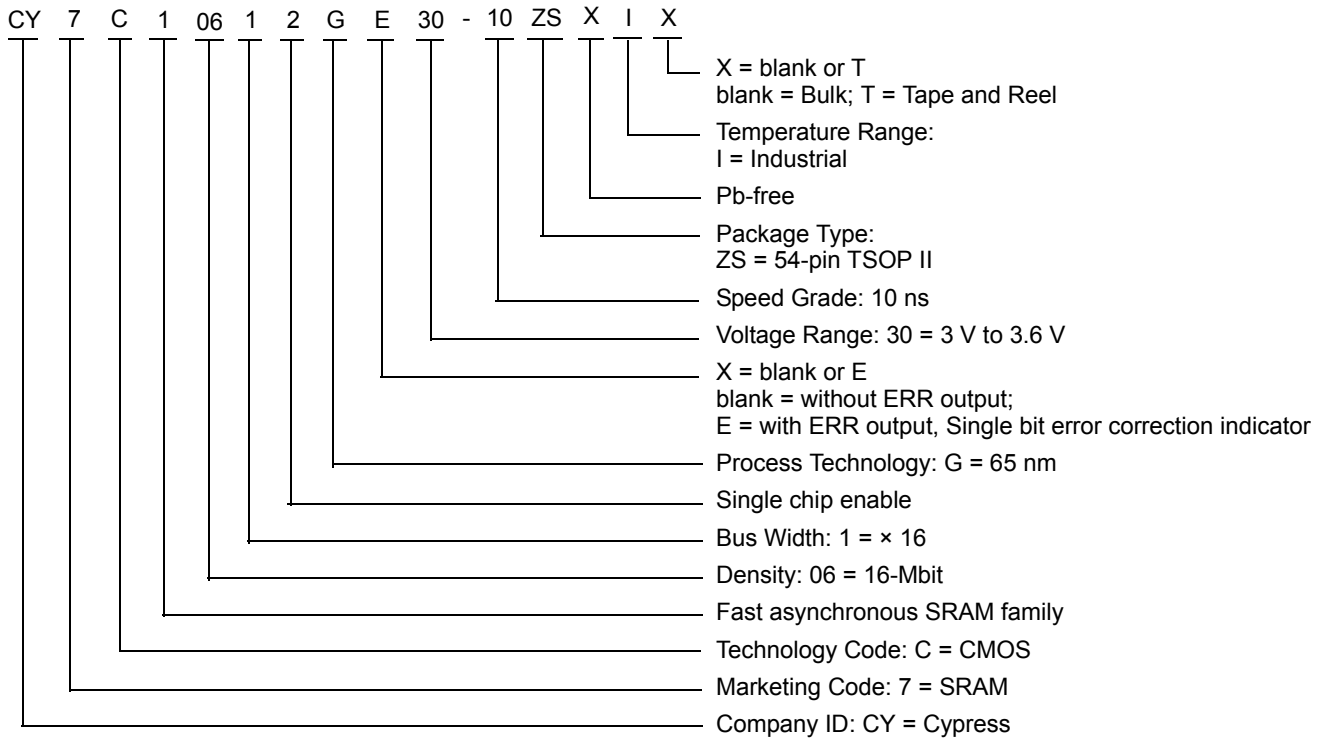
**Note**

31. ERR is an Output pin. If not used, this pin should be left floating.

### Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type (Pb-free)	Operating Range
10	CY7C10612G30-10ZSXI	51-85160	54-pin TSOP II	Industrial
	CY7C10612G30-10ZSXIT		54-pin TSOP II, Tape and Reel	
	CY7C10612GE30-10ZSXI		54-pin TSOP II, with ERR Pin	
	CY7C10612GE30-10ZSXIT		54-pin TSOP II, with ERR Pin, Tape and Reel	

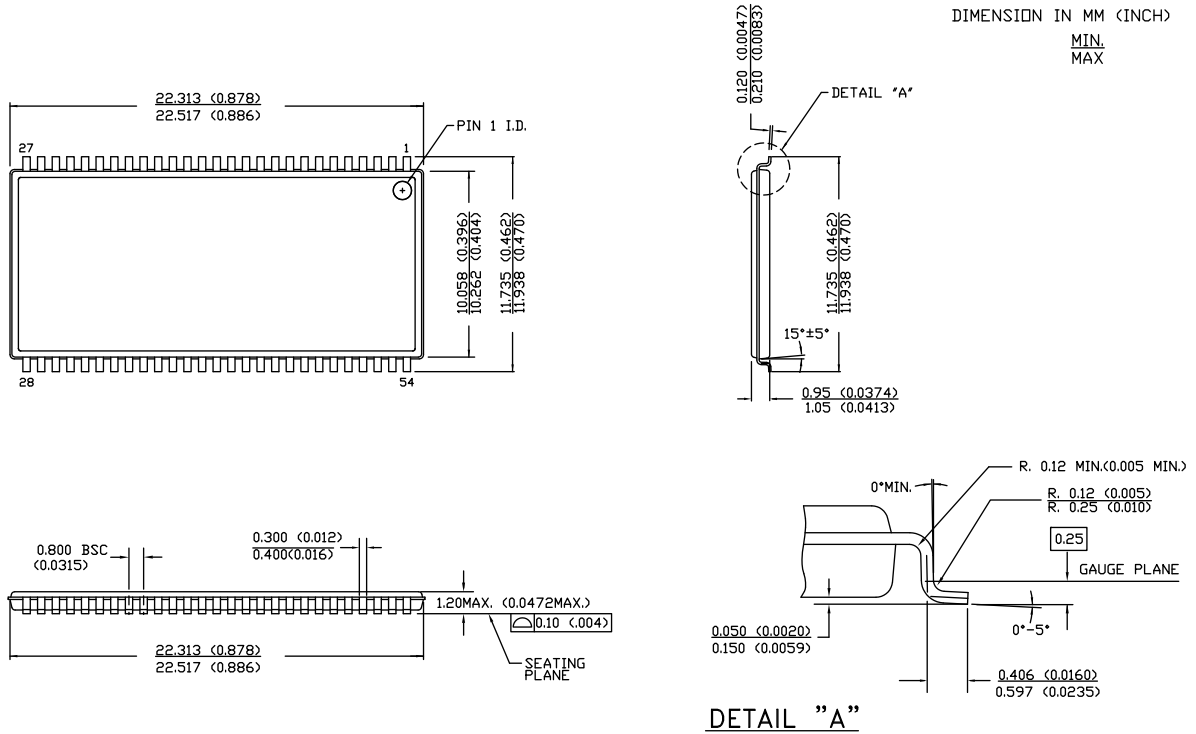
### Ordering Code Definitions





### Package Diagrams

Figure 11. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 \*E

## Acronyms

**Table 1. Acronyms Used in this Document**

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
MHz	megahertz
$\mu\text{A}$	microampere
$\mu\text{s}$	microsecond
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C10612G/CY7C10612GE, 16-Mbit (1M × 16) Static RAM				
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Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*D	4865557	NILE	07/31/2015	Changed status from Preliminary to Final.
*E	5437839	NILE	09/15/2016	Updated <a href="#">Maximum Ratings</a> : Updated Note 4 (Replaced “2 ns” with “20 ns”). Updated <a href="#">DC Electrical Characteristics</a> : Removed all values corresponding to V <sub>OH</sub> parameter. Included Operating Ranges “2.2 V to 2.7 V” and “2.7 V to 3.0 V” and all values corresponding to V <sub>OH</sub> parameter. Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Ordering Code Definitions</a> . Updated to new template. Completing Sunset Review.
*F	6011828	AESATMP8	01/03/2018	Updated logo and Copyright.

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