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CY7C2268KV18/CY7C2270KV18

36-Mbit DDR II+ SRAM Two-Word Burst Architecture (2.5 Cycle Read Latency) with ODT

Features

- 36-Mbit density (2M × 18, 1M × 36)
- 550 MHz clock for high bandwidth
- Two-word burst for reducing address bus frequency
- Double data rate (DDR) interfaces (data transferred at 1100 MHz) at 550 MHz
- Available in 2.5 clock cycle latency
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high speed systems
- Data valid pin (QVLD) to indicate valid data on the output
- On-die termination (ODT) feature
  - Supported for $D_{[x:0]}$, $BWS_{[x:0]}$, and K/$\overline{K}$ inputs
- Synchronous internally self-timed writes
- DDR II+ operates with 2.5 cycle read latency when $\overline{DOFF}$ is asserted HIGH
- Operates similar to DDR I device with 1 cycle read latency when $\overline{DOFF}$ is asserted LOW
- Core V_{DD} = 1.8 V ± 0.1 V; I/O V_{DDQ} = 1.4 V to V_{DD}[1]
  - Supports both 1.5 V and 1.8 V I/O supply
- HSTL inputs and variable drive HSTL output buffers
- Available in 165-ball FBGA package (13 × 15 × 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1 compatible test access port
- Phase-locked loop (PLL) for accurate data placement

Configurations

With Read Cycle Latency of 2.5 Cycles:

CY7C2268KV18 – 2M × 18

CY7C2270KV18 – 1M × 36

Functional Description

The CY7C2268KV18, and CY7C2270KV18 are 1.8 V synchronous pipelined SRAMs equipped with DDR II+ architecture. The DDR II+ consists of an SRAM core with advanced synchronous peripheral circuitry. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of K and $\overline{K}$. Each address location is associated with two 18-bit words (CY7C2268KV18), or 36-bit words (CY7C2270KV18) that burst sequentially into or out of the device.

These devices have an on-die termination feature supported for $D_{[x:0]}$, $BWS_{[x:0]}$, and K/$\overline{K}$ inputs, which helps eliminate external termination resistors, reduce cost, reduce board area, and simplify board routing.

Asynchronous inputs include an output impedance matching input (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need for separately capturing data from each individual DDR SRAM in the system design.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

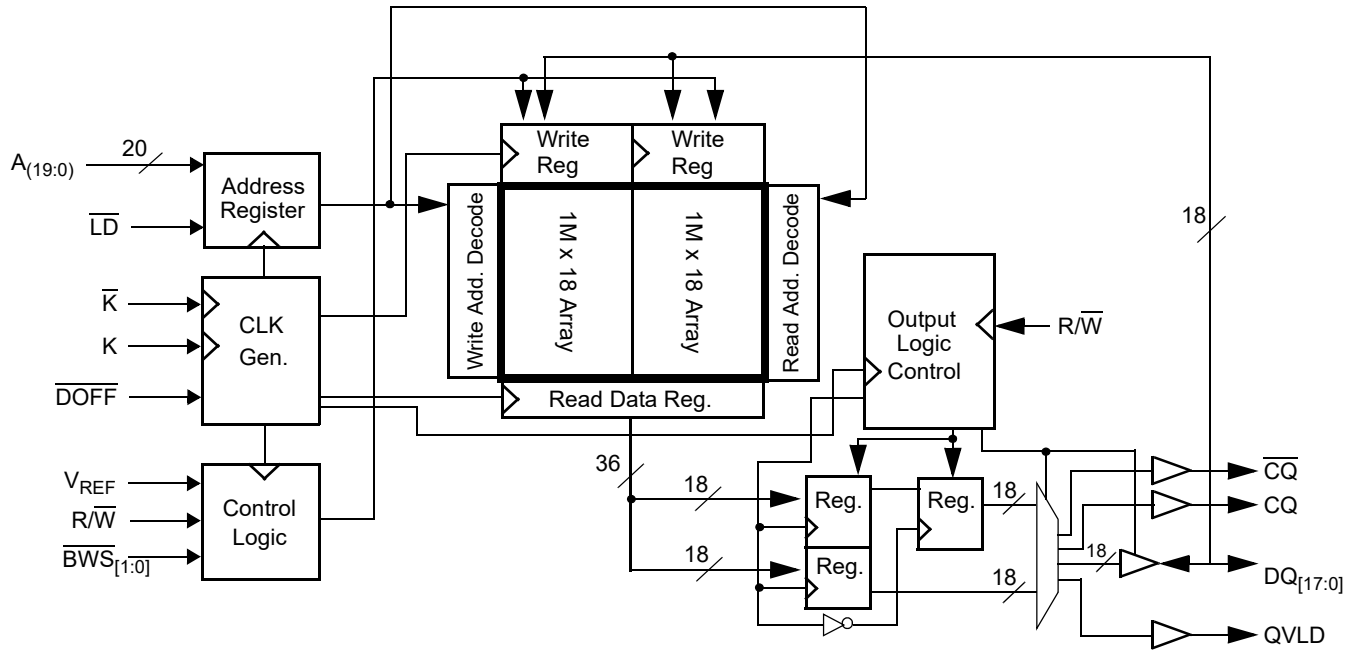
For a complete list of related documentation, click here.

Selection Guide

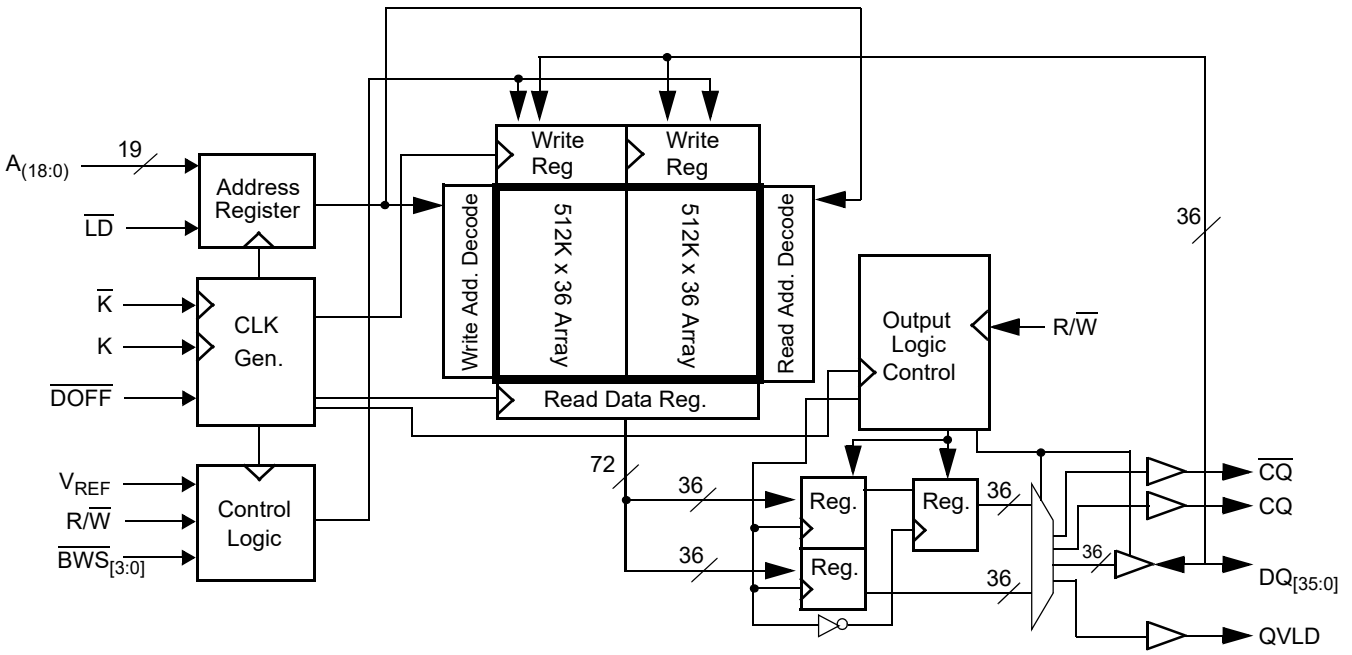
Description		550 MHz	450 MHz	400 MHz	Unit
Maximum operating frequency		550	450	400	MHz
Maximum operating current	× 18	700	600	Not Offered	mA
	× 36	890	Not Offered	690	

Note
1. The Cypress QDR II+ devices surpass the QDR consortium specification and can support V_{DDQ} = 1.4 V to V_{DD}.

Logic Block Diagram – CY7C2268KV18



Logic Block Diagram – CY7C2270KV18



Contents

Pin Configurations

The pin configuration for CY7C2268KV18, and CY7C2270KV18 follow. [2]

Figure 1. 165-ball FBGA (13 × 15 × 1.4 mm) pinout

CY7C2268KV18 (2M × 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	QVLD	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	ODT	A	A	A	TMS	TDI

CY7C2270KV18 (1M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	R/$\overline{W}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{LD}$	A	NC/72M	CQ
B	NC	DQ27	DQ18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	A	NC	A	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	A	A	A	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	A	A	QVLD	A	A	NC	DQ9	DQ0
R	TDO	TCK	A	A	A	ODT	A	A	A	TMS	TDI

Note
2. NC/72M, NC/144M, and NC/288M are not connected to the die and can be tied to any voltage level.

Pin Definitions

Pin Name	I/O	Pin Description
$DQ_{[x:0]}$	Input output-synchronous	**Data input output signals**. Inputs are sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. These pins drive out the requested data when the read operation is active. Valid data is driven out on the rising edge of both the K and $\overline{K}$ clocks during read operations. When read access is deselected, $Q_{[x:0]}$ are automatically tri-stated. CY7C2268KV18 – $DQ_{[17:0]}$ CY7C2270KV18 – $DQ_{[35:0]}$
$\overline{LD}$	Input-synchronous	**Synchronous load**. Sampled on the rising edge of the K clock. This input is brought LOW when a bus cycle sequence is defined. This definition includes address and read/write direction. All transactions operate on a burst of 2 data. $\overline{LD}$ must meet the setup and hold times around edge of K.
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$	Input-synchronous	**Byte write select 0, 1, 2, and 3 – active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C2268KV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$ and $\overline{BWS_1}$ controls $D_{[17:9]}$. CY7C2270KV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$ and $\overline{BWS_3}$ controls $D_{[35:27]}$. All the byte write selects are sampled on the same edge as the data. Deselecting a byte write select ignores the corresponding byte of data and it is not written into the device.
A	Input-synchronous	**Address inputs**. Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 2 M × 18 (2 arrays each of 1 M × 18) for CY7C2268KV18, and 1 M × 36 (2 arrays each of 512 K × 36) for CY7C2270KV18.
R/$\overline{W}$	Input-synchronous	**Synchronous read or write input**. When $\overline{LD}$ is LOW, this input designates the access type (read when R/$\overline{W}$ is HIGH, write when R/$\overline{W}$ is LOW) for loaded address. R/$\overline{W}$ must meet the setup and hold times around edge of K.
QVLD	Valid output indicator	**Valid output indicator**. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
ODT [3]	On-die termination input pin	**On-die termination input**. This pin is used for on-die termination of the input signals. ODT range selection is made during power up initialization. A LOW on this pin selects a low range that follows RQ/3.33 for 175 Ω ≤ RQ ≤ 350 Ω (where RQ is the resistor tied to ZQ pin). A HIGH on this pin selects a high range that follows RQ/1.66 for 175 Ω ≤ RQ ≤ 250 Ω (where RQ is the resistor tied to ZQ pin). When left floating, a high range termination value is selected by default.
K	Input clock	**Positive input clock input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input clock	**Negative input clock input**. $\overline{K}$ is used to capture synchronous data being presented to the device and to drive out data through $Q_{[x:0]}$.
CQ	Echo clock	**Synchronous echo clock outputs**. This is a free running clock and is synchronized to the input clock (K) of the DDR II+. The timing for the echo clocks is shown in the Switching Characteristics on page 23.
$\overline{CQ}$	Echo clock	**Synchronous echo clock outputs**. This is a free running clock and is synchronized to the input clock ($\overline{K}$) of the DDR II+. The timing for the echo clocks is shown in the Switching Characteristics on page 23.
ZQ	Input	**Output impedance matching input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 × RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.

Note
3. On-die termination (ODT) feature is supported for $D_{[x:0]}$, $BWS_{[x:0]}$, and K/$\overline{K}$ inputs.

Pin Definitions *(continued)*

Pin Name	I/O	Pin Description
$\overline{DOFF}$	Input	**PLL turn off** – **active LOW**. Connecting this pin to ground turns off the PLL inside the device. The timing in the PLL turned off operation differs from those listed in this data sheet. For normal operation, this pin can be connected to a pull up through a 10 kΩ or less pull-up resistor. The device behaves in DDR I mode when the PLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with DDR I timing.
TDO	Output	**TDO pin for JTAG**.
TCK	Input	**TCK pin for JTAG**.
TDI	Input	**TDI pin for JTAG**.
TMS	Input	**TMS pin for JTAG**.
NC	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/72M	Input	**Not connected to the die**. Can be tied to any voltage level.
NC/144M	Input	**Not connected to the die**. Can be tied to any voltage level.
NC/288M	Input	**Not connected to the die**. Can be tied to any voltage level.
V_{REF}	Input-reference	**Reference voltage input**. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the device**.
V_{DDQ}	Power supply	**Power supply inputs for the outputs of the device**.

Functional Overview

The CY7C2268KV18, and CY7C2270KV18 are synchronous pipelined burst SRAMs equipped with a DDR interface, which operates with a read latency of two and half cycles when $\overline{DOFF}$ pin is tied HIGH. When $\overline{DOFF}$ pin is set LOW or connected to V_{SS} the device behaves in DDR I mode with a read latency of one clock cycle.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input and output timing is referenced from the rising edge of the input clocks (K and $\overline{K}$).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

All synchronous control (R/$\overline{W}$, $\overline{LD}$, $\overline{BWS}_{[X:0]}$) inputs pass through input registers controlled by the rising edge of the input clock (K).

CY7C2268KV18 is described in the following sections. The same basic descriptions apply to CY7C2270KV18.

Read Operations

The CY7C2268KV18 is organized internally as two arrays of 1M × 18. Accesses are completed in a burst of 2 sequential 18-bit data words. Read operations are initiated by asserting R/$\overline{W}$ HIGH and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to the address inputs is stored in the read address register. Following the next two $\overline{K}$ clock rise, the corresponding 18-bit word of data from this address location is driven onto the $Q_{[17:0]}$ using $\overline{K}$ as the output timing reference. On the subsequent rising edge of K, the next 18-bit data word is driven onto the $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the input clock (K and $\overline{K}$). To maintain the internal logic, each read access must be allowed to complete. Read accesses can be initiated on every rising edge of the positive input clock (K).

When read access is deselected, the CY7C2268KV18 first completes the pending read transactions. Synchronous internal circuitry automatically tri-states the output following the next rising edge of the negative input clock ($\overline{K}$). This enables for a transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting R/$\overline{W}$ LOW and $\overline{LD}$ LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the write address register. On the following K clock rise, the data presented to $D_{[17:0]}$ is latched and stored into the 18-bit write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock (K) the information presented to $D_{[17:0]}$ is also stored into the write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. The 36 bits of data are then written into the memory array at the specified location. Write accesses can be initiated on every rising edge of the positive input clock (K). Doing so pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When the write access is deselected, the device ignores all inputs after the pending write operations are completed.

Byte Write Operations

Byte write operations are supported by the CY7C2268KV18. A write operation is initiated as described in the section Write Operations on page 6. The bytes that are written are determined

by $\overline{BWS_0}$ and $\overline{BWS_1}$, which are sampled with each set of 18-bit data words. Asserting the appropriate byte write select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the byte write select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read, modify, or write operations to a byte write operation.

DDR Operation

The CY7C2268KV18 enables high performance operation through high clock frequencies (achieved through pipelining) and DDR mode of operation. The CY7C2268KV18 requires two No Operation (NOP) cycle during transition from a read to a write cycle. At higher frequencies, some applications require third NOP cycle to avoid contention.

If a read occurs after a write cycle, address and data for the write are stored in registers. The write information is stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the read(s), the stored data from the earlier write is written into the SRAM array. This is called a posted write.

If a read is performed on the same address on which a write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

Depth Expansion

Depth expansion requires replicating the $\overline{LD}$ control signal for each bank. All other control signals can be common between banks as appropriate.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5 × the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with V_{DDQ} = 1.5 V. The output impedance is adjusted every 1024 cycles upon power-up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the DDR II+ to simplify data capture on high speed systems. Two echo clocks are generated by the DDR II+. CQ is referenced with respect to K and $\overline{CQ}$ is referenced with respect to $\overline{K}$. These are free-running clocks and are synchronized to the input clock of the DDR II+. The timing for the echo clocks is shown in the Switching Characteristics on page 23.

Valid Data Indicator (QVLD)

QVLD is provided on the DDR II+ to simplify data capture on high speed systems. The QVLD is generated by the DDR II+ device along with data output. This signal is also edge aligned with the echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

On-Die Termination (ODT)

These devices have an on-die termination feature for data inputs ($D_{[x:0]}$), byte write selects ($BWS_{[x:0]}$), and input clocks (K and $\overline{K}$). The termination resistors are integrated within the chip. The ODT range selection is enabled through ball R6 (ODT pin). The ODT termination tracks value of RQ where RQ is the resistor tied to the ZQ pin. ODT range selection is made during power-up initialization. A LOW on this pin selects a low range that follows RQ/3.33 for 175 Ω ≤ RQ ≤ 350 Ω (where RQ is the resistor tied to ZQ pin). A HIGH on this pin selects a high range that follows RQ/1.66 for 175 Ω ≤ RQ ≤ 250 Ω (where RQ is the resistor tied to ZQ pin). When left floating, a high range termination value is selected by default. For a detailed description on the ODT implementation, refer to the application note, *On-Die Termination for QDRII+/DDRII+ SRAMs*.

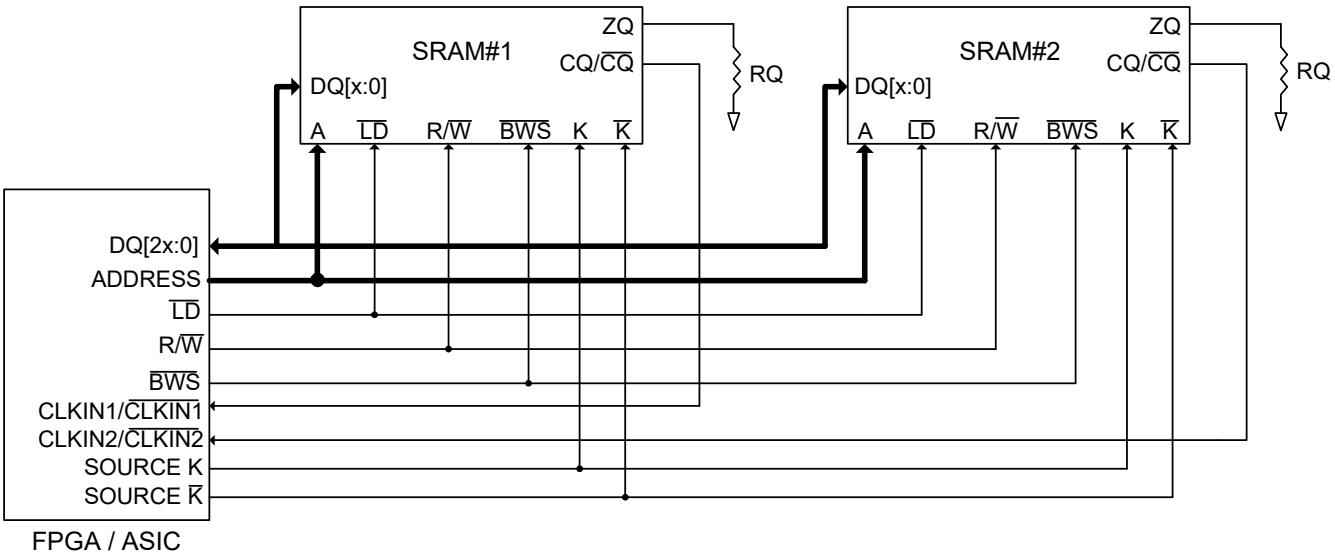
PLL

These chips use a PLL that is designed to function between 120 MHz and the specified maximum clock frequency. During power up, when the $\overline{DOFF}$ is tied HIGH, the PLL is locked after 20 µs of stable clock. The PLL can also be reset by slowing or stopping the input clock K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary to reset the PLL to lock to the desired frequency. The PLL automatically locks 20 µs after a stable clock is presented. The PLL may be disabled by applying ground to the $\overline{DOFF}$ pin. When the PLL is turned off, the device behaves in DDR I mode (with one cycle latency and a longer access time). For information, refer to the application note, *PLL Considerations in QDRII/DDRII/QDRII+/DDRII+*.

Application Example

Figure 2 shows two DDR II+ used in an application.

Figure 2. Application Example (Width Expansion)



Truth Table

The truth table for CY7C2268KV18 and CY7C2270KV18 follow. [4, 5, 6, 7, 8, 9]

Operation	K	$\overline{LD}$	R/$\overline{W}$	DQ	DQ
Write cycle: Load address; wait one cycle; input write data on consecutive K and $\overline{K}$ rising edges.	L–H	L	L	D(A) at K(t + 1) ↑	D(A+1) at $\overline{K}$(t + 1) ↑
Read cycle: (2.5 cycle latency) Load address; wait two and half cycles; read data on consecutive $\overline{K}$ and K rising edges.	L–H	L	H	Q(A) at $\overline{K}$(t + 2)↑	Q(A+1) at K(t + 3) ↑
NOP: No operation	L–H	H	X	High Z	High Z
Standby: Clock stopped	Stopped	X	X	Previous state	Previous state

Write Cycle Descriptions

The write cycle description table for and CY7C2268KV18 follows. [4, 10]

$\overline{BWS_0}$	$\overline{BWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence: CY7C2268KV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L–H	During the data portion of a write sequence: CY7C2268KV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence: CY7C2268KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence: CY7C2268KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence: CY7C2268KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence: CY7C2268KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Notes
4. X = “Don’t Care,” H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
5. Device powers up deselected with the outputs in a tri-state condition.
6. “A” represents address location latched by the devices when transaction was initiated. A + 1 represents the address sequence in the burst.
7. “t” represents the cycle at which a read/write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the “t” clock cycle.
8. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges as well.
9. It is recommended that K = $\overline{K}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
10. Is based on a write cycle that was initiated in accordance with Truth Table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

Write Cycle Descriptions

The write cycle description table for CY7C2270KV18 follows. [11, 12]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

Notes
11. X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
12. Is based on a write cycle that was initiated in accordance with Truth Table on page 9. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the set-up and hold requirements are achieved.

IEEE Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard. The TAP operates using JEDEC-standard V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which will not interfere with the operation of the device.

Test Access Port

Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see TAP Controller State Diagram on page. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram on page. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The Boundary Scan Order on page show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, -bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

7KH ,'&2'(LQVWUXFWLRQ FDXVHV D YHQGRUVSHFLILF ELW FRGH WR EH ORDGHG LQWR WKH LQVWUXFWLRQ UHJLVWHU ,W DOVR SODFHV WKH LQVWUXFWLRQ UHJLVWHU EHWZHHQ WKH 7', DQG 7'2 SLQV DQG VKLIWV WKH ,'&2'(RXW RI WKH GHYLFH ZKHQ WKH 7$3 FRQWUROOHU HQWHUV WKH 6KLIW '5 VWDWH 7KH ,'&2'(LQVWUXFWLRQ LV ORDGHG LQWR WKH LQVWUXFWLRQ UHJLVWHU XSRQ SRZHU XS RU ZKHQHYHU WKH 7$3 FRQWUROOHU LV VXSSOLHG D 7HVW /RJLF 5HVHW VWDWH

SAMPLE Z

7KH 6$03/(= LQVWUXFWLRQ FRQQHFWV WKH ERXQGDU\ VFDQ UHJLVWHU EHWZHHQ WKH 7', DQG 7'2 SLQV ZKHQ WKH 7$3 FRQWUROOHU LV LQ D 6KLIW '5 VWDWH 7KH 6$03/(= FRPPDQG SXWV WKH RXWSXW EXV LQWR D KLJK = VWDWH XQWLO WKH QH[W FRPPDQG LV VXSSOLHG GXULQJ WKH 8SGDWH ,5 VWDWH

SAMPLE/PRELOAD

6$03/(35(/2$' LV D PDQGDWRU\ LQVWUXFWLRQ :KHQ WKH 6$03/(35(/2$' LQVWUXFWLRQV DUH ORDGHG LQWR WKH LQVWUXFWLRQ UHJLVWHU DQG WKH 7$3 FRQWUROOHU LV LQ WKH &DSWXUH '5 VWDWH D VQDSVKRW RI GDWD RQ WKH LQSXWV DQG RXWSXW SLQV LV FDSWXUHG LQ WKH ERXQGDU\ VFDQ UHJLVWHU

7KH XVHU PXVW EH DZDUH WKDW WKH 7$3 FRQWUROOHU FORFN FDQ RQO\ RSHUDWH DW D IUHTXHQF\ XS WR 0+] ZKLOH WKH 65$0 FORFN RSHUDWHV PRUH WKDQ DQ RUGHU RI PDJQLWXGH IDVWHU %HFDXVH WKHUH LV D ODUJH GLIIHUHQFH LQ WKH FORFN IUHTXHQFLHV LW LV SRVVLEOH WKDW GXULQJ WKH &DSWXUH '5 VWDWH DQ LQSXW RU RXWSXW XQGHUJRHV D WUDQVLWLRQ 7KH 7$3 PD\ WKHQ WU\ WR FDSWXUH D VLJQDO ZKLOH LQ WUDQVLWLRQ PHWDVWDEOH VWDWH 7KLV GRHV QRW KDUP WKH GHYLFH EXW WKHUH LV QR JXDUDQWHH DV WR WKH YDOXH WKDW ZLOO EH FDSWXUHG 5HSHDWDEOH UHVXOWV PD\ QRW EH SRVVLEOH

7R JXDUDQWHH WKDW WKH ERXQGDU\ VFDQ UHJLVWHU FDSWXUHV WKH FRUUHFW YDOXH RI D VLJQDO WKH 65$0 VLJQDO PXVW EH VWDELOL]HG ORQJ HQRXJK WR PHHW WKH 7$3 FRQWUROOHU V FDSWXUH VHWXS SOXV KROG WLPHV W&6 DQG W&+ 7KH 65$0 FORFN LQSXW PLJKW QRW EH FDSWXUHG FRUUHFWO\ LI WKHUH LV QR ZD\ LQ D GHVLJQ WR VWRS RU VORZ WKH FORFN GXULQJ D 6$03/(35(/2$' LQVWUXFWLRQ ,I WKLV LV DQ LVVXH LW LV VWLOO SRVVLEOH WR FDSWXUH DOO RWKHU VLJQDOV DQG VLPSO\ LJQRUH WKH YDOXH RI WKH &. DQG &. FDSWXUHG LQ WKH ERXQGDU\ VFDQ UHJLVWHU

$IWHU WKH GDWD LV FDSWXUHG LW LV SRVVLEOH WR VKLIW RXW WKH GDWD E\ SXWWLQJ WKH 7$3 LQWR WKH 6KLIW '5 VWDWH 7KLV SODFHV WKH ERXQGDU\ VFDQ UHJLVWHU EHWZHHQ WKH 7', DQG 7'2 SLQV

35(/2$' SODFHV DQ LQLWLDO GDWD SDWWHUQ DW WKH ODWFKHG SDUDOOHO RXWSXWV RI WKH ERXQGDU\ VFDQ UHJLVWHU FHOOV EHIRUH WKH VHOHFWLRQ RI DQRWKHU ERXQGDU\ VFDQ WHVW RSHUDWLRQ

7KH VKLIWLQJ RI GDWD IRU WKH 6$03/(DQG 35(/2$' SKDVHV FDQ RFFXU FRQFXUUHQWO\ ZKHQ UHTXLUHG WKDW LV ZKLOH WKH GDWD FDSWXUHG LV VKLIWHG RXW WKH SUHORDGHG GDWD FDQ EH VKLIWHG LQ

BYPASS

:KHQ WKH %<3$66 LQVWUXFWLRQ LV ORDGHG LQ WKH LQVWUXFWLRQ UHJLVWHU DQG WKH 7$3 LV SODFHG LQ D 6KLIW '5 VWDWH WKH E\SDVV UHJLVWHU LV SODFHG EHWZHHQ WKH 7', DQG 7'2 SLQV 7KH DGYDQWDJH RI WKH %<3$66 LQVWUXFWLRQ LV WKDW LW VKRUWHQV WKH ERXQGDU\ VFDQ SDWK ZKHQ PXOWLSOH GHYLFHV DUH FRQQHFWHG WRJHWKHU RQ D ERDUG

EXTEST

7KH (;7(67 LQVWUXFWLRQ GULYHV WKH SUHORDGHG GDWD RXW WKURXJK WKH V\VWHP RXWSXW SLQV 7KLV LQVWUXFWLRQ DOVR FRQQHFWV WKH ERXQGDU\ VFDQ UHJLVWHU IRU VHULDO DFFHVV EHWZHHQ WKH 7', DQG 7'2 LQ WKH 6KLIW '5 FRQWUROOHU VWDWH

EXTEST OUTPUT BUS TRI-STATE

,(((6WDQGDUG PDQGDWHV WKDW WKH 7$3 FRQWUROOHU EH DEOH WR SXW WKH RXWSXW EXV LQWR D WUL VWDWH PRGH

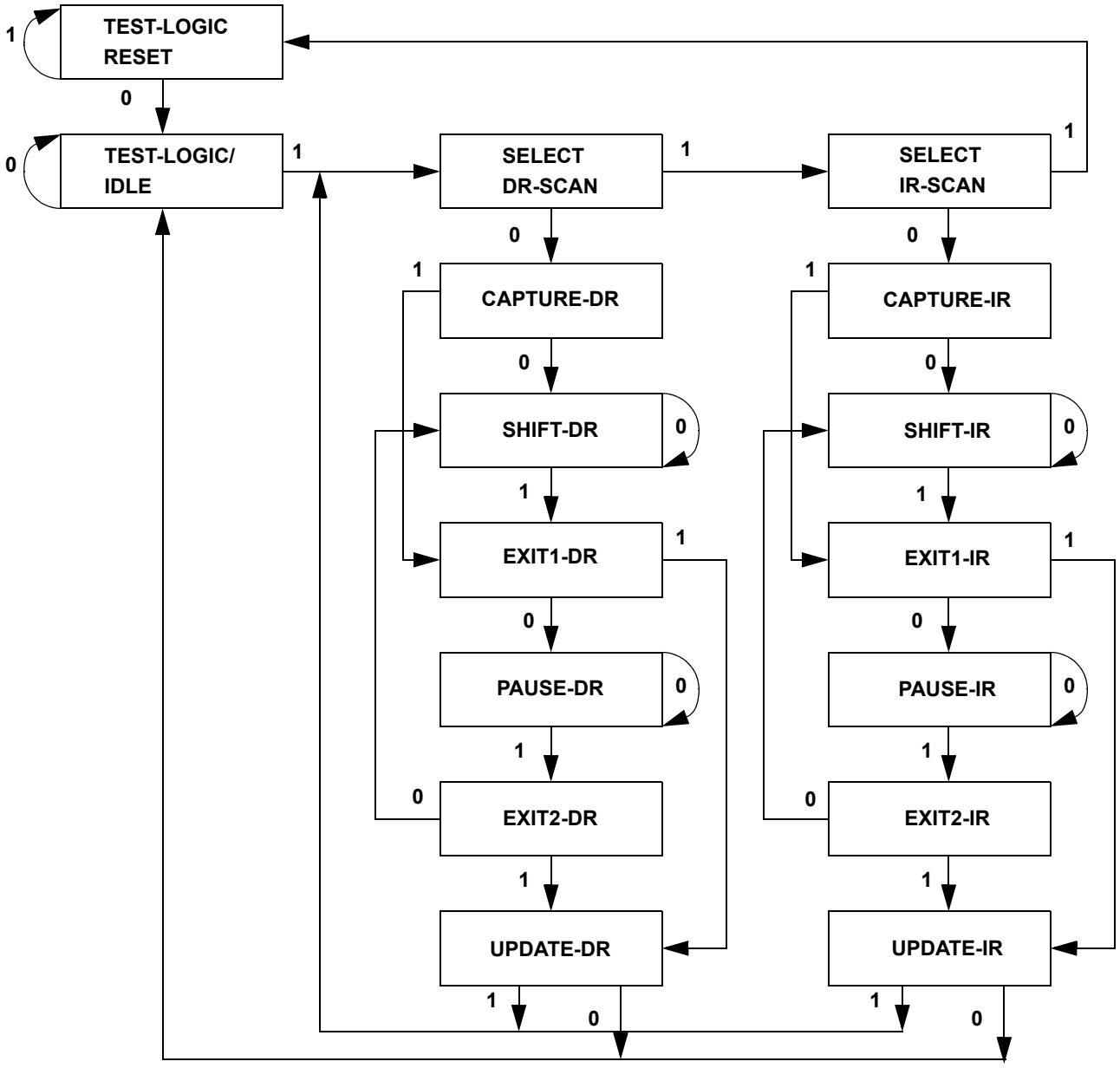
7KH ERXQGDU\ VFDQ UHJLVWHU KDV D VSHFLDO ELW ORFDWHG DW ELW 7KLV ELW FDQ EH VHW WR FRQWURO WKH RXWSXW EXV ZKHQ WKH (;7(67 LQVWUXFWLRQ LV HQWHUHG

Reserved

7KHVH LQVWUXFWLRQV DUH QRW LPSOHPHQWHG EXW DUH UHVHUYHG IRU IXWXUH XVH 'R QRW XVH WKHVH LQVWUXFWLRQV

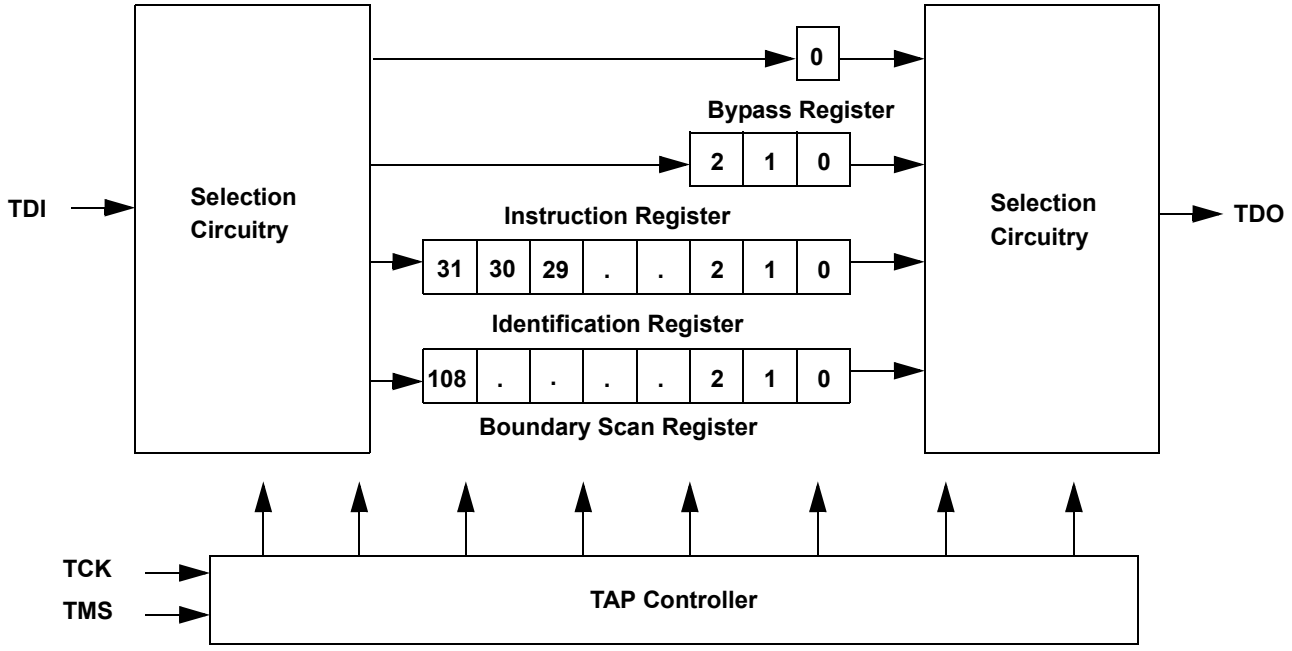
TAP Controller State Diagram

The state diagram for the TAP controller follows. [13]



Note
13. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range

Parameter [14, 15, 16]	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH voltage	I_{OH} = –2.0 mA	1.4	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	1.6	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2.0 mA	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 100 µA	–	0.2	V
V_{IH}	Input HIGH voltage		0.65 × V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		–0.3	0.35 × V_{DD}	V
I_X	Input and output load current	GND ≤ V_I ≤ V_{DD}	–5	5	µA

Notes
14. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics on page 20.
15. Overshoot: $V_{IH(AC)}$ < V_{DDQ} + 0.3 V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL(AC)}$ > –0.3 V (Pulse width less than $t_{CYC}/2$).
16. All voltage referenced to ground.

TAP AC Switching Characteristics

Over the Operating Range

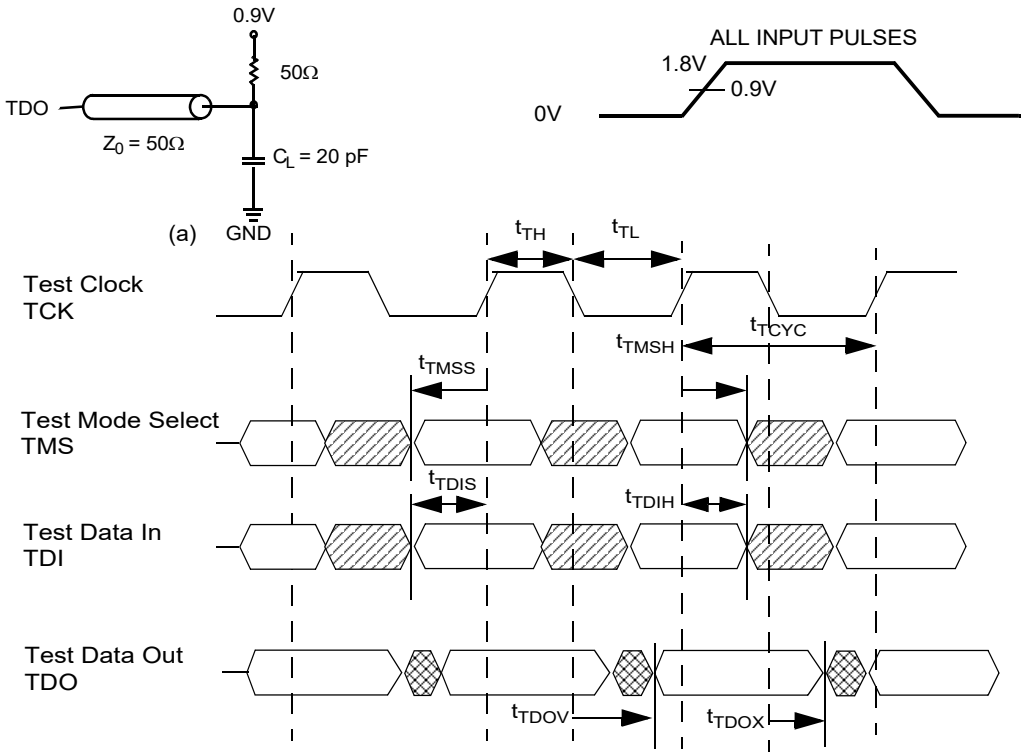
Parameter [17, 18]	Description	Min	Max	Unit
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH	20	–	ns
t_{TL}	TCK clock LOW	20	–	ns
Setup Times				
t_{TMSS}	TMS set-up to TCK clock rise	5	–	ns
t_{TDIS}	TDI set-up to TCK clock rise	5	–	ns
t_{CS}	Capture set-up to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns

Notes
17. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
18. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions

Figure 3 shows the TAP timing and test conditions. [19]

Figure 3. TAP Timing and Test Conditions



Notes
19. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

Identification Register Definitions

Instruction Field	Value		Description
	CY7C2268KV18	CY7C2270KV18	
Revision number (31:29)	000	000	Version number.
Cypress device ID (28:12)	11010111000010111	11010111000100111	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID register presence (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary scan	109

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J
27	11H

Bit #	Bump ID
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	10A
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A
54	7B
55	6B

Bit #	Bump ID
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	2A
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F
81	3G
82	2G
83	1H

Bit #	Bump ID
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R
108	Internal

Power Up Sequence in DDR II+ SRAM

DDR II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

Power Up Sequence

- Apply power and drive $\overline{DOFF}$ either HIGH or LOW (all other inputs can be HIGH or LOW).
  - Apply V_{DD} before V_{DDQ}.
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.
  - Drive $\overline{DOFF}$ HIGH.
- Provide stable $\overline{DOFF}$ (HIGH), power and clock (K, $\overline{K}$) for 20 µs to lock the PLL

PLL Constraints

- PLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The PLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the PLL is enabled, then the PLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 20 µs of stable clock to relock to the desired clock frequency.

Figure 4. Power Up Waveforms