

# 512-Kbit (32 K × 16) Static RAM

### **Features**

- Pin- and function-compatible with CY7C1020B
- High speed
  - □ t<sub>AA</sub> = 10 ns
- Low active power
  - $\Box$  I<sub>CC</sub> = 80 mA @ 10 ns
- Low complementary metal oxide semiconductor (CMOS) standby power
  - $\square$  I<sub>SB2</sub> = 3 mA
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin thin small outline package (TSOP) II packages

## **Functional Description**

The CY7C1020D <sup>[1]</sup> is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected. The input and output pins ( $IO_0$  through  $IO_{15}$ ) are placed in a high-impedance state when:

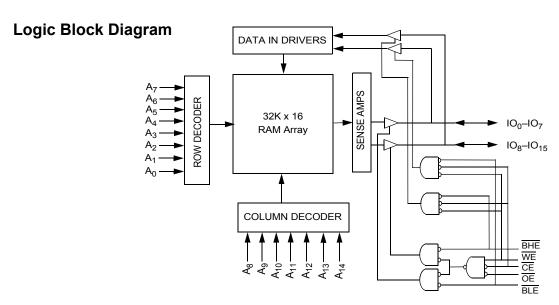
- Deselected (CE HIGH)
- Outputs are disabled (OE HIGH)
- BHE and BLE are disabled (BHE, BLE HIGH)
- When the write operation is active (CE LOW, and WE LOW)

Write to the device by taking Chip Enable  $(\overline{CE})$  and Write Enable  $(\overline{WE})$  inputs LOW. If Byte Low Enable  $(\overline{BLE})$  is LOW, then data from IO pins  $(IO_0$  through  $IO_7)$ , is written into the location specified on the address pins  $(A_0$  through  $A_{14})$ . If Byte High Enable  $(\overline{BHE})$  is LOW, then data from IO pins  $(IO_8$  through  $IO_{15})$  is written into the location specified on the address pins  $(A_0$  through  $A_{14})$ .

Reading from the device by taking Chip Enable  $(\overline{CE})$  and Output Enable  $(\overline{OE})$  LOW while forcing the Write Enable  $(\overline{WE})$  HIGH. If Byte Low Enable  $(\overline{BLE})$  is LOW, then data from the memory location specified by the address pins appears on  $IO_0$  to  $IO_7$ . If Byte High Enable  $(\overline{BHE})$  is LOW, then data from memory appears on  $IO_8$  to  $IO_{15}$ . See the "Truth Table" on page 11 for a complete description of read and write modes.

The CY7C1020D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.



### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.





## Contents

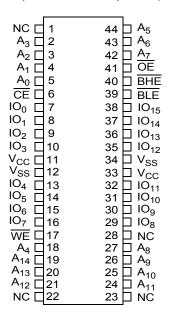
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## **Pin Configurations**

Figure 1. 44-pin SOJ/TSOP II pinout (Top View) [2]



## **Selection Guide**

Description	-10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current	3	mA

### Note

2. NC pins are not connected on the die.



## **Maximum Ratings**

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested. Storage temperature ......-65 °C to +150 °C Ambient temperature with power applied ......–55 °C to +125 °C Supply voltage on  $V_{CC}$  to Relative GND  $^{[3]}$  .....–0.5 V to +6.0 V 

DC input voltage [3]	–0.5 V to V <sub>CC</sub> + 0.5 V
Current into outputs (LOW)	20 mA
Static discharge voltage (per MIL-STD-883, Method 3015)	>2001 V
Latch-up current	>200 mA

## **Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>	Speed
Industrial	–40 °C to +85 °C	$5~V\pm0.5~V$	10 ns

### **Electrical Characteristics**

Over the Operating Range

Downston	Description	Took Conditions	Test Conditions		-10 (Industrial)	
Parameter	Description	lest Conditions			Max	Unit
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -4.0 mA	I <sub>OH</sub> = -4.0 mA		-	V
		I <sub>OH</sub> = -0.1 mA		_	3.4 <sup>[4]</sup>	
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 8.0 mA		_	0.4	V
V <sub>IH</sub>	Input HIGH voltage			2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW voltage [3]	_	-			V
I <sub>IX</sub>	Input load current	$GND \le V_I \le V_{CC}$	$GND \le V_{I} \le V_{CC}$			μΑ
I <sub>OZ</sub>	Output leakage current	GND $\leq V_1 \leq V_{CC}$ , output disabled	$GND \le V_1 \le V_{CC}$ , output disabled			
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	$V_{CC} = Max$ , $I_{OUT} = 0$ mA, $f = f_{max} = 1/t_{RC}$	100 MHz	_	80	mA
			83 MHz	_	72	mA
			66 MHz	_	58	mA
			40 MHz	_	37	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	Max $V_{CC}$ , $\overline{CE} \ge V_{IH}$ $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ , $f = f_{max}$		-	10	mA
I <sub>SB2</sub>	Automatic CE Power-Down current – CMOS inputs	$\begin{array}{c} \text{Max V}_{CC}, \ \overline{\text{CE}} \geq \text{V}_{CC} - 0.3 \text{ V}, \\ \text{V}_{\text{IN}} \geq \text{V}_{CC} - 0.3 \text{ V}, \text{ or V}_{\text{IN}} \leq 0.3 \text{ V} \end{array}$	′, f = 0	-	3	mA

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V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 1 V for pulse durations of less than 5 ns.
 Please note that the maximum V<sub>OH</sub> limit does not exceed minimum CMOS V<sub>IH</sub> of 3.5V. If you are interfacing this SRAM with 5V legacy processors that require a minimum V<sub>IH</sub> of 3.5V, please refer to Application Note AN6081 for technical details and options you may consider.



## Capacitance

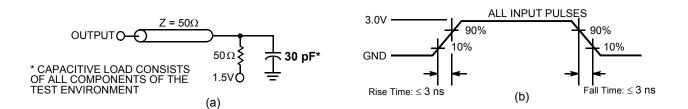
Parameter [5]	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = 5.0 \text{V}$	8	pF
C <sub>OUT</sub>	Output capacitance		8	pF

### **Thermal Resistance**

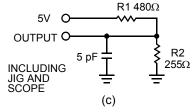
Parameter [5]	Description	Test Conditions	SOJ	TSOP II	Unit
$\Theta_{JA}$		Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	°C/W
30	Thermal resistance (junction to case)		36.75	21.24	°C/W

### **AC Test Loads and Waveforms**

Figure 2. AC Test Loads and Waveforms [6]



### **High-Z characteristics:**



### Notes

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<sup>5.</sup> Tested initially and after any design or process changes that may affect these parameters.

<sup>6.</sup> AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).



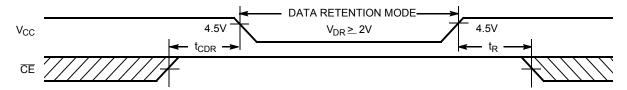
## **Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Min	Max	Unit	
$V_{DR}$	V <sub>CC</sub> for data retention	_	2.0	-	V
I <sub>CCDR</sub>	Data retention current	$V_{CC} = V_{DR} = 2.0 \text{ V}, \overline{CE} \ge V_{CC} - 0.3 \text{ V},$ $V_{IN} \ge V_{CC} - 0.3 \text{ V or } V_{IN} \le 0.3 \text{ V}$	_	3	mA
t <sub>CDR</sub> <sup>[7]</sup>	Chip deselect to data retention time	_	0	_	ns
t <sub>R</sub> <sup>[8]</sup>	Operation recovery time	-	t <sub>RC</sub>	_	ns

## **Data Retention Waveform**

Figure 3. Data Retention Waveform



- Notes
  7. Tested initially and after any design or process changes that may affect these parameters.
  8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \ge 50 \,\mu s$  or stable at  $V_{CC(min)} \ge 50 \,\mu s$ .



## **Switching Characteristics**

Over the Operating Range

[9]	B 1.41	-10 (Inc	dustrial)	11*
Parameter [9]	Description	Min	Max	Unit
Read Cycle			•	
t <sub>power</sub> <sup>[10]</sup>	V <sub>CC</sub> (typical) to the first access	100	-	μS
t <sub>RC</sub>	Read cycle time	10	-	ns
t <sub>AA</sub>	Address to data valid	-	10	ns
t <sub>OHA</sub>	Data hold from address change	3	-	ns
t <sub>ACE</sub>	CE LOW to data valid	-	10	ns
t <sub>DOE</sub>	OE LOW to data valid	-	5	ns
t <sub>LZOE</sub>	OE LOW to Low Z [12]	0		ns
t <sub>HZOE</sub>	OE HIGH to High Z [11, 12]	-	5	ns
t <sub>LZCE</sub>	CE LOW to Low Z [12]	3	-	ns
t <sub>HZCE</sub>	CE HIGH to High Z [11, 12]	-	5	ns
t <sub>PU</sub> <sup>[13]</sup>	CE LOW to power-up	0	-	ns
t <sub>PD</sub> <sup>[13]</sup>	CE HIGH to power-down	-	10	ns
t <sub>DBE</sub>	Byte enable to data valid		5	ns
t <sub>LZBE</sub>	Byte enable to Low Z	0	-	ns
t <sub>HZBE</sub>	Byte disable to High Z	-	5	ns
Write Cycle [14	, 15]	·		
t <sub>WC</sub>	Write cycle time	10	_	ns
t <sub>SCE</sub>	CE LOW to write end	7	-	ns
t <sub>AW</sub>	Address set-up to write end	7	-	ns
t <sub>HA</sub>	Address hold from write end	0	-	ns
t <sub>SA</sub>	Address set-up to write start	0	-	ns
t <sub>PWE</sub>	WE pulse width	7	-	ns
t <sub>SD</sub>	Data set-up to write end	6	-	ns
t <sub>HD</sub>	Data hold from write end	0	_	ns
t <sub>LZWE</sub>	WE HIGH to Low Z [12]	3	_	ns
t <sub>HZWE</sub>	WE LOW to High Z [11, 12]	-	5	ns
t <sub>BW</sub>	Byte enable to end of write	7	-	ns

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<sup>9.</sup> Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.

10. t<sub>POWER</sub> gives the minimum amount of time that the power supply should be at typical V<sub>CC</sub> values until the first memory access can be performed.

11. t<sub>HZOE</sub>, t<sub>HZBE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.

12. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZCE</sub>, and t<sub>HZWE</sub> for any given device.

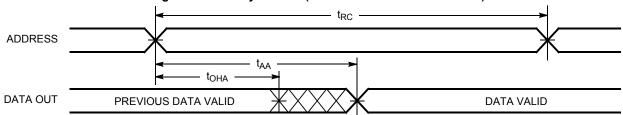
<sup>13.</sup> This parameter is guaranteed by design and is not tested.

 <sup>13.</sup> This parameter is guaranteed by design and is not tested.
 14. The internal write time of the memory is defined by the overlap of CE LOW, WE LOW and BHE/BLE LOW. CE, WE and BHE/BLE must be LOW to initiate a write and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
 15. The minimum write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) should be equal to the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

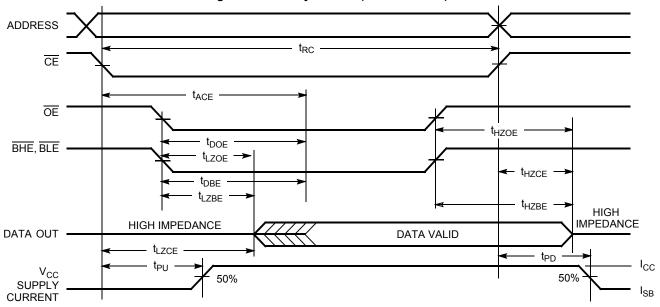


## **Switching Waveforms**

Figure 4. Read Cycle No.1 (Address Transition Controlled) [16, 17]







<sup>16.</sup> Device is continuously selected. OE, CE, BHE and/or BLE = V<sub>IL</sub>. 17. WE is HIGH for read cycle.

<sup>18.</sup> Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.



## **Switching Waveforms**(continued)

Figure 6. Write Cycle No. 1 (CE Controlled) [19, 20]

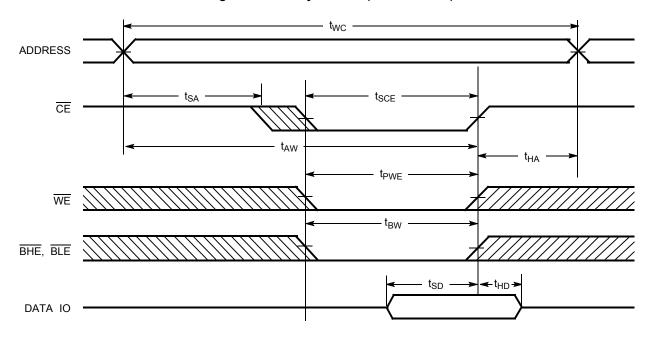
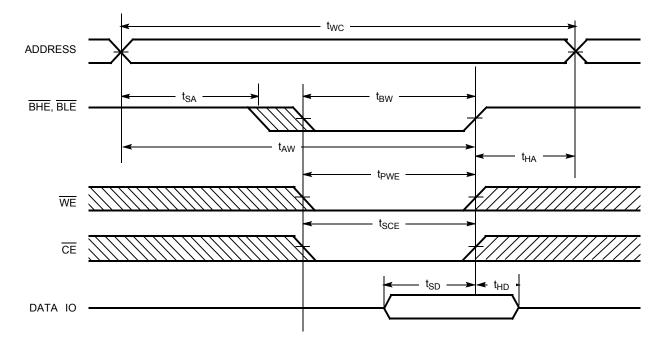


Figure 7. Write Cycle No. 2 (BLE or BHE Controlled) [19, 20]



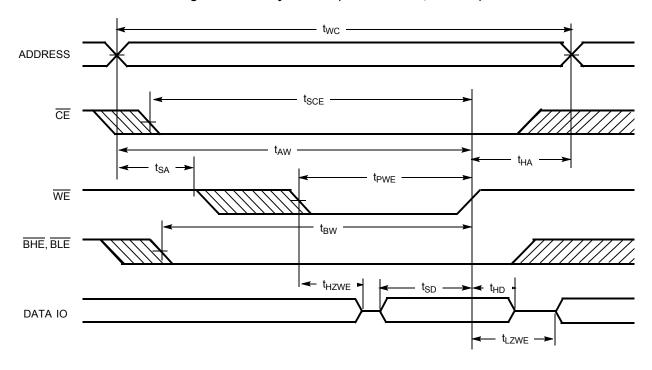
19. Data IO is high impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IH}$ .

20. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.



## **Switching Waveforms**(continued)

Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) [21, 22]



### Notes

<sup>21.</sup> The minimum write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) should be equal to the sum of t<sub>HZWE</sub> and t<sub>SD.</sub> 22. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.



## **Truth Table**

CE	OE	WE	BLE	BHE	IO <sub>0</sub> –IO <sub>7</sub>	IO <sub>8</sub> -IO <sub>15</sub>	Mode	Power
Н	Х	Х	X	X	High Z	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	Н	L	L	Data out	Data out	Read – All bits	Active (I <sub>CC</sub> )
			L	Н	Data out	High Z	Read – Lower bits only	Active (I <sub>CC</sub> )
			Н	L	High Z	Data out	Read – Upper bits only	Active (I <sub>CC</sub> )
L	Х	L	L	L	Data in	Data in	Write – All bits	Active (I <sub>CC</sub> )
			L	Н	Data in	High Z	Write – Lower bits only	Active (I <sub>CC</sub> )
			Н	L	High Z	Data in	Write – Upper bits only	Active (I <sub>CC</sub> )
L	Н	Н	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L	Х	Х	Н	Н	High Z	High Z	selected, outputs disabled	Active (I <sub>CC</sub> )

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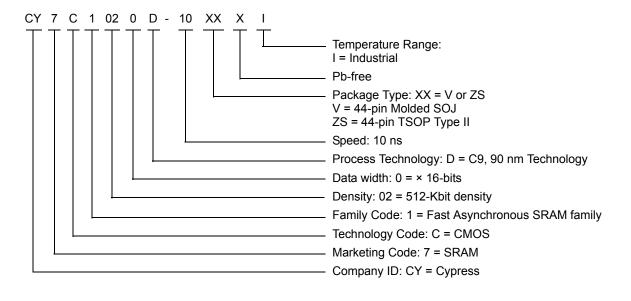


## **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1020D-10VXI	51-85082	44-pin SOJ (400 Mils) Pb-free	Industrial
	CY7C1020D-10ZSXI	51-85087	44-pin TSOP (Type II) Pb-free	

Please contact your local Cypress sales representative for availability of these parts.

### **Ordering Code Definitions**

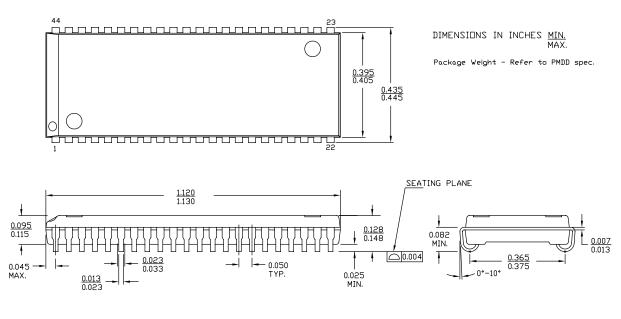


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# **Package Diagrams**

Figure 9. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082

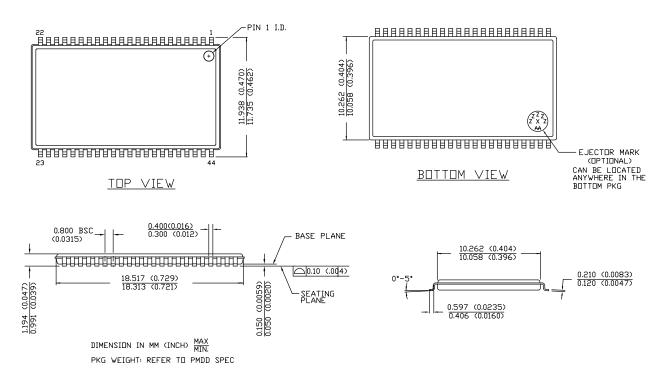


51-85082 \*E



## Package Diagrams(continued)

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 \*E



## **Acronyms**

Acronym	Description			
BGA	Ball Grid Array			
CMOS	Complementary Metal Oxide Semiconductor			
FBGA	Fine-Pitch Ball Gird Array			
I/O	Input/Output			
SRAM	Static Random Access Memory			
TSOP	Thin Small Outline Package			
TTL	Transistor-Transistor Logic			

## **Document Conventions**

## **Units of Measure**

Symbol	Unit of Measure			
°C	degree Celsius			
MHz	megahertz			
μΑ	microampere			
mA	milliampere			
ns	nanosecond			
Ω	ohm			
pF	picofarad			
V	volt			
W	watt			

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# **Document History Page**

Document Title: CY7C1020D, 512-Kbit (32 K × 16) Static RAM Document Number: 38-05463					
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change	
**	201560	See ECN	SWI	Advance Data sheet for C9 IPP	
*A	233695	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-0216)     Pb-free Offering in the 'Ordering Information'	
*B	263769	See ECN	RKF	1) Corrected pin #18 on SOJ/TSOPII Pinout (Page #1) from A <sub>15</sub> to A <sub>4</sub> 2) Changed IO <sub>1</sub> - IO <sub>16</sub> to IO <sub>0</sub> - IO <sub>15</sub> on the Pin-out diagram 3) Added T <sub>power</sub> Spec in Switching Characteristics Table 4) Added Data Retention Characteristics Table and Waveforms 5) Shaded 'Ordering Information'	
*C	307594	See ECN	RKF	Reduced Speed bins to -10, -12 and -15 ns	
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #3	
*E	802877	See ECN	VKN	Changed $I_{\rm CC}$ specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz	
*F	3109992	12/14/2010	AJU	Added Ordering Code Definitions. Updated Package Diagrams.	
*G	3219056	04/07/2011	PRAS	Added TOC Added Acronyms and Units of Measure table. Updated Datasheet as per template.	
*H	4033925	06/19/2013	MEMJ	Updated Functional Description. Updated Electrical Characteristics: Added one more Test Condition "I <sub>OH</sub> = -0.1mA" for V <sub>OH</sub> parameter and added maximum value corresponding to that Test Condition. Added Note 4 and referred the same note in maximum value for V <sub>OH</sub> parameter corresponding to Test Condition "I <sub>OH</sub> = -0.1mA". Updated Package Diagrams: spec 51-85082 – Changed revision from *C to *E. spec 51-85087 – Changed revision from *C to *E.	
*	4385769	05/21/2014	MEMJ	No technical updates. Completing Sunset Review.	
*J	4576526	11/21/2014	MEMJ	Added related documentation hyperlink in page 1.	

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