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# 16-Mbit (1 M words × 16 bit) Static RAM with PowerSnooze™ and ECC

## Features

- High speed
  - $t_{AA} = 10$  ns
- Ultra-low power PowerSnooze™<sup>[1]</sup> device
  - Deep Sleep (DS) current  $I_{DS} = 22$ - $\mu$ A maximum
- Low active and standby currents
  - $I_{CC} = 90$ -mA typical
  - $I_{SB2} = 20$ -mA typical
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- Embedded error-correcting code (ECC) for single-bit error correction
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages

## Functional Description

The CY7S1061G/CY7S1061GE is a high-performance CMOS fast static RAM organized as 1,048,576 words by 16 bits. This device features fast access times (10 ns) and a unique ultra-low power Deep Sleep mode. With Sleep mode currents as low as 22  $\mu$ A, the CY7S1061G device combines the best features of fast and low-power SRAM in industry-standard package options. The device also features embedded ECC<sup>[2]</sup>. ECC logic can detect and correct single-bit error in the accessed location. The CY7S1061GE device includes an ERR pin that signals an error-detection and correction event during a read cycle.

To access devices with a single-chip enable input, assert the chip enable input (CE) LOW. To access dual chip enable devices, assert both chip enable inputs –  $\overline{CE}_1$  as LOW and  $\overline{CE}_2$  as HIGH.

To perform data writes, assert the Write Enable ( $\overline{WE}$ ) input LOW, and provide the data and address on device data pins ( $I/O_0$  through  $I/O_{15}$ ) and address pins ( $A_0$  through  $A_{19}$ ) respectively. The Byte High Enable (BHE) and Byte Low Enable (BLE) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. BHE controls  $I/O_8$  through  $I/O_{15}$  and BLE controls  $I/O_0$  through  $I/O_7$ .

To perform data reads, assert the Output Enable ( $\overline{OE}$ ) input and provide the required address on the address lines. Read data is accessible on the I/O lines ( $I/O_0$  through  $I/O_{15}$ ). You can perform byte accesses by asserting the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH for single chip enable devices and  $\overline{CE}_1$  HIGH and  $\overline{CE}_2$  LOW for dual chip enable devices), or the control signals ( $\overline{OE}$ ,  $\overline{BLE}$ ,  $\overline{BHE}$ ) are de-asserted.

The device is placed in a low power Deep Sleep mode when the Deep Sleep pin (DS) is LOW. In this state, the device is disabled for normal operation and is placed in a data retention mode. The device can be activated by de-asserting the Deep Sleep pin ( $\overline{DS}$  HIGH).

The CY7S1061G/CY7S1061G is available in 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages.

For a complete list of related resources, [click here](#).

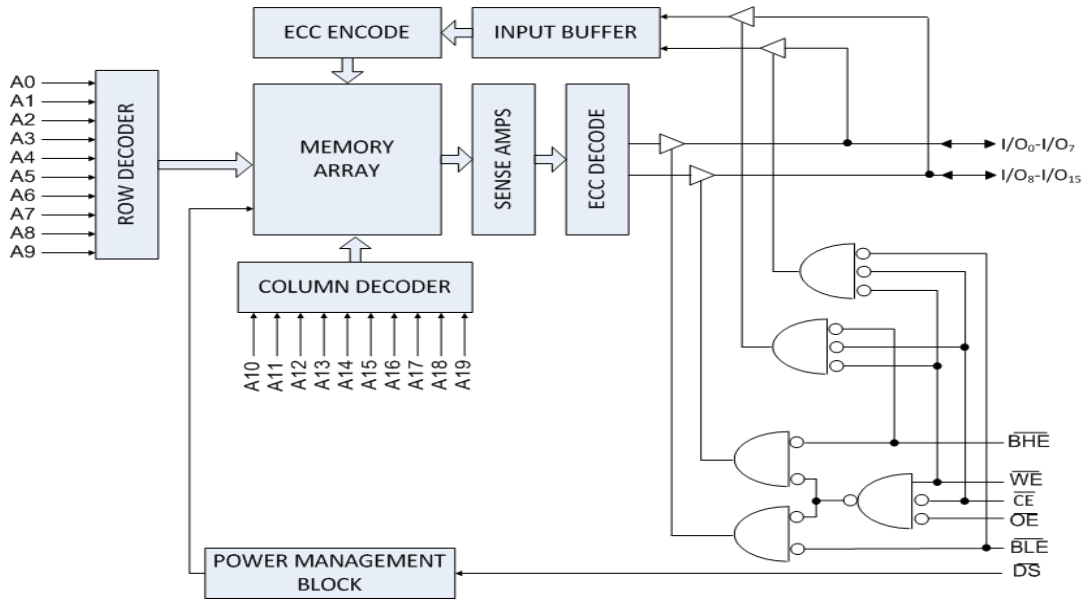
## Product Portfolio

Product	Range	$V_{CC}$ Range (V)	Speed (ns)	Current Consumption					
				Operating $I_{CC}$ (mA)		Standby, $I_{SB2}$ (mA)		Deep-Sleep Current ( $\mu$ A)	
				$f = f_{max}$		Typ <sup>[3]</sup>	Max	Typ <sup>[1]</sup>	Max
				Typ <sup>[3]</sup>	Max				
CY7S1061G18	Industrial	1.65 V–2.2 V	15	70	80	20	30	8	22
CY7S1061G(E)30		2.2 V–3.6 V	10	90	110				
CY7S1061G		4.5–5.5 V	10	90	110				

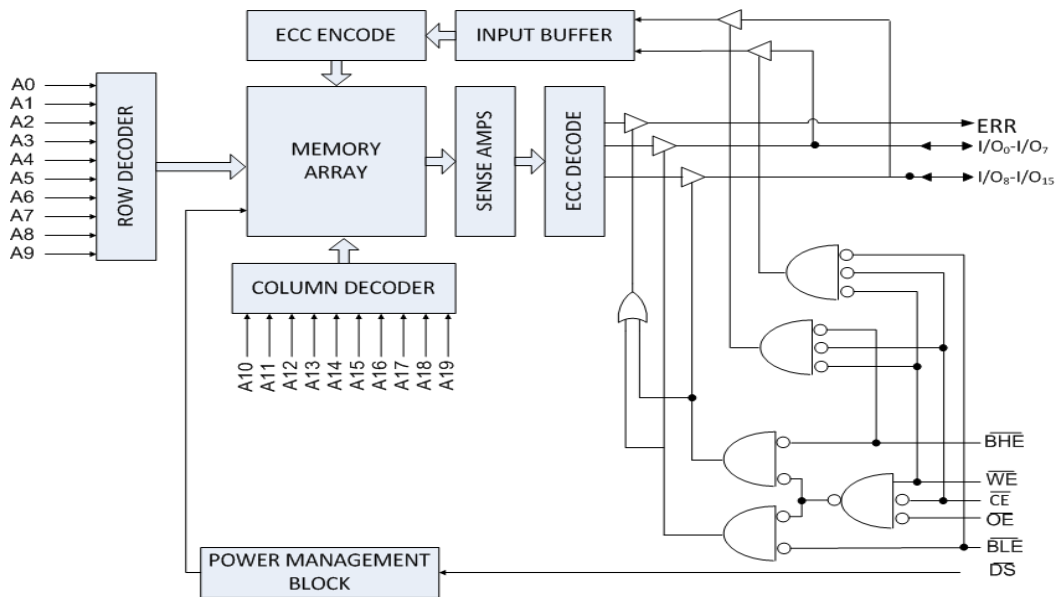
### Notes

1. Refer to AN89371 for details on PowerSnooze™ feature of this device.
2. This device does not support automatic write-back on error detection.
3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8$  V (for a  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3$  V (for a  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC} = 5$  V (for a  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25$  °C.

Logic Block Diagram – CY7S1061G



Logic Block Diagram – CY7S1061GE



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## Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout (Top View) <sup>[4]</sup>

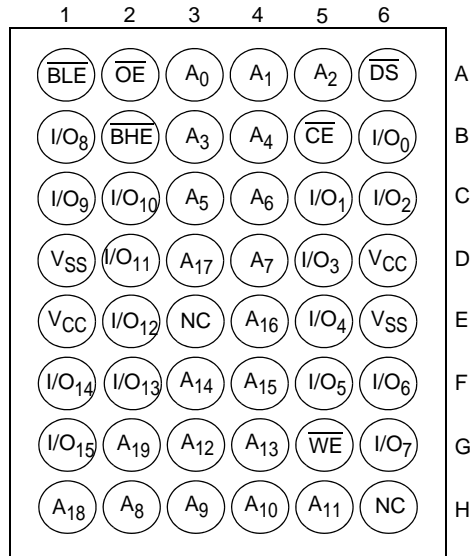
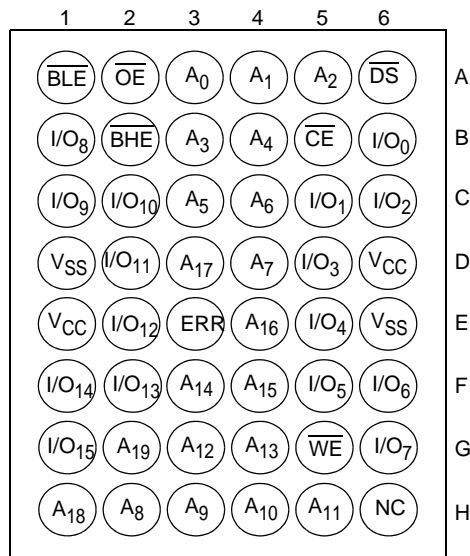


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout with ERR (Top View) <sup>[4]</sup>

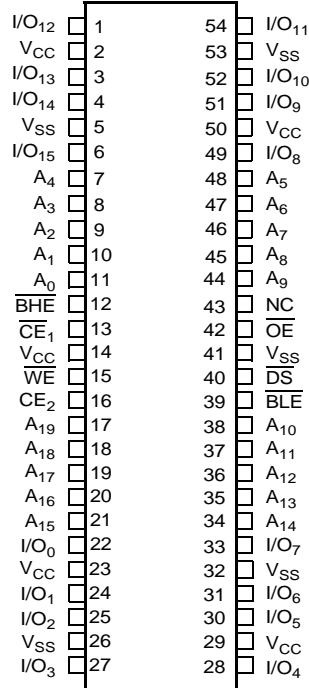


**Note**

- 4. NC pins are not connected internally to the die.

**Pin Configurations** (continued)

**Figure 3. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Pinout** <sup>[5]</sup>



**Note**

- NC pins are not connected internally to the die.

Pin Configurations (continued)

Figure 4. 48-pin TSOP I (12 x 18.4 x 1 mm) Pinout (Top View) [6]

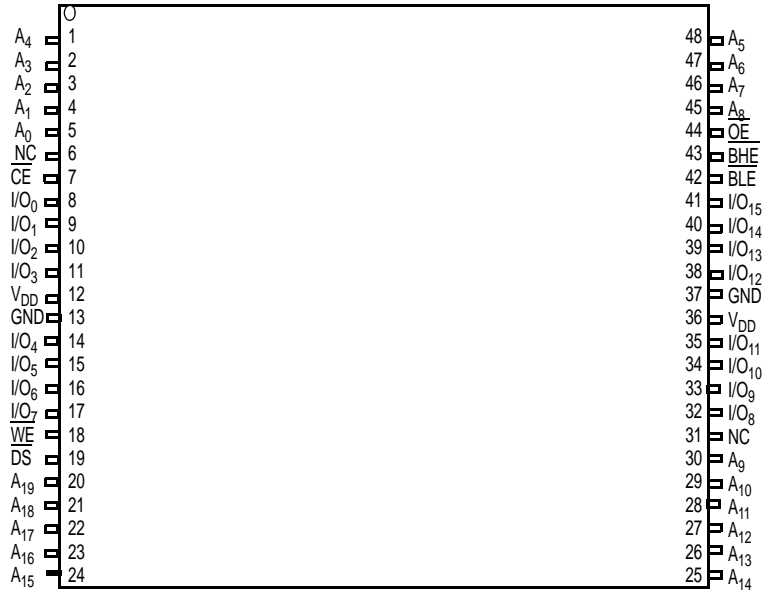
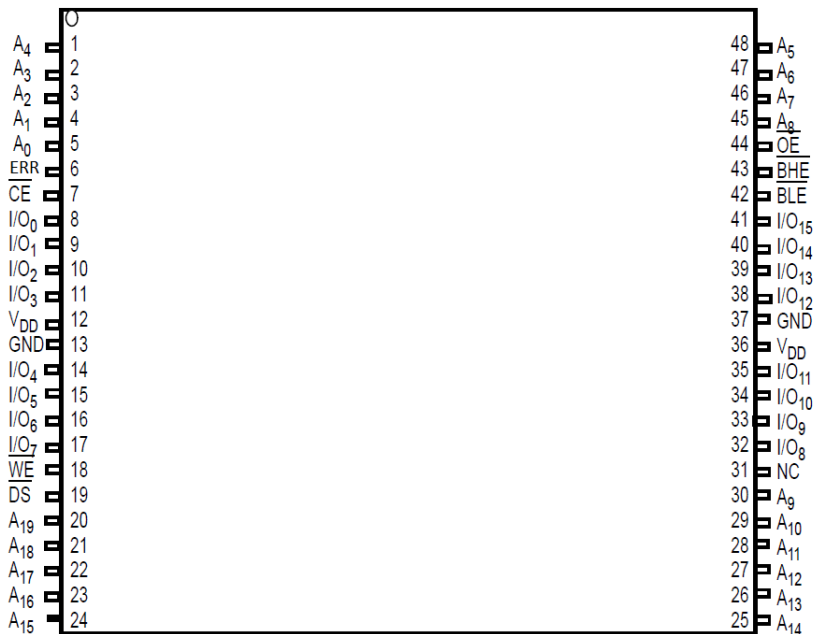


Figure 5. 48-pin TSOP I (12 x 18.4 x 1 mm) Pinout, ERR Output at Pin 6 (Top View)



Note

6. NC pins are not connected internally to the die.

### Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

- Storage temperature ..... -65 °C to +150 °C
- Ambient temperature with power applied ..... -55 °C to +125 °C
- Supply voltage on V<sub>CC</sub> relative to GND <sup>[7]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V
- DC voltage applied to outputs in High Z State <sup>[7]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

- DC input voltage <sup>[7]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V
- Current into outputs (LOW) ..... 20 mA
- Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V
- Latch-up current ..... > 140 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

### DC Electrical Characteristics

Over the operating range of -40 °C to +85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit	
			Min	Typ <sup>[8]</sup>	Max		
V <sub>OH</sub>	Output HIGH voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	1.4	-	-	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.0	-	-	
		2.7 V to 3.0 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.2	-	-	
		3.0 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	-	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> - 0.4 <sup>[9]</sup>	-	-	
V <sub>OL</sub>	Output LOW voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.2	V
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2 mA	-	-	0.4	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	-	0.4	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	-	0.4	
V <sub>IH</sub> <sup>[7, 10]</sup>	Input HIGH voltage	1.65 V to 2.2 V	-	1.4	-	V <sub>CC</sub> + 0.2	V
		2.2 V to 2.7 V	-	2.0	-	V <sub>CC</sub> + 0.3	
		2.7 V to 3.6 V	-	2.0	-	V <sub>CC</sub> + 0.3	
		4.5 V to 5.5 V	-	2.2	-	V <sub>CC</sub> + 0.5	
V <sub>IL</sub> <sup>[7, 10]</sup>	Input LOW voltage	1.65 V to 2.2 V	-	-0.2	-	0.4	V
		2.2 V to 2.7 V	-	-0.3	-	0.6	
		2.7 V to 3.6 V	-	-0.3	-	0.8	
		4.5 V to 5.5 V	-	-0.5	-	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> (for all pins except $\overline{DS}$ ) V <sub>IN</sub> = GND (or) V <sub>IN</sub> ≥ V <sub>IH</sub> (for DS pin only)	-1.0	-	+1.0	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1.0	-	+1.0	μA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, CMOS levels	f = 100 MHz f = 66.7 MHz	- -	90.0 70.0	110.0 80.0	mA
I <sub>SB1</sub>	Standby current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE}^{[11]}$ ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	-	-	40.0	mA
I <sub>SB2</sub>	Standby current – CMOS inputs	Max V <sub>CC</sub> , $\overline{CE}^{[11]}$ ≥ V <sub>CC</sub> - 0.2 V, $\overline{DS}$ ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0	-	20.0	-	30.0	mA
I <sub>DS</sub>	Deep-Sleep current	Max V <sub>CC</sub> , $\overline{CE}^{[11]}$ ≥ V <sub>CC</sub> - 0.2 V, $\overline{DS}$ ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0	-	8.0	-	22.0	μA

**Notes**

7. V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.
8. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for a V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for a V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for a V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.
9. This parameter is guaranteed by design and is not tested.
10. For  $\overline{DS}$  pin, V<sub>IH</sub> (min) is V<sub>CC</sub> - 0.2 V and V<sub>IL</sub> (max) is 0.2 V.
11. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and CE<sub>2</sub>. When  $\overline{CE}_1$  is LOW and CE<sub>2</sub> is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or CE<sub>2</sub> is LOW,  $\overline{CE}$  is HIGH.



## Capacitance

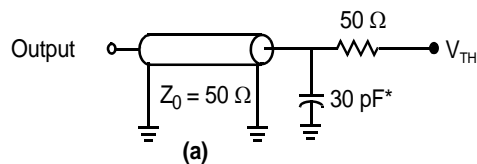
Parameter <sup>[12]</sup>	Description	Test Conditions	All packages	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> (typ)	10	pF
C <sub>OUT</sub>	I/O capacitance		10	pF

## Thermal Resistance

Parameter <sup>[12]</sup>	Description	Test Conditions	48-ball VFBGA	54-pin TSOP II	48-pin TSOP I	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	31.50	93.63	57.99	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		15.75	21.58	13.42	°C/W

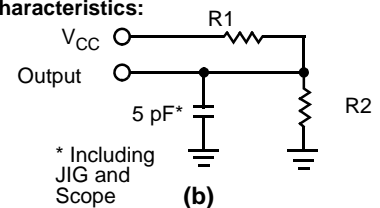
## AC Test Loads and Waveforms

Figure 6. AC Test Loads and Waveforms<sup>[13]</sup>

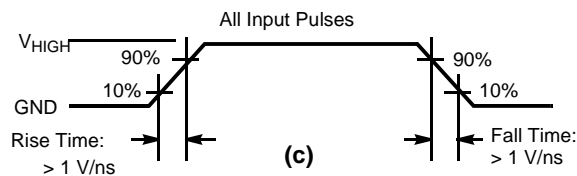


\* Capacitive Load Consists of all Components of the Test Environment

High-Z Characteristics:



\* Including JIG and Scope



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V <sub>TH</sub>	V <sub>CC</sub> /2	1.5	1.5	V
V <sub>HIGH</sub>	1.8	3.0	3.0	V

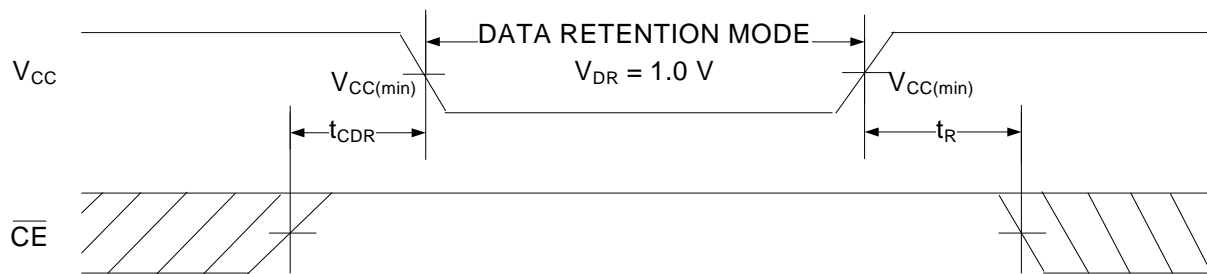
## Data Retention Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $\overline{DS} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	30.0	mA
$t_{CDR}^{[14]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[14]}$	Operation recovery time	$2.2\text{ V} < V_{CC} \leq 5.5\text{ V}$	10.0	–	ns
		$V_{CC} \leq 2.2\text{ V}$	15.0	–	ns

## Data Retention Waveform

Figure 7. Data Retention Waveform<sup>[15, 16]</sup>



### Notes

14. These parameters are guaranteed by design and are not tested.

15. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$ .

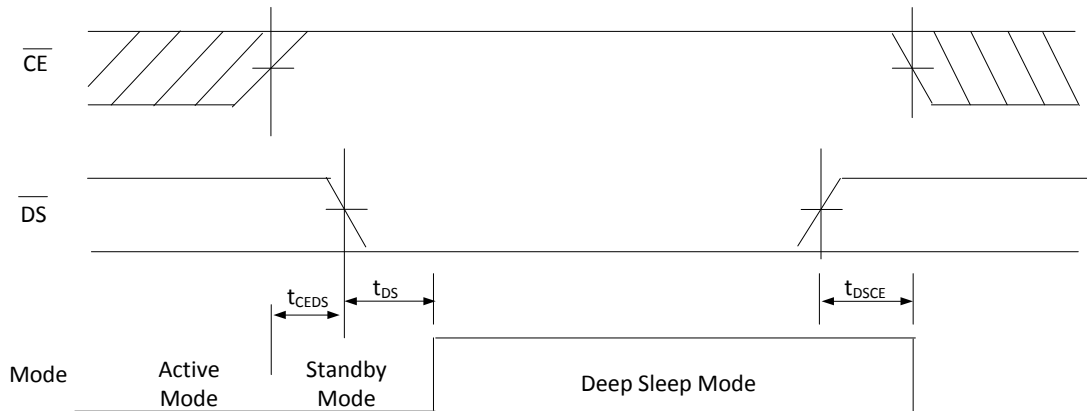
16. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

## Deep-Sleep Mode Characteristics

Over the Operating Range of -40 °C to +85 °C

Parameter	Description	Conditions	Min	Max	Unit
$I_{DS}$	Deep Sleep Mode current	$V_{CC} = V_{CC}(\text{max}), \overline{CE}^{[17]} \geq V_{CC} - 0.2 \text{ V}, \overline{DS} \leq 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	-	22	$\mu\text{A}$
$t_{CEDS}^{[17, 18]}$	Time between de-assertion of $\overline{CE}^{[17]}$ and assertion of $\overline{DS}$		100	-	ns
$t_{DS}^{[17, 18]}$	$\overline{DS}$ assertion to Deep Sleep mode transition time		-	1	ms
$t_{DSCE}^{[17, 18]}$	Time between de-assertion of $\overline{DS}$ and assertion of $\overline{CE}^{[17]}$		1	-	ms

**Figure 8. Active, Standby, and Deep-Sleep Operation Modes** <sup>[19]</sup>



### Notes

17. Address, data, and control lines should not toggle within  $t_{DS}$ . They should be fixed to one of the logic levels -  $V_{IH}$  or  $V_{IL}$ .

18. These parameters are guaranteed by design and are not tested.

19. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

## AC Switching Characteristics

Over the operating range of -40 °C to +85 °C

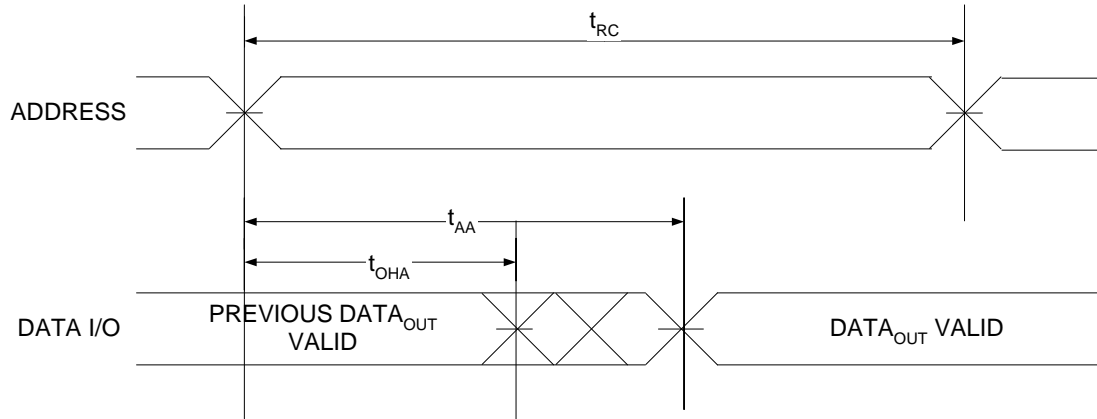
Parameter [20, 21]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{power}$	$V_{CC}$ (stable) to the first access [22, 23]	100.0	–	100.0	–	µs
$t_{RC}$	Read cycle time	10.0	–	15.0	–	ns
$t_{AA}$	Address to data valid / ERR valid	–	10.0	–	15.0	ns
$t_{OHA}$	Data / ERR hold from address change	3.0	–	3.0	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid / ERR valid	–	10.0	–	15.0	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid / ERR valid	–	5.0	–	8.0	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z [24, 25, 26]	0	–	1.0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z [24, 25, 26]	–	5.0	–	8.0	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z [24, 25, 26, 27]	3.0	–	3.0	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z [24, 25, 26, 27]	–	5.0	–	8.0	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up [23]	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down [23]	–	10.0	–	15.0	ns
$t_{DBE}$	Byte enable to data valid	–	5.0	–	8.0	ns
$t_{LZBE}$	Byte enable to low Z [24, 25]	0	–	1.0	–	ns
$t_{HZBE}$	Byte disable to high Z [24, 25]	–	5.0	–	8.0	ns
<b>Write Cycle</b> [28, 29]						
$t_{WC}$	Write cycle time	10.0	–	15.0	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end [27]	7.0	–	12.0	–	ns
$t_{AW}$	Address setup to write end	7.0	–	12.0	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7.0	–	12.0	–	ns
$t_{SD}$	Data setup to write end	5.0	–	8.0	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z [24, 25, 26]	3.0	–	3.0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z [24, 25, 26]	–	5.0	–	8.0	ns
$t_{BW}$	Byte Enable to End of Write	7.0	–	12.0	–	ns

### Notes

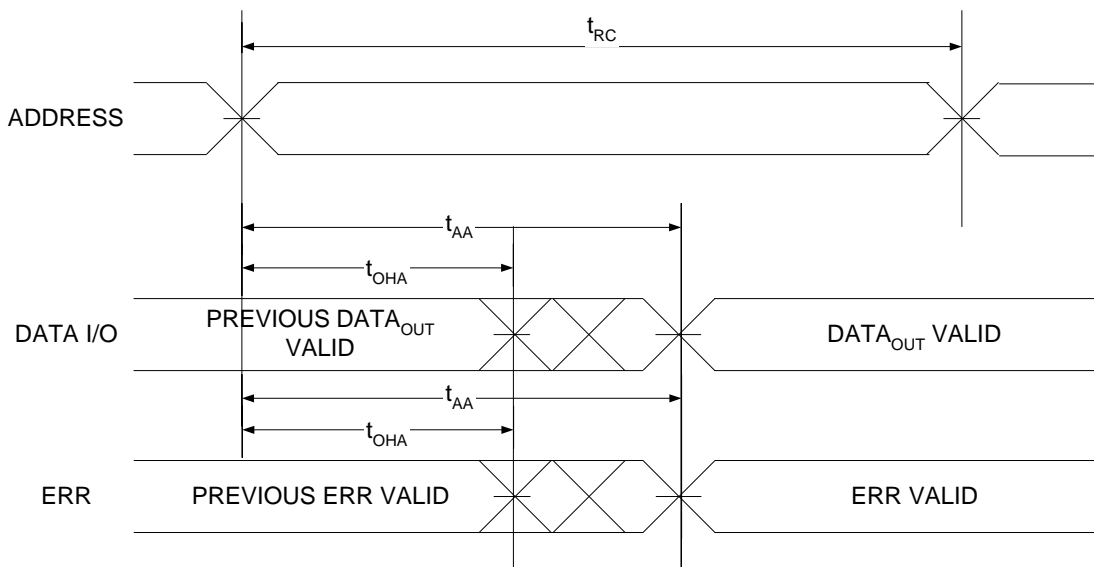
20. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V), and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use the output loading shown in part (a) of Figure 6 on page 8, unless specified otherwise.
21. DS must be HIGH for chip access. Refer to AN89371 for details.
22.  $t_{POWER}$  gives the minimum amount of time that the power supply is at stable  $V_{CC}$  until the first memory access is performed.
23. These parameters are guaranteed by design and are not tested.
24.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ , and  $t_{HZBE}$  are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 6 on page 8. Hi-Z, Lo-Z transition is measured  $\pm 200$  mV from steady state voltage.
25. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
26. Tested initially and after any design or process changes that may affect these parameters.
27. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . When  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW,  $\overline{CE}$  is HIGH.
28. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ , and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
29. The minimum write pulse width for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

**Figure 9. Read Cycle No. 1 of CY7S1061G (Address Transition Controlled)** [30, 31]



**Figure 10. Read Cycle No. 2 of CY7S1061GE (Address Transition Controlled)** [30, 31]

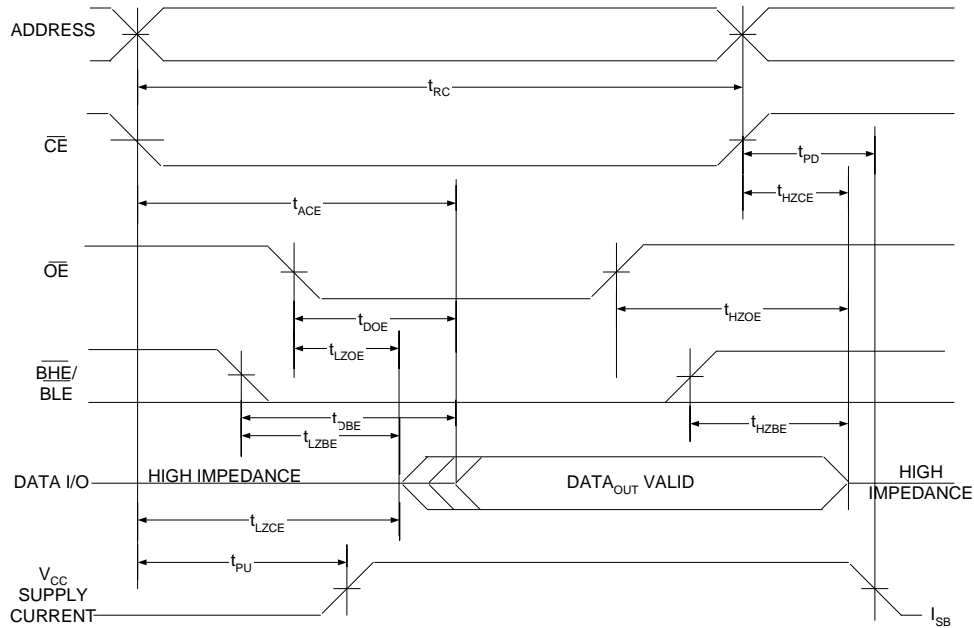


### Notes

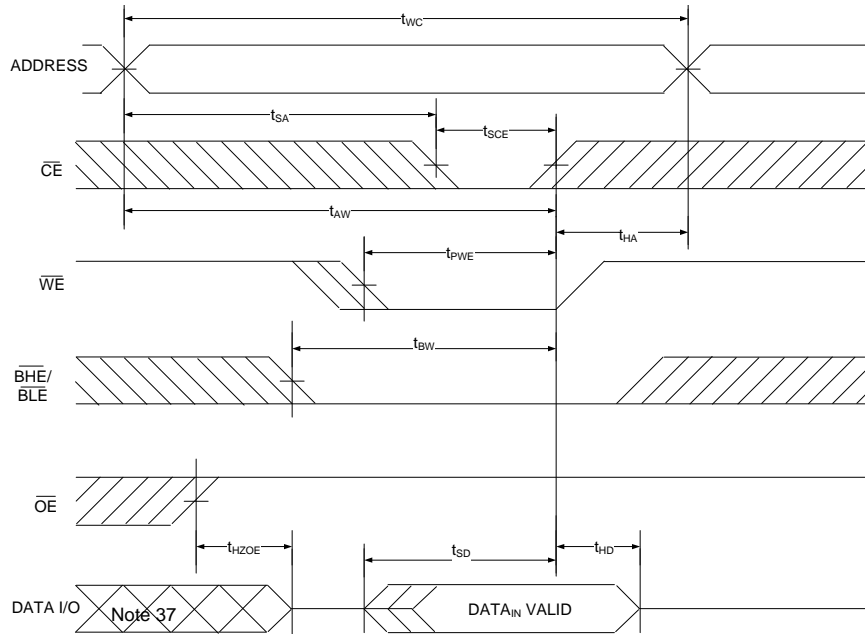
30. The device is continuously selected.  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ .  
31.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms** (continued)

**Figure 11. Read Cycle No. 3 (OE Controlled)** [32, 33, 34]



**Figure 12. Write Cycle No. 1 (CE Controlled)** [33, 35, 36]



**Notes**

- 32.  $\overline{WE}$  is HIGH for read cycle.
- 33. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 34. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.
- 35. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 36. Data I/O is in high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 37. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 13. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [38, 39, 40, 41]

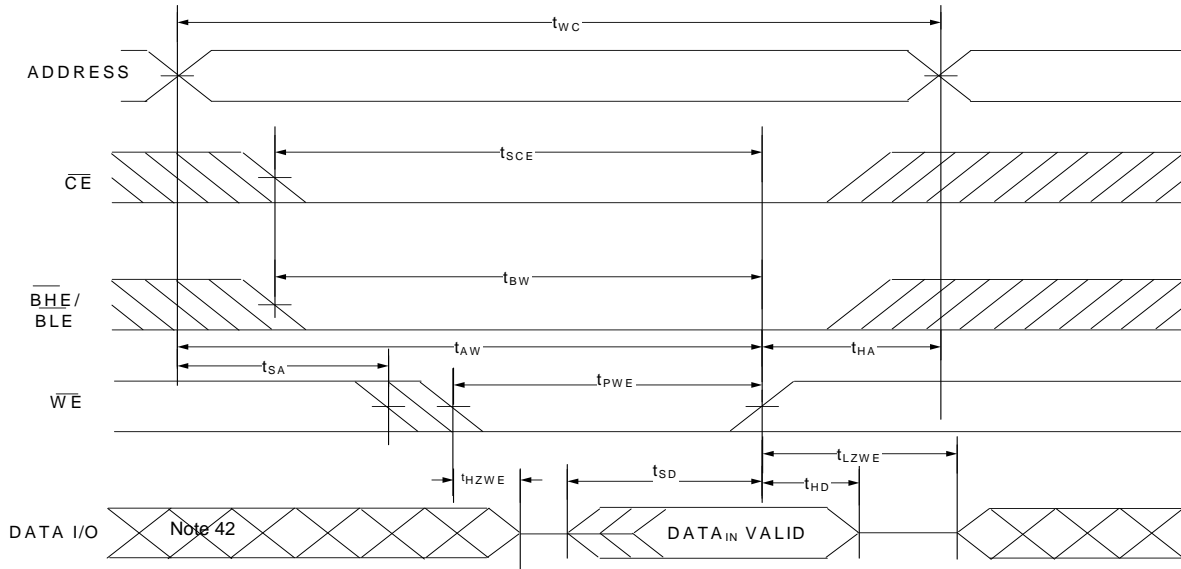
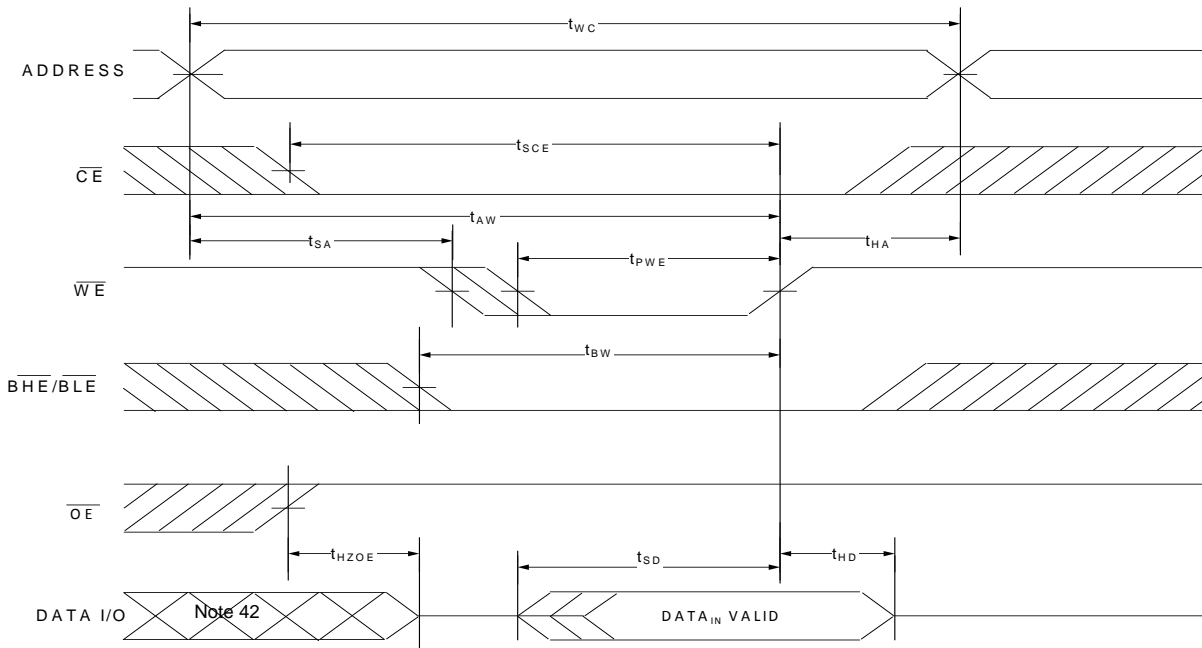


Figure 14. Write Cycle No. 3 ( $\overline{WE}$  controlled) [38, 40, 41]

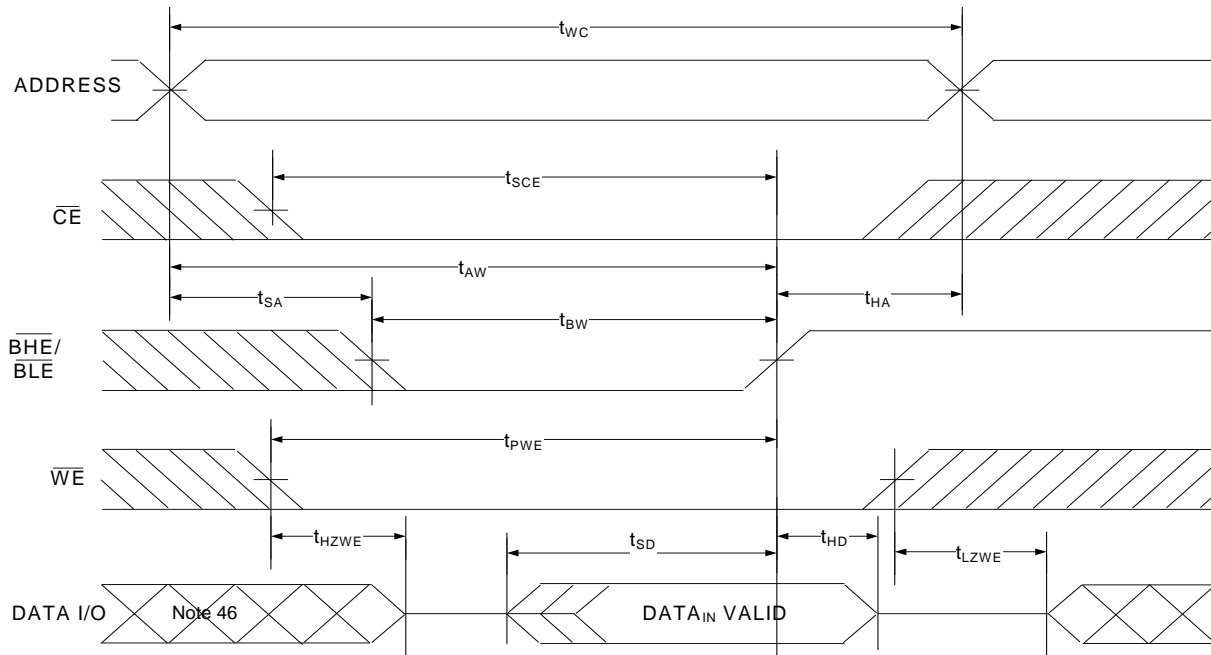


Notes

- 38. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 39. The minimum write pulse width for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 40. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 41. Data I/O is in high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 42. During this period, the I/Os are in output state. Do not apply input signals.

**Switching Waveforms** (continued)

**Figure 15. Write Cycle No. 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)** [43, 44, 45]



**Notes**

- 43. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
- 44. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$  and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{\text{IL}}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 45. Data I/O is in high-impedance state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$ , or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
- 46. During this period, the I/Os are in output state. Do not apply input signals.



**Truth Table**

$\overline{DS}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	H	X <sup>[47]</sup>	X <sup>[47]</sup>	X <sup>[47]</sup>	X <sup>[47]</sup>	High-Z	High-Z	Standby	Standby (I <sub>SB</sub> )
H	L	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
H	L	L	H	L	H	Data out	High-Z	Read lower bits only	Active (I <sub>CC</sub> )
H	L	L	H	H	L	High-Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
H	L	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
H	L	X	L	L	H	Data in	High-Z	Write lower bits only	Active (I <sub>CC</sub> )
H	L	X	L	H	L	High-Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
H	L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L <sup>[48]</sup>	H	X	X	X	X	High-Z	High-Z	Deep Sleep	Deep-Sleep Ultra Low Power (I <sub>DS</sub> )
L	L	X	X	X	X	–	–	Invalid mode <sup>[49]</sup>	–
H	L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

**ERR Output – CY7S1061GE**

Output <sup>[50]</sup>	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected or outputs disabled or Write operation

**Notes**

47. The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>.

48. V<sub>IL</sub> on  $\overline{DS}$  must be ≤ 0.2 V.

49. This mode does not guarantee data retention. Power cycling needs to be performed for the device to return to normal operation.

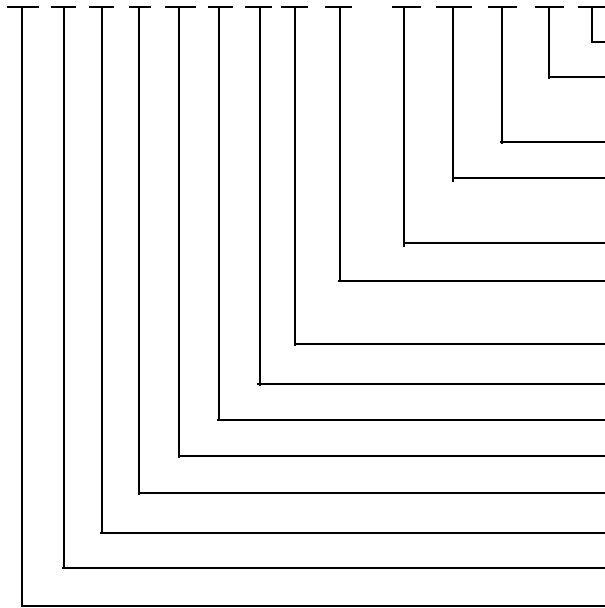
50. ERR is an Output pin. If not used, this pin should be left floating.

**Ordering Information**

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type All (Pb-free)	ERR Pin/Ball	Operating Range	
15	1.65 V–2.2 V	CY7S1061G18-15ZSXI	51-85160	54-pin TSOP II	No	Industrial	
		CY7S1061G18-15ZSXIT					
10	2.2 V–3.6 V	CY7S1061G30-10ZSXI	51-85160	54-pin TSOP II	No		
		CY7S1061G30-10ZSXIT					
		CY7S1061G30-10BVXI	51-85150	48-ball VFBGA	No		
		CY7S1061G30-10BVXIT					
		CY7S1061GE30-10BVXI			Yes		
		CY7S1061GE30-10BVXIT					
	4.5 V–5.5 V	48-pin TSOP I	CY7S1061G30-10ZXI	51-85183	48-pin TSOP I		No
			CY7S1061G30-10ZXIT				
			CY7S1061GE30-10ZXI			Yes	
			CY7S1061GE30-10ZXIT				
4.5 V–5.5 V	48-pin TSOP I	CY7S1061GE-10ZXI	51-85183	48-pin TSOP I	Yes		
		CY7S1061GE-10ZXIT					

**Ordering Code Definitions**

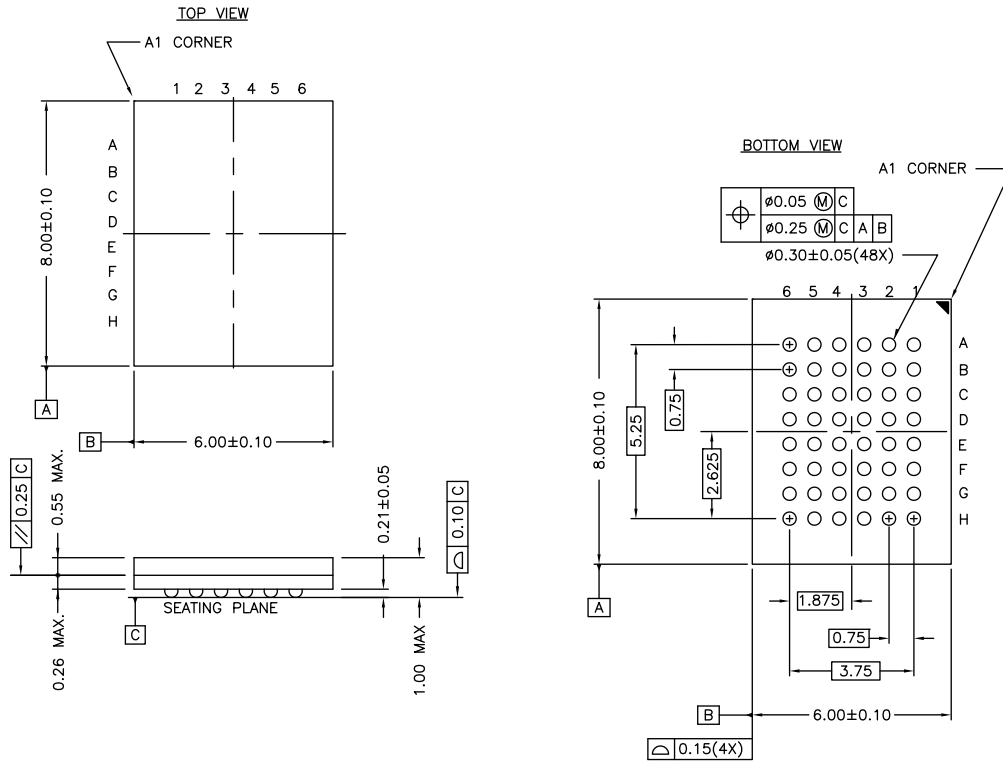
CY 7 S 1 06 1 G E 30 - 10 XX X I X



- X: Tape & Reel; T = Tape & Reel, Blank = Bulk
- Temperature Range:  
I = Industrial
- Pb-free
- Package Type: XX = BV or Z or ZS  
BV = 48-ball VFBGA; Z = 48-pin TSOP I; ZS = 54-pin TSOP II
- Speed: 10 ns
- Voltage Range:  
30 = 3-V typ; 18 = 1.8-V typ; no character = 5-V typ
- ERR output
- Revision Code "G": Process Technology – 65 nm
- Data width: 1 = x 16-bits
- Density: 06 = 16-Mbit
- Family Code: 1 = Fast Asynchronous SRAM family
- S = Deep-Sleep feature
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

Figure 16. 48-ball VFBGA (6 x 8 x 1.0 mm) BV48/BZ48 Package Outline



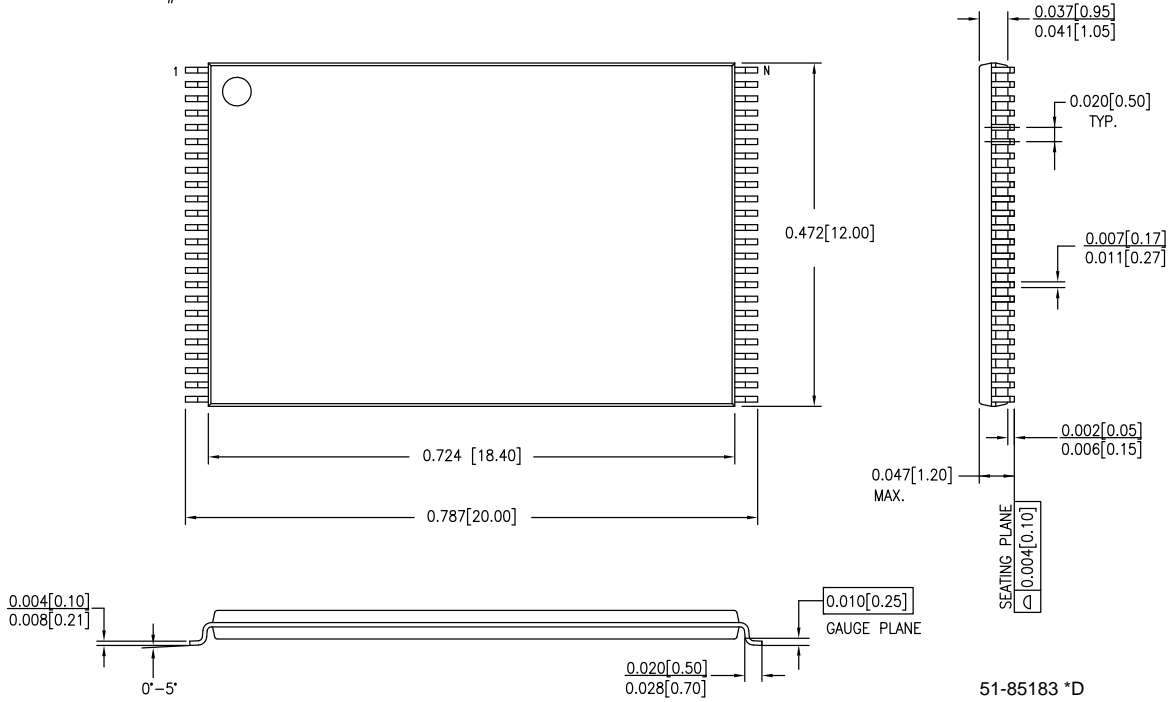
NOTE:  
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H

Package Diagrams (continued)

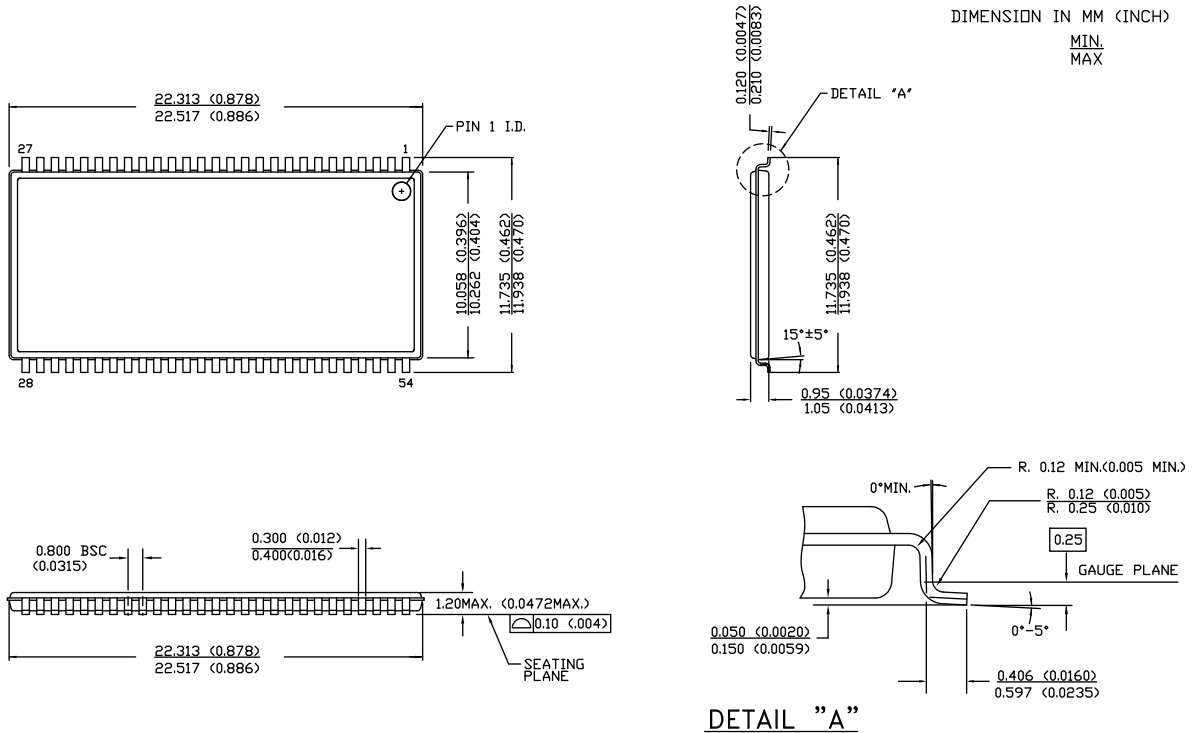
Figure 17. 48-pin TSOP I (12 x 18.4 x 1.0 mm) Z48A Package Outline

DIMENSIONS IN INCHES[MM] MIN.  
MAX.  
JEDEC # MO-142



Package Diagrams (continued)

Figure 18. 54-pin TSOP II (22.4 x 11.84 x 1.0 mm) Z54-II Package Outline



DETAIL "A"

51-85160 \*E

## Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/output
OE	Output Enable
SRAM	Static random access memory
TTL	Transistor-transistor logic
VFBGA	Very fine-pitch ball grid array
WE	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7S1061G/CY7S1061GE, 16-Mbit (1 M words x 16 bit) Static RAM with PowerSnooze™ and ECC				
Document Number: 001-79707				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*M	4791835	NILE	06/10/2015	Changed datasheet status to Final
*N	5436633	VINI	09/15/2016	Updated <a href="#">DC Electrical Characteristics</a> : Updated VOH values for the voltage range $V_{CC} = 2.7V$ to $3.6V$ . Updated Note <a href="#">7</a> . Updated <a href="#">Ordering Code Definitions</a> : Added Tape and Reel parts. Updated Copyright and Disclaimer.

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