PRELIMINARY

CY7C1049DV33

4-Mbit (512K x 8) Static RAM

Features

- **Pin- and function-compatible with CY7C1049CV33**
- **High speed**
  - **— t_{AA} = 8 ns**
- **Low active power**
  - **— I_{CC} = 90 mA @ 8 ns (Commercial)**
  - **— I_{CC} = 100 mA @ 8 ns (Industrial)**
- **Low CMOS standby power**
  - **— I_{SB2} = 10 mA**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Available in Lead-Free 36-lead (400-mil) Molded SOJ V36 and 44-pin TSOP II ZS44 packages**

Functional Description[1]

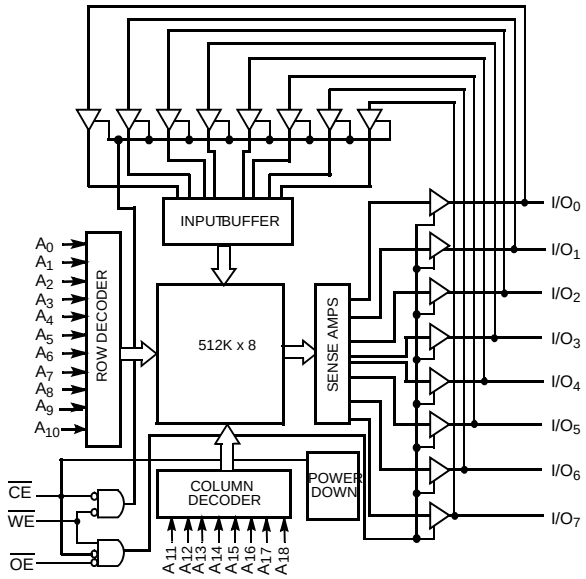
The CY7C1049DV33 is a high-performance CMOS Static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

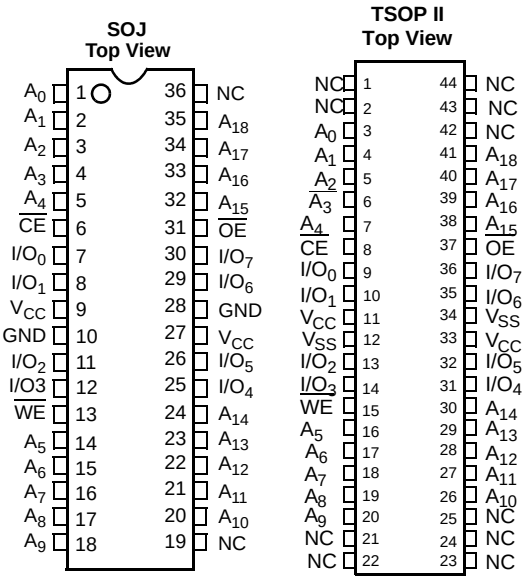
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1049DV33 is available in standard 400-mil-wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



Pin Configuration



Selection Guide

		-8	-10	-12	Unit
Maximum Access Time		8	10	12	ns
Maximum Operating Current	Commercial	90	80	75	mA
	Industrial	100	90	85	
Maximum CMOS Standby Current	Commercial/Industrial	10	10	10	mA

Note:
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.3V to +4.6V

DC Voltage Applied to Outputs in High-Z State[2].....–0.3V to V_{CC} + 0.3V

DC Input Voltage[2] .....–0.3V to V_{CC} + 0.3V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... .....>2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-8		-10		-12		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Com'l		90		80		75	mA
			Ind'l		100		90		85	
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}; V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l/Ind'l		20		20		20	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l/Ind'l		10		10		10	mA

Capacitance[3]

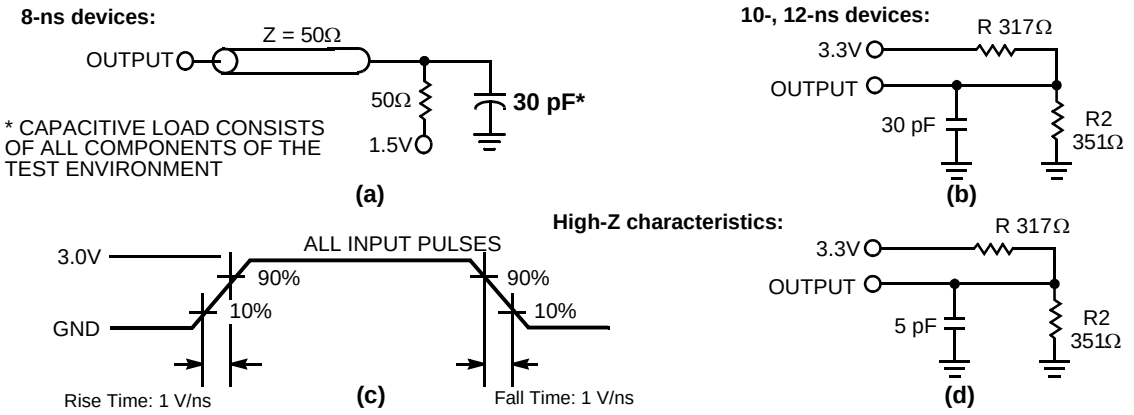
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance[3]

Parameter	Description	Test Conditions	All Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[3]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[3]		TBD	°C/W

Notes:
2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[4]



AC Switching Characteristics[5] Over the Operating Range

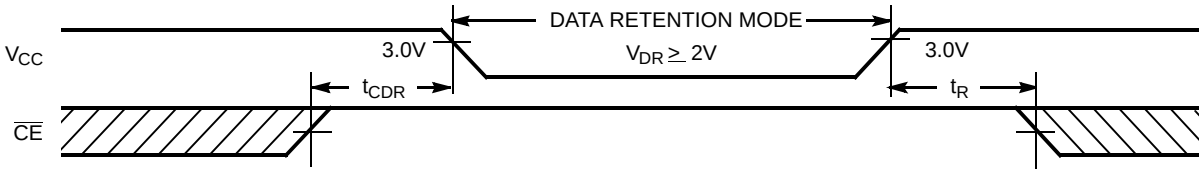
Parameter	Description	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{power}[6]	V_{CC}(typical) to the first access	100		100		100		µs
t_{RC}	Read Cycle Time	8		10		12		ns
t_{AA}	Address to Data Valid		8		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		4		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[7, 8]		4		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[7, 8]		4		5		6	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		8		10		12	ns
Write Cycle[9, 10]								
t_{WC}	Write Cycle Time	8		10		12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	6		7		8		ns
t_{AW}	Address Set-up to Write End	6		7		8		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		7		8		ns
t_{SD}	Data Set-up to Write End	4		5		6		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[8]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[7, 8]		4		5		6	ns

Notes:
4. AC characteristics (except High-Z) for 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V , and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
7. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
10. The minimum Write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions [12]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$,		10	mA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{CE} \geq V_{CC} - 0.3V$	0		ns
t_R[11]	Operation Recovery Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	t_{RC}		ns

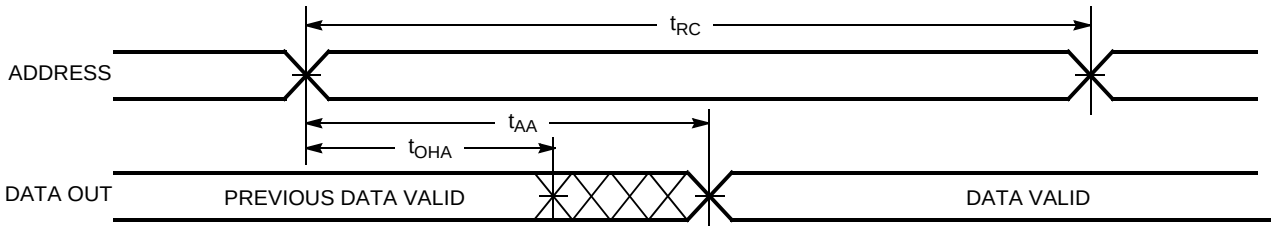
Data Retention Waveform



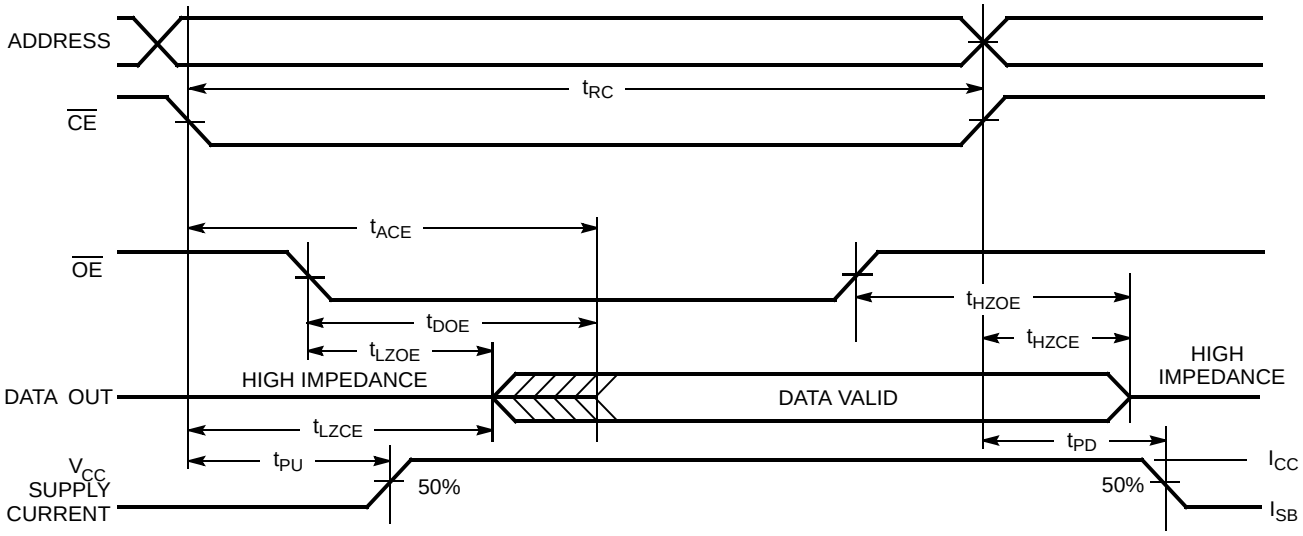
Notes:
11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\,\mu s$ or stable at $V_{CC(min.)} \geq 50\,\mu s$
12. No input may exceed V_{CC} + 0.3V.

Switching Waveforms

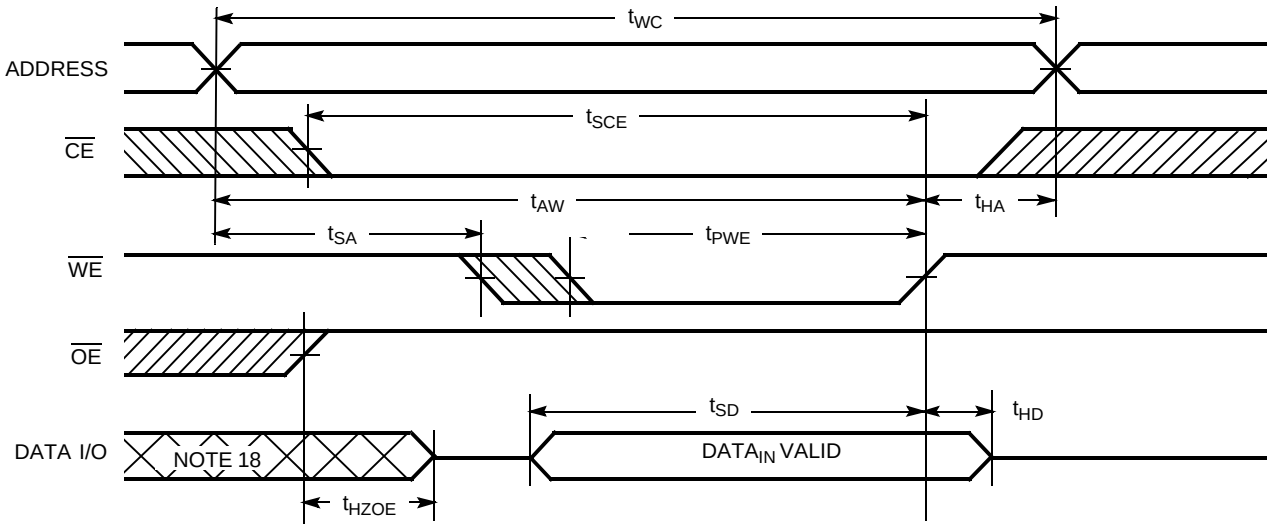
Read Cycle No. 1[13, 14]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]



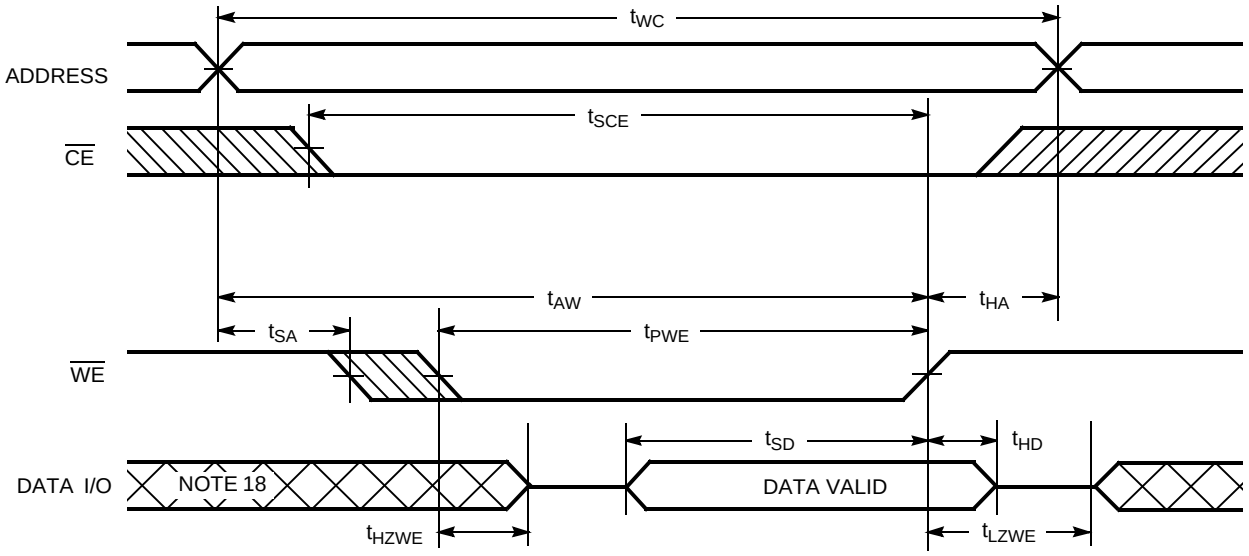
Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[16, 17]



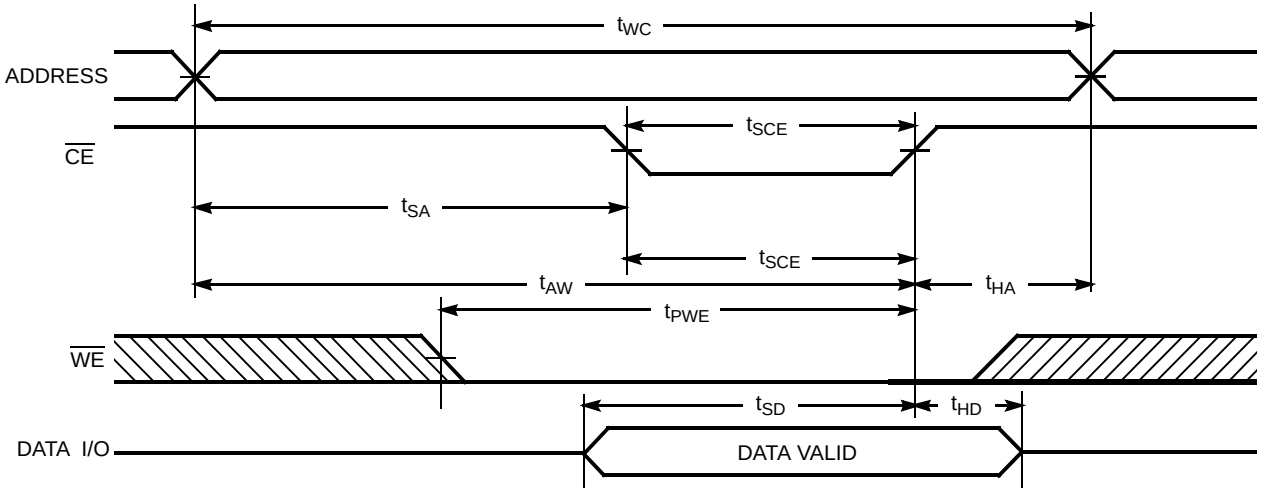
Notes:
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
14. $\overline{WE}$ is HIGH for Read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. Data I/O is high-impedance if $\overline{OE}$ = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
18. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms(continued)

Write Cycle No. 2 (WE Controlled, OE LOW)[17]



Write Cycle No. 3 (CE Controlled)[16, 17]



Truth Table

CE	OE	WE	I/O0–I/O7	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

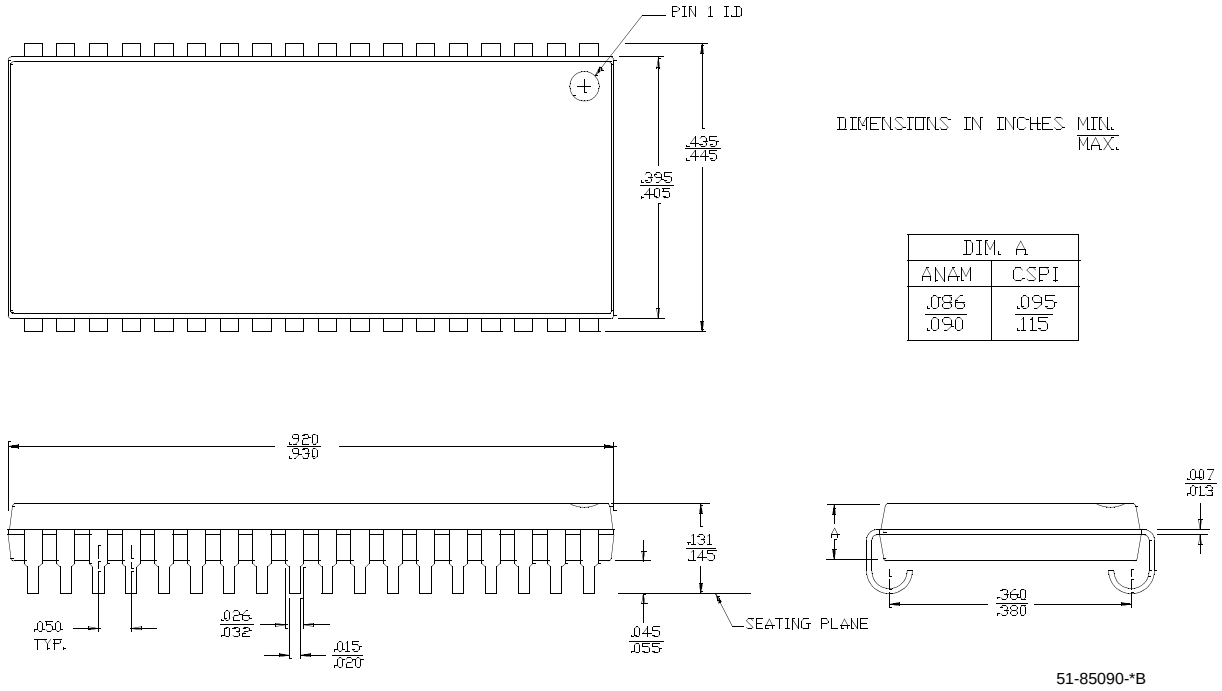
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1049DV33-8VXC	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1049DV33-8ZSXC	ZS44	44-pin TSOP II (Pb-Free)	
	CY7C1049DV33-8VXI	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1049DV33-8ZSXI	ZS44	44-pin TSOP II (Pb-Free)	
10	CY7C1049DV33-10VXC	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1049DV33-10ZSXC	ZS44	44-pin TSOP II (Pb-Free)	
	CY7C1049DV33-10VXI	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1049DV33-10ZSXI	ZS44	44-pin TSOP II (Pb-Free)	
12	CY7C1049DV33-12VXC	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1049DV33-12ZSXC	ZS44	44-pin TSOP II (Pb-Free)	
	CY7C1049DV33-12VXI	V36	36-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1049DV33-12ZSXI	ZS44	44-pin TSOP II (Pb-Free)	

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

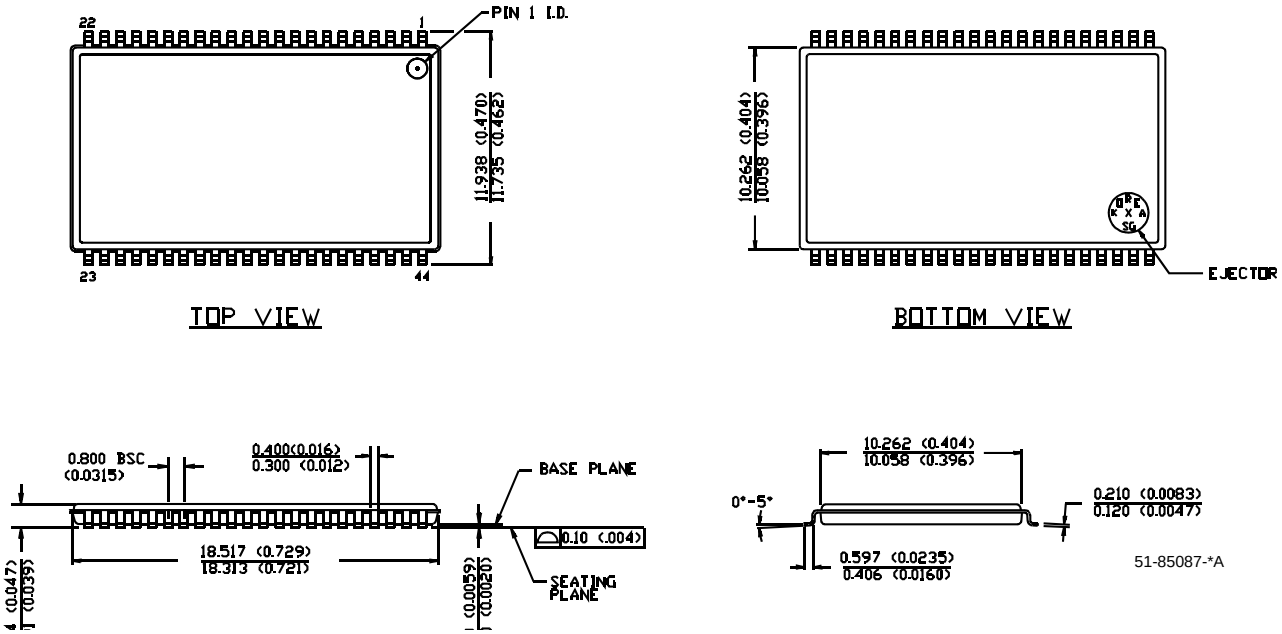
36-lead (400-mil) Molded SOJ V36



Package Diagrams(continued)

44-pin TSOP II ZS44

DIMENSION IN MM (INCH)
MAX
MIN



Document History Page

Document Title: CY7C1049DV33 4-Mbit (512K x 8) Static RAM Document Number: 38-05475				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Data sheet for C9 IPP
*A	233729	See ECN	SYT	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'ordering information'
*B	351096	See ECN	PCI	Changed from Advance to Preliminary Removed 20 ns Speed bin Corrected DC voltage (min) value in maximum ratings section from - 0.5 to - 0.3V Redefined I_{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 100, 80 and 67 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively I_{CC} (Ind'l): Changed from 80 and 67 mA to 90 and 85 mA for 10 and 12ns speed bins respectively Added $V_{IH(max)}$ spec in Note# 2 Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Data Retention Characteristics/Waveform and footnotes 11 and 12 Changed Package Diagram name from 44-pin TSOP II Z44 to 44-pin TSOP II ZS44 Changed part names from Z to ZS in the Ordering Information Table Added 8 ns parts in the Ordering Information Table Added Lead-Free Ordering Information Shaded Ordering Information Table