CY7C199CN

256 K (32 K × 8) Static RAM

Features

- Fast access time: 15 ns and 20 ns
- Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)
- complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Transistor transistor logic (TTL) compatible inputs and outputs
- 2.0 V data retention
- Low CMOS standby power
- Automated power down when deselected
- Available in Pb-free 28-pin Thin Small Outline Package (TSOP) I, 28-pin Molded Small Outline J-Lead (SOJ) and 28-pin DIP packages

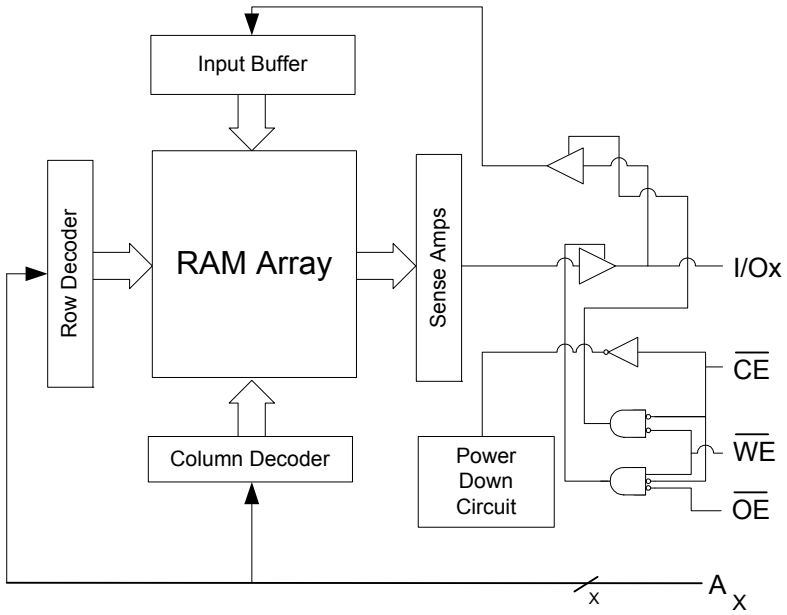
General Description [1]

The CY7C199CN is a high performance CMOS Asynchronous SRAM organized as 32K by 8 bits that supports an asynchronous memory interface. The device features an automatic power down feature that reduces power consumption when deselected.

See the "Truth Table" on page 4 in this data sheet for a complete description of read and write modes.

The CY7C199CN is available in Pb-free 28-pin TSOP I, 28-pin Molded SOJ and 28-pin DIP package(s).

Logic Block Diagram



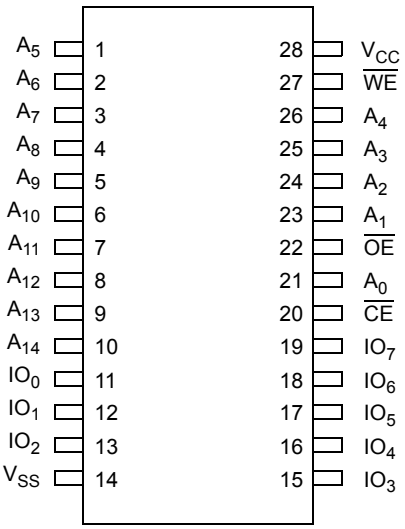
Product Portfolio

	–15	–20	Unit
Maximum access time	15	20	ns
Maximum operating current	80	75	mA
Maximum CMOS standby current (low power)	500	500	µA

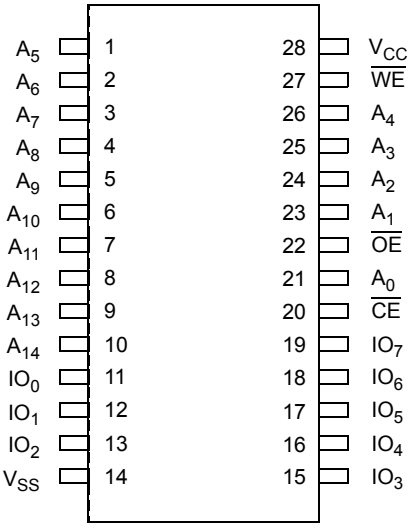
Contents

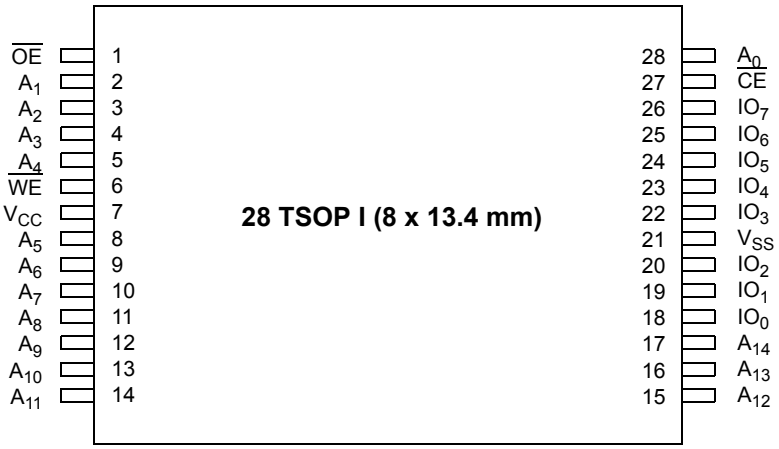
Pin Layout and Specifications

28 DIP



28 SOJ





28 TSOP I (8 x 13.4 mm)

Note
1. For best practices recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Pin Description

Pin	Type	Description	DIP	SOJ	TSOP I
A_X	Input	Address inputs	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26	2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 28
$\overline{CE}$	Control	Chip rnable	20	20	27
IO_X	Input or Output	Data input outputs	11, 12, 13, 15, 16, 17, 18, 19	11, 12, 13, 15, 16, 17, 18, 19	18, 19, 20, 22, 23, 24, 25, 26
$\overline{OE}$	Control	Output rnable	22	22	1
V_{CC}	Supply	Power (5.0V)	28	28	7
V_{SS}	Supply	Ground	14	14	21
$\overline{WE}$	Control	Write enable	27	27	6

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	IOx	Mode	Power
H	X	X	High-Z	Deselect/Power down	Stand by (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs disabled	Active (I_{CC})

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Value	Unit
T_{STG}	Storage temperature	–65 to +150	°C
T_{AMB}	Ambient temperature with power applied (that is, case temperature)	–55 to +125	°C
V_{CC}	Core Supply voltage relative to V_{SS}	–0.5 to +7.0	V
V_{IN}, V_{OUT}	DC voltage applied to any pin relative to V_{SS}	–0.5 to V_{CC} + 0.5	V
I_{OUT}	Output short-circuit current	20	mA
V_{ESD}	Static discharge voltage (in accordance with MIL-STD-883, Method 3015)	> 2001	V
I_{LU}	Latch-up current	> 200	mA

Operating Range

Range	Ambient Temperature (T_A)	Voltage Range (V_{CC})
Commercial	0 °C to 70 °C	5.0 V ± 10%
Industrial	–40 °C to 85 °C	5.0 V ± 10%

DC Electrical Characteristics

Over the Operating Range (–15, –20) [2]

Parameter	Description	Condition		–15		–20		Unit
				Min	Max	Min	Max	
V_{IH}	Input HIGH voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage			–0.5	0.8	–0.5	0.8	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	–	0.4	V
I_{CC}	V_{CC} Operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = F_{max} = $1/t_{RC}$		–	80	–	75	mA
I_{SB1}	Automatic $\overline{CE}$ power down current TTL inputs	Max V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{max}		–	30	–	30	mA
			L	–	10	–	10	mA
I_{SB2}	Automatic $\overline{CE}$ Power down current CMOS Inputs	Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3 V, $V_{IN} \geq V_{CC}$ – 0.3 V, or $V_{IN} \leq$ 0.3 V, f = 0		–	10	–	10	mA
			L	–	500	–	500	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, output disabled		–5	+5	–5	+5	µA
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–5	+5	–5	+5	µA

Capacitance [3]

Parameter	Description	Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		8	

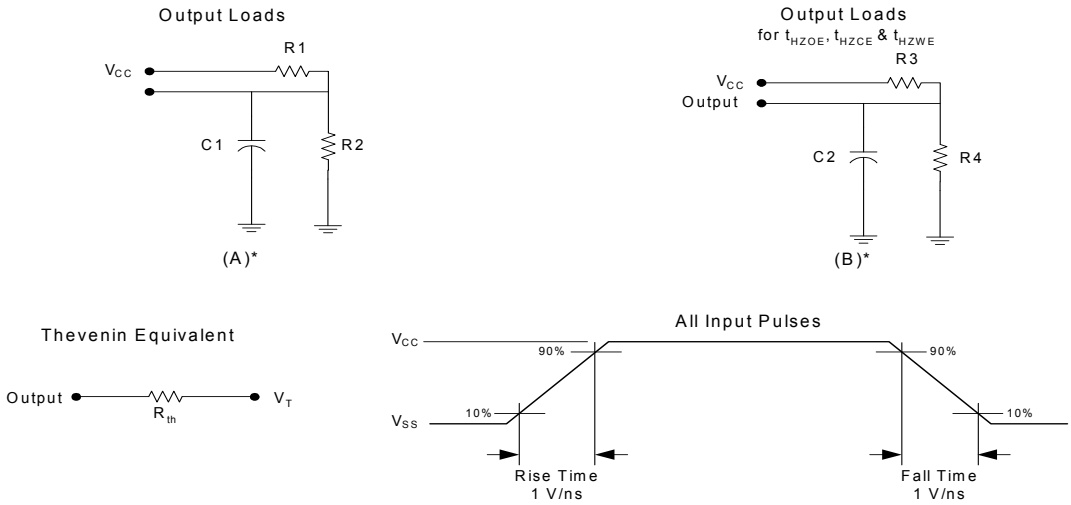
Thermal Resistance [3]

Parameter	Description	Conditions	TSOP I	SOJ	DIP	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 square inch, two–layer printed circuit board	88.6	79	69.33	°C/W
Θ_{JC}	Thermal resistance (junction to case)		21.94	41.42	31.62	

Note

2. V_{IL} (min) = –2.0 V for pulse durations of less than 20 ns.

AC Test Loads



* including scope and jig capacitance

AC Test Conditions

Parameter	Description	Nom	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

Note
3. Tested initially and after any design or process change that may affect these parameters.

AC Electrical Characteristics [4]

Parameter	Description	–15		–20		Unit
		Min	Max	Min	Max	
t_{RC}	Read cycle time	15	–	20	–	ns
t_{AA}	Address to data valid	–	15	–	20	ns
t_{OHA}	Data hold from address change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to data valid	–	15	–	20	ns
t_{DOE}	$\overline{OE}$ to data valid	–	7	–	9	ns
t_{LZOE}	$\overline{OE}$ to Low-Z [5]	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ to High-Z [5, 6]	–	7	–	9	ns
t_{LZCE}	$\overline{CE}$ to Low-Z [5]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High-Z [5, 6]	–	7	–	9	ns
t_{PU}	$\overline{CE}$ to Power Up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power Down	–	15	–	20	ns
t_{WC}	Write Cycle Time [7]	15	–	20	–	ns
t_{SCE}	$\overline{CE}$ to write end	10	–	15	–	ns
t_{AW}	Address setup to write end	10	–	15	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	9	–	15	–	ns
t_{SD}	Data setup to write end	9	–	10	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [5, 6]	–	7	–	10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [5]	3	–	3	–	ns

Data Retention Characteristics [8]

Parameter	Description	Condition	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	150	µA
t_{CDR}	Chip deselect to data retention time		0	–	ns
t_R	Operation recovery time		200	–	µs

Notes

4. Test Conditions are based on a transition time of 3 ns or less and timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
6. t_{HZOE}, t_{HZCE}, t_{HZWE} are specified as in part (b) of the “” on page 5. Transitions are measured ± 200 mV from steady state voltage.
7. The internal memory write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing must be referenced to the leading edge of the signal that terminates the write.
8. L-version only.

Timing Waveforms

Data Retention Waveform

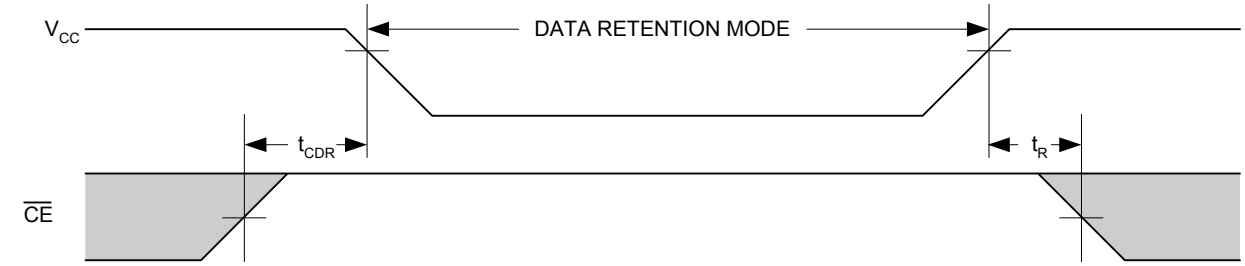
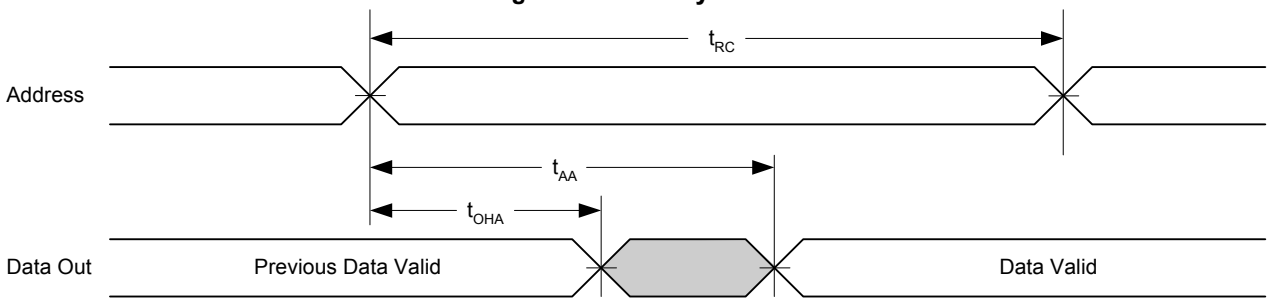


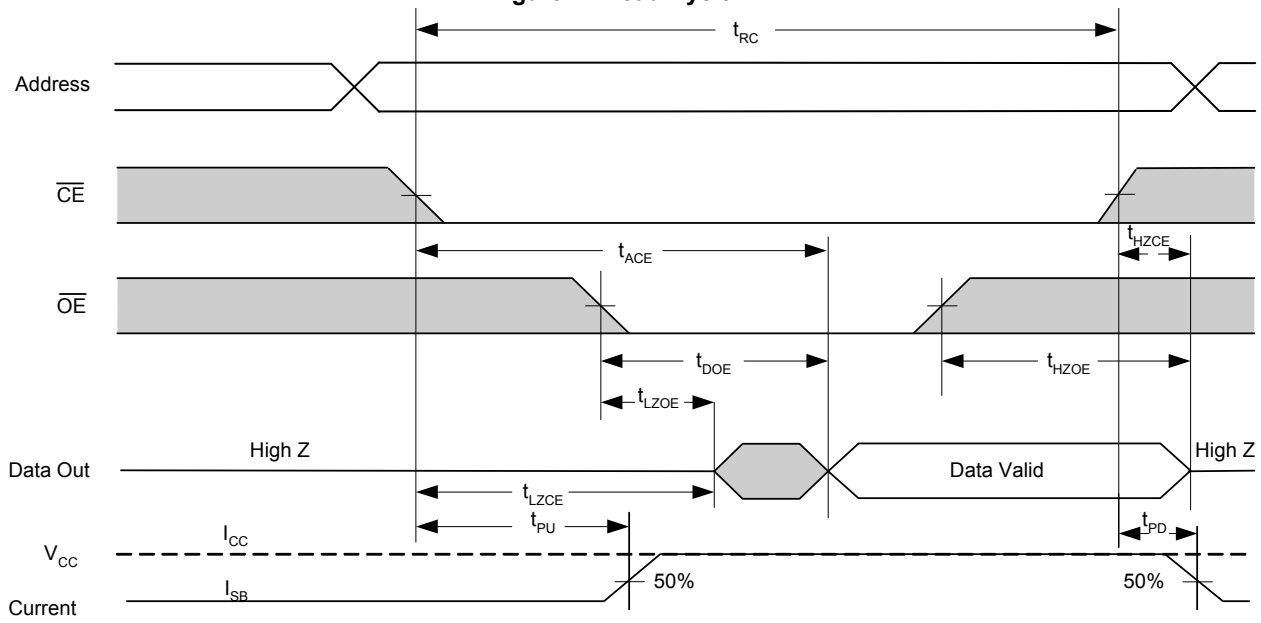
Figure 1. Read Cycle 1 [9, 10]



Notes
9. Device is continuously selected. $\overline{OE}$ = V_{IL} = $\overline{CE}$.
10. $\overline{WE}$ is HIGH for read cycle.

Timing Waveforms *(continued)*

Figure 2. Read Cycle 2 [11, 12]



Notes
11. This cycle is $\overline{OE}$ controlled and $\overline{WE}$ is HIGH read cycle.
12. Address valid before or similar with $\overline{CE}$ transition LOW.

Timing Waveforms *(continued)*

Figure 3. Write Cycle 1 ($\overline{WE}$ controlled) [13, 14, 15]

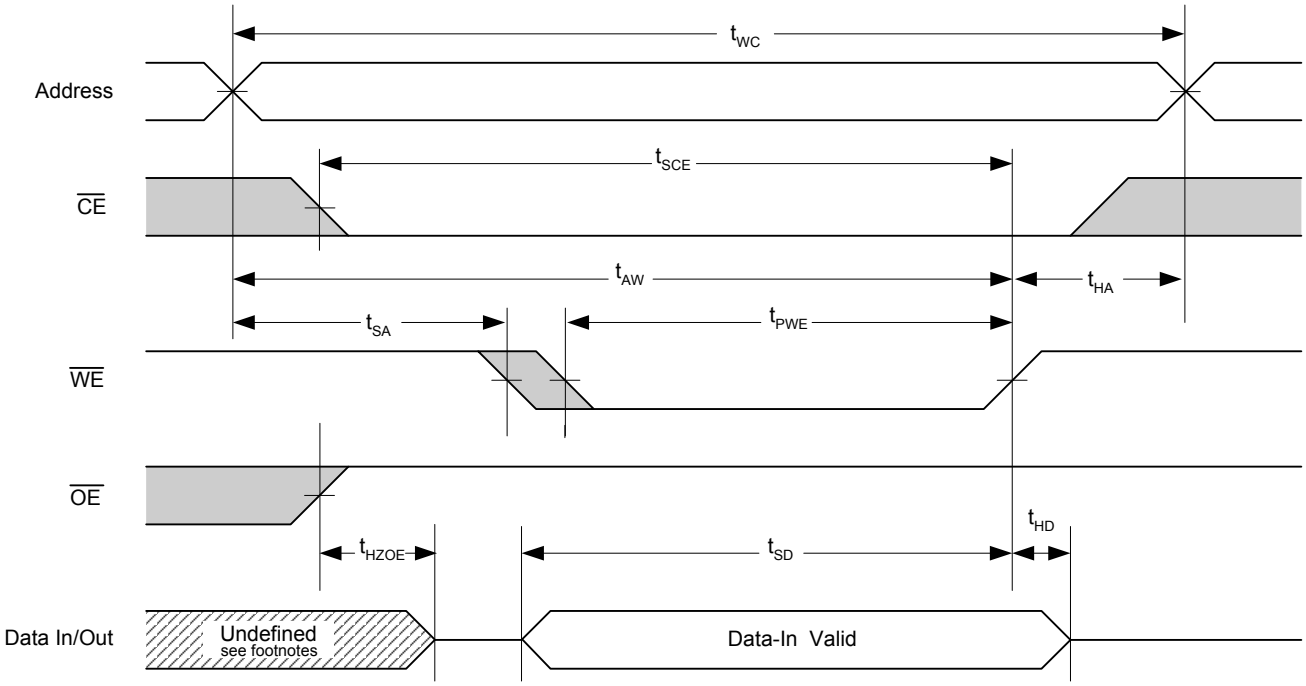
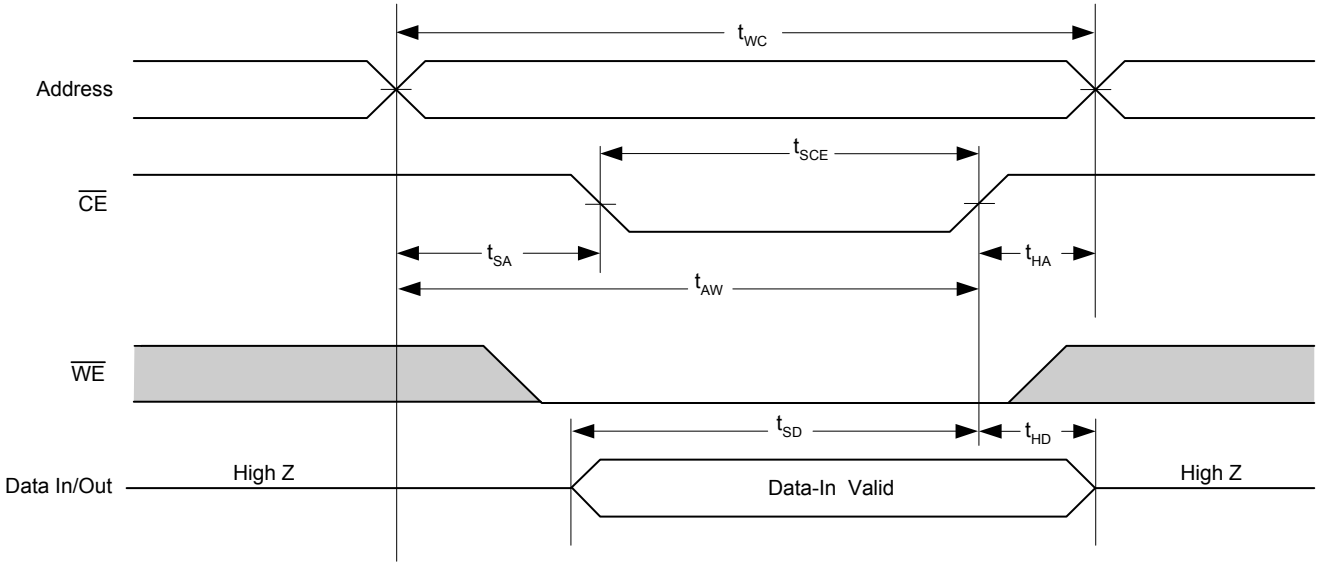


Figure 4. Write Cycle 2 ($\overline{CE}$ controlled) [14, 16, 17]

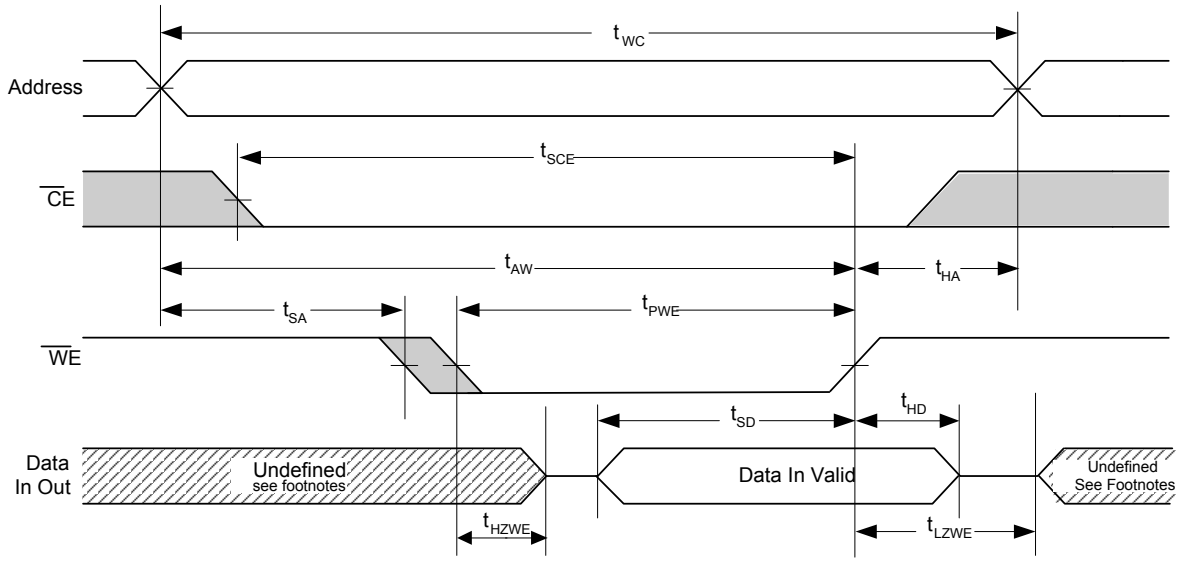


Notes

13. This cycle is $\overline{WE}$ controlled, $\overline{OE}$ is HIGH during write.
14. Data in and/or out is high impedance if $\overline{OE}$ = V_{IH}.
15. During this period the IOs are in output state and input signals must not be applied.
16. This cycle is $\overline{CE}$ controlled.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Timing Waveforms *(continued)*

Figure 5. Write Cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ low) [18]



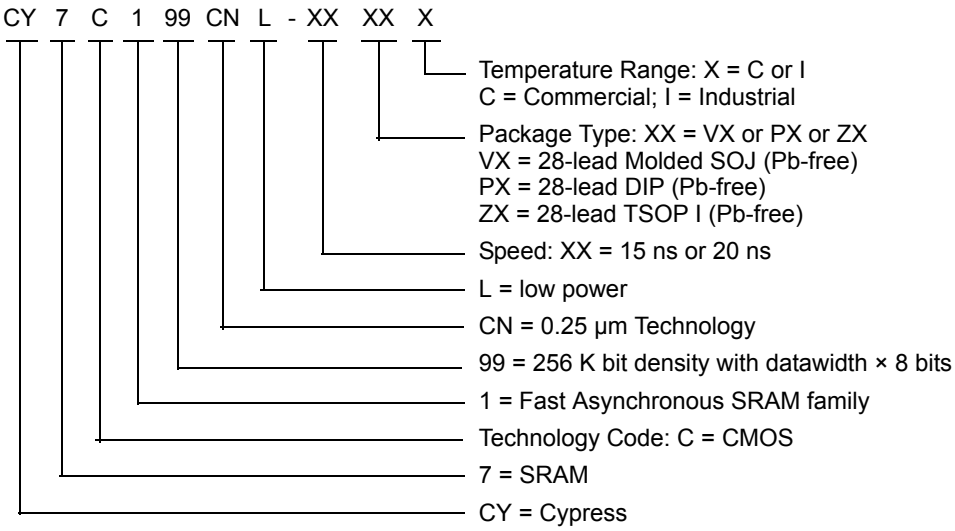
Note
18. The cycle is $\overline{WE}$ controlled, $\overline{OE}$ LOW. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.

Ordering Information

Contact local sales representative regarding availability of these parts.

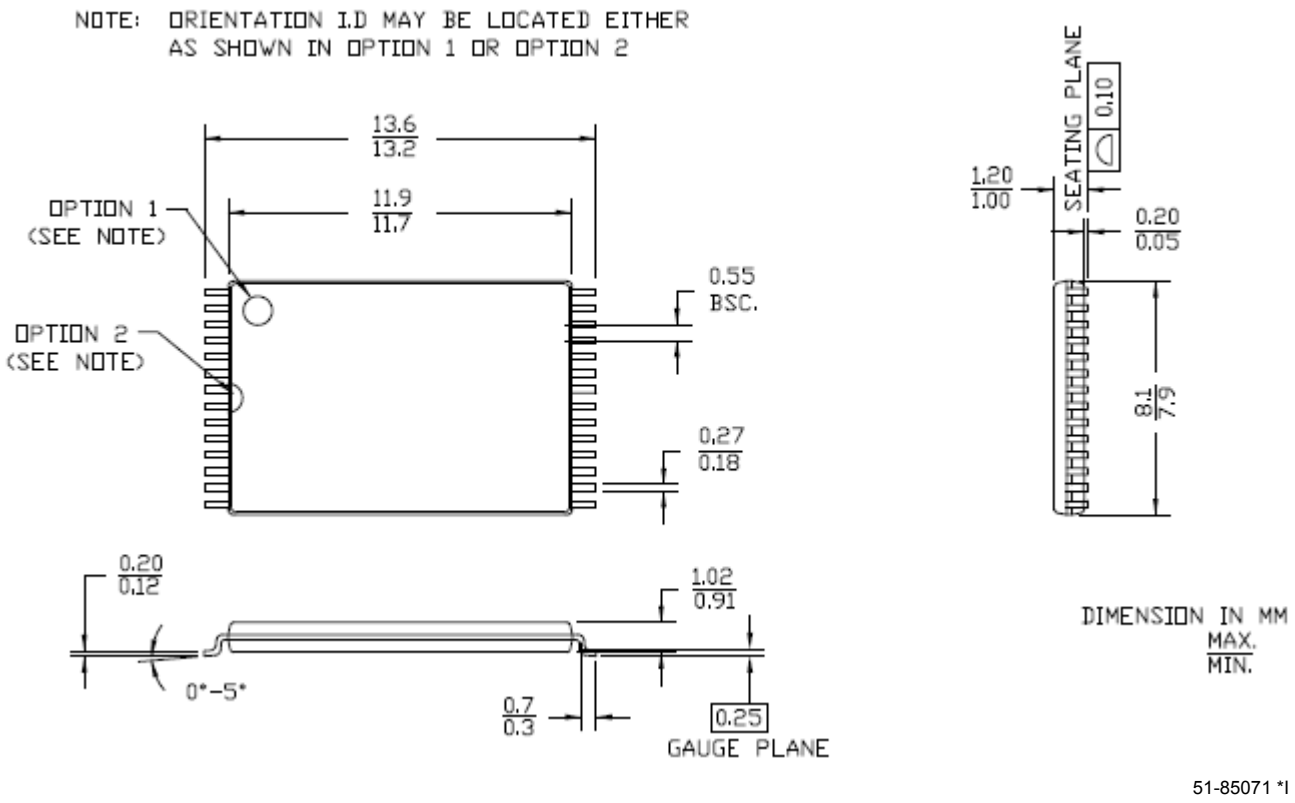
Speed (ns)	Ordering Code	Package Diagram	Package Type	Power Option	Operating Range
15	CY7C199CN-15PXC	51-85014	28 DIP (6.9 x 35.6 x 3.5 mm), Pb-free	Standard	Commercial
	CY7C199CN-15VXC	51-85031	28-Pin (300-Mil) Molded SOJ, Pb-free	Standard	Commercial
	CY7C199CNL-15VXI	51-85031	28-Pin (300-Mil) Molded SOJ, Pb-free	Low Power	Industrial
20	CY7C199CN-20ZXI	51-85071	28 TSOP I (8 x 13.4 mm), Pb-free	Standard	Industrial

Ordering Code Definitions



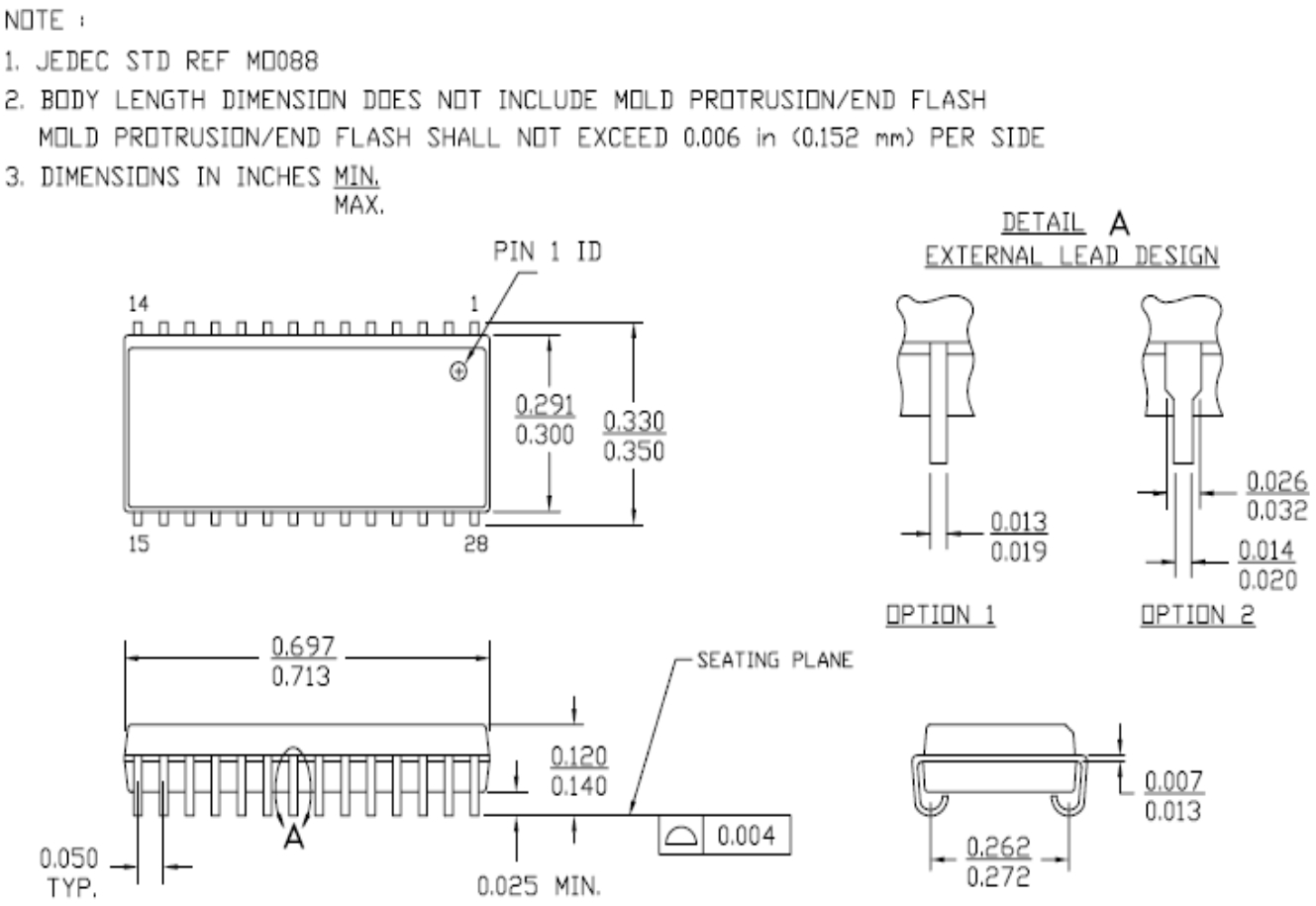
Package Diagrams

Figure 6. 28-pin TSOP I (8 x 13.4 mm), 51-85071



Package Diagrams *(continued)*

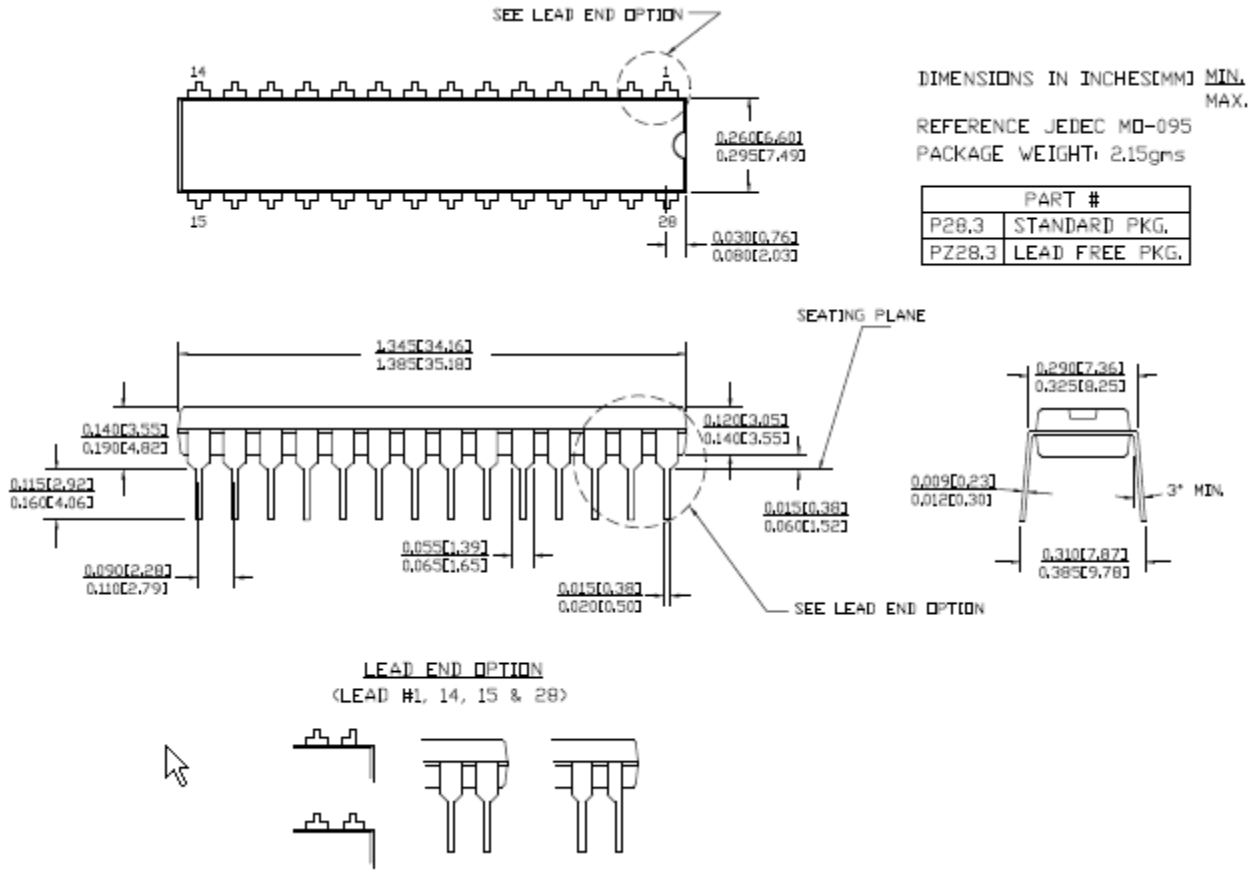
Figure 7. 28-pin (300 Mil) Molded SOJ, 51-85031



51-85031 *D

Package Diagrams *(continued)*

Figure 8. 28-pin (300 Mil) PDIP, 51-85014



51-85014 *E

Acronyms

Acronym	Description
CE	chip enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	output enable
SRAM	Static random access memory
SOJ	Small Outline J-Lead
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts

Document History Page

Document Title: CY7C199CN, 256 K (32 K × 8) Static RAM Document Number: 001-06435				
Revision	**ECN.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	430363	See ECN	NXR	New Data Sheet
*A	684342	See ECN	VKN	Added Automotive-A Information Updated Ordering Information Table
*B	839904	See ECN	VKN	Added t_{DOE} spec for Automotive-A part in AC Electrical characteristics table
*C	2896044	03/19/2010	NXR	Updated Ordering Information Table Updated Package Diagram
*D	3108898	12/13/2010	PRAS	Added Ordering Code Definitions.
*E	3198636	03/17/11	PRAS	Dislodged Automotive device information to 001-67737 Updated template and styles.
*F	3246329	05/04/2011	PRAS	Addtional information on ISB1, ISB2 with respect to L parts

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