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CY7C344B

32-Macrocell MAX® EPLD

Features

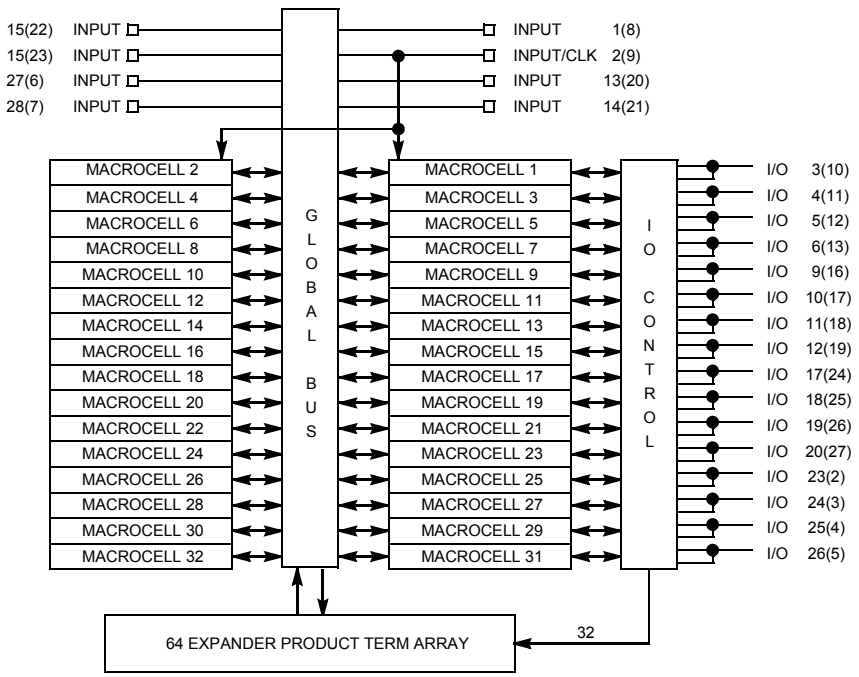
- **High-performance, high-density replacement for TTL, 74HC, and custom logic**
- **32 macrocells, 64 expander product terms in one LAB**
- **8 dedicated inputs, 16 I/O pins**
- **Advanced 0.65-micron CMOS EPROM technology to increase performance**
- **28-pin, 300-mil DIP, cerDIP or 28-pin HLCC, PLCC package**

Functional Description

Available in a 28-pin, 300-mil DIP or windowed J-leaded ceramic chip carrier (HLCC), the CY7C344B represents the densest EPLD of this size. Eight dedicated inputs and 16 bidirectional I/O pins communicate to one logic array block. In the CY7C344B LAB there are 32 macrocells and 64 expander product terms. When an I/O macrocell is used as an input, two expanders are used to create an input path. Even if all of the I/O pins are driven by macrocell registers, there are still 16 "buried" registers available. All inputs, macrocells, and I/O pins are interconnected within the LAB.

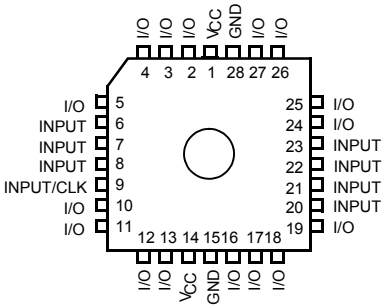
The speed and density of the CY7C344B makes it a natural for all types of applications. With just this one device, the designer can implement complex state machines, registered logic, and combinatorial "glue" logic, without using multiple chips. This architectural flexibility allows the CY7C344B to replace multichip TTL solutions, whether they are synchronous, asynchronous, combinatorial, or all three.

Logic Block Diagram[1]

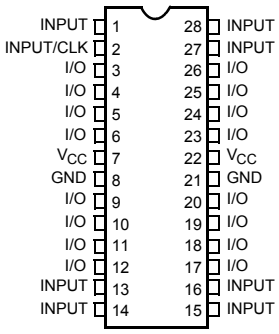


Pin Configurations

HLCC Top View



CerDIP Top View



Selection Guide

	7C344B-15	7C344B-20	7C344B-25	Unit
Maximum Access Time	15	20	25	ns

Note:
1. Number in () refers to J-leaded packages.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +135°C

Ambient Temperature with Power Applied.....-65°C to +135°C

Maximum Junction Temperature (Under Bias)..... 150°C

Supply Voltage to Ground Potential[2].....–2.0V to +7.0V

DC Output Current, per Pin[2].....–25 mA to +25 mA

DC Input Voltage[2].....–2.0V to +7.0V

Operating Range[3]

Range	Ambient Temperature	V_{CC}
Commercial	–0°C to +70°C	5V ±5%
Industrial	–40°C to +85°C	5V ±10%

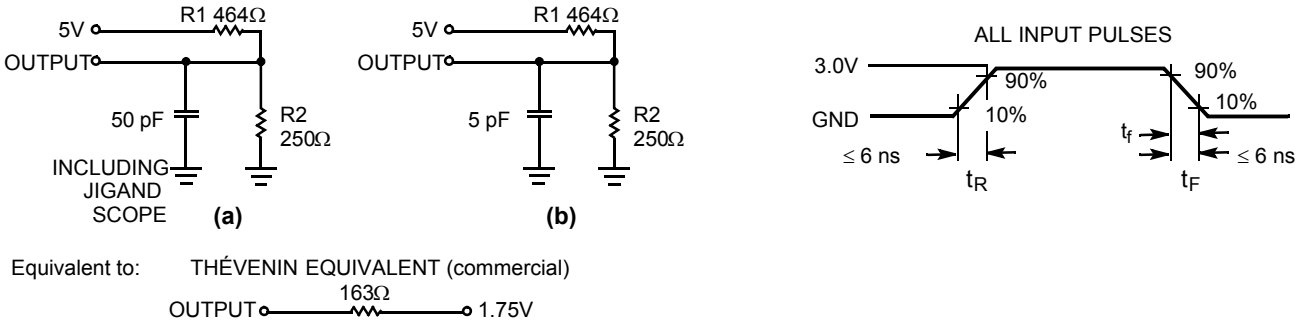
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage	Maximum V_{CC} rise time is 10 ms	4.75(4.5)	5.25(5.5)	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA DC[4]	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA DC[4]		0.45	V
V_{IH}	Input HIGH Level		2.0	V_{CC}+0.3	V
V_{IL}	Input LOW Level		–0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}	–10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND	–40	+40	µA
t_R	Recommended Input Rise Time			100	ns
t_F	Recommended Input Fall Time			100	ns

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz	12	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT (commercial)

Notes:

2. Minimum DC input is –0.3V. During transactions, the inputs may undershoot to –2.0V or overshoot to 7.0V for input currents less then 100 mA and periods shorter than 20 ns.
3. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
4. The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.

Design Recommendations

Operation of the devices described herein with conditions above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C344B contains circuitry to protect device pins from high-static voltages or electric fields; however, normal precautions should be taken to avoid applying any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay.

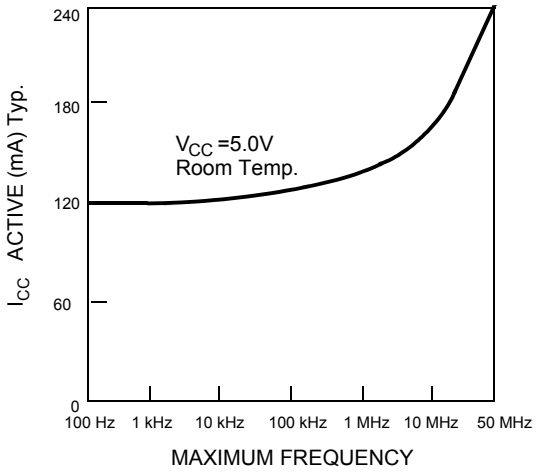
When calculating synchronous frequencies, use t_{SU} if all inputs are on the input pins. When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{SU}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{SU})$ is the lowest frequency. The lowest of these frequencies is the maximum data-path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins.

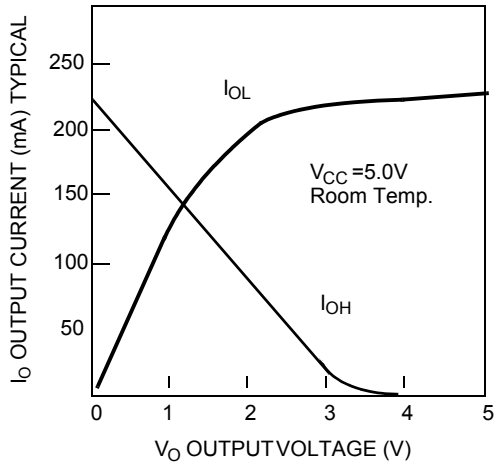
When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data-path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

Typical I_{CC} vs. f_{MAX}



Output Drive Current



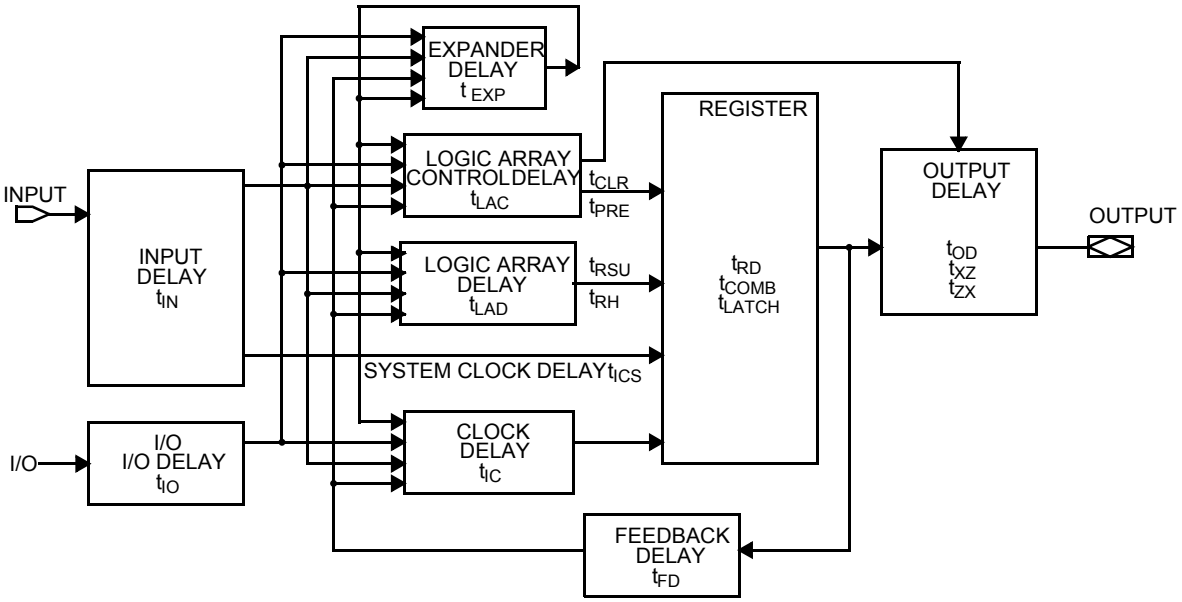


Figure 1. CY7C344B Timing Model

External Synchronous Switching Characteristics Over Operating Range

Parameter	Description		7C344B-15		7C344B-20		7C344B-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[5]	Com'l/Ind		15		20		25	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[5]	Com'l/Ind		15		20		25	ns
t_{SU}	Global Clock Set-up Time	Com'l/Ind	9		12		15		ns
t_{CO1}	Synchronous Clock Input to Output Delay[5]	Com'l/Ind		10		12		15	ns
t_{H}	Input Hold Time from Synchronous Clock Input	Com'l/Ind	0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	Com'l/Ind	6		7		8		ns
t_{WL}	Synchronous Clock Input LOW Time	Com'l/Ind	6		7		8		ns
f_{MAX}	Maximum Register Toggle Frequency[6]	Com'l/Ind	83.3			71.4		62.5	MHz
t_{CNT}	Minimum Global Clock Period	Com'l/Ind		13		16		20	ns
t_{ODH}	Output Data Hold Time After Clock	Com'l/Ind	1		1		1		ns
f_{CNT}	Maximum Internal Global Clock Frequency[7]	Com'l/Ind	76.9		62.5		50		MHz

Notes:
5. C1 = 35 pF
6. The f_{MAX} values represent the highest frequency for pipeline data.
7. This parameter is measured with a 32-bit counter programmed into each LAB.

External Asynchronous Switching Characteristics Over Operating Range

Parameter	Description		7C344B-15		7C344B-20		7C344B-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[5]	Com'l/Ind		15		18		22	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input	Com'l/Ind	5		6		8		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l/Ind	5		6		8		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[8]	Com'l/Ind	6		7		9		ns
t_{AWL}	Asynchronous Clock Input LOW Time[8]	Com'l/Ind	7		9		11		ns
t_{ACNT}	Minimum Internal Array Clock Frequency	Com'l/Ind		13		16		20	ns
f_{ACNT}	Maximum Internal Array Clock Frequency[7]	Com'l/Ind	76.9		62.5		50		MHz

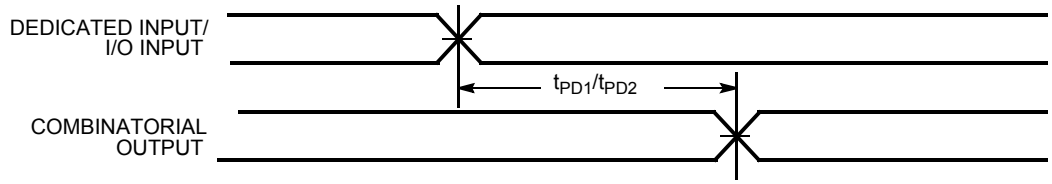
Typical Internal Switching Characteristics Over Operating Range

Parameter	Description		7C344B-15		7C344B-20		7C344B-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l/Ind		3		5		7	ns
t_{IO}	I/O Input Pad and Buffer Delay	Com'l/Ind		3		5		7	ns
t_{EXP}	Expander Array Delay	Com'l/Ind		8		10		15	ns
t_{LAD}	Logic Array Data Delay	Com'l/Ind		7		10		13	ns
t_{LAC}	Logic Array Control Delay	Com'l/Ind		4		4		4	ns
t_{OD}	Output Buffer and Pad Delay[5]	Com'l/Ind		4		4		4	ns
t_{ZX}	Output Buffer Enable Delay[5]	Com'l /Ind		7		7		7	ns
t_{XZ}	Output Buffer Disable Delay[5]	Com'l/Ind		7		7		7	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	Com'l/Ind	4		4		5		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l/Ind	5		8		10		ns
t_{LATCH}	Flow-Through Latch Delay	Com'l/Ind		1		1		1	ns
t_{RD}	Register Delay	Com'l/Ind		1		1		1	ns
t_{COMB}	Transparent Mode Delay	Com'l/Ind		1		1		1	ns
t_{IC}	Asynchronous Clock Logic Delay	Com'l/Ind		7		8		10	ns
t_{ICS}	Synchronous Clock Delay	Com'l/Ind		2		2		3	ns
t_{FD}	Feedback Delay	Com'l/Ind		1		1		1	ns
t_{PRE}	Asynchronous Register Preset Time	Com'l/Ind		5		6		9	ns
t_{CLR}	Asynchronous Register Clear Time	Com'l/Ind		5		6		9	ns

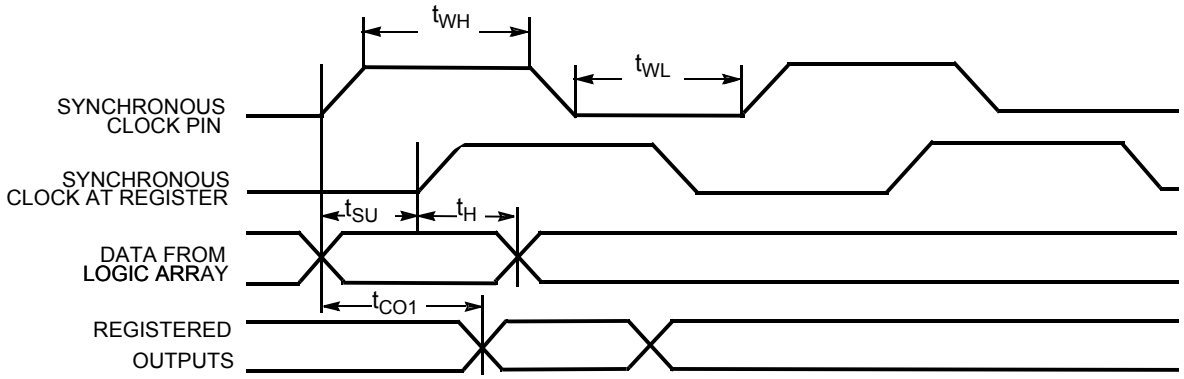
Note:
8. This parameter is measured with a positive-edge-triggered clock at the register. For the negative-edge clocking, the t_{ACH} and t_{ACL} parameter must be swapped.

Switching Waveforms

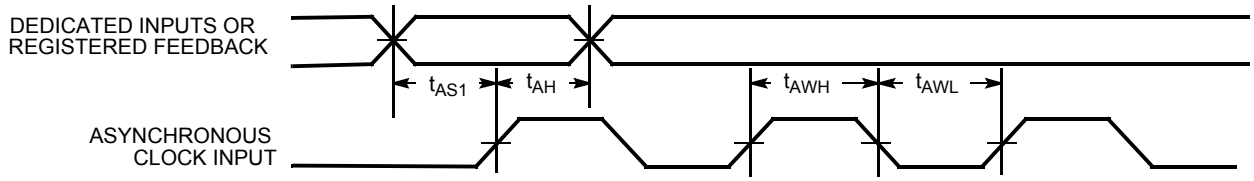
External Combinatorial



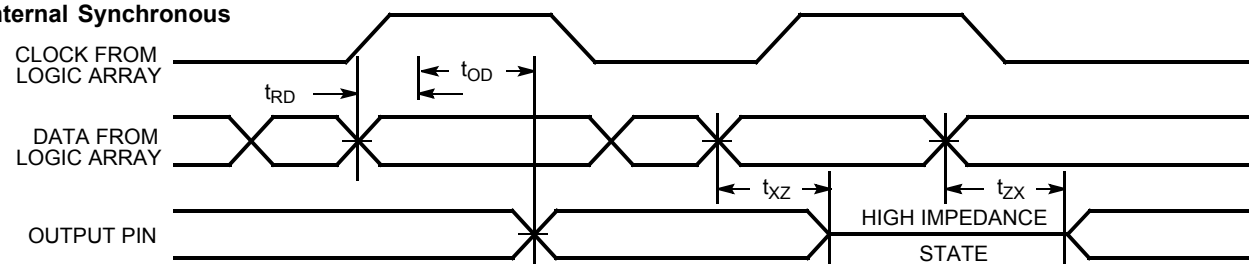
External Synchronous



External Asynchronous

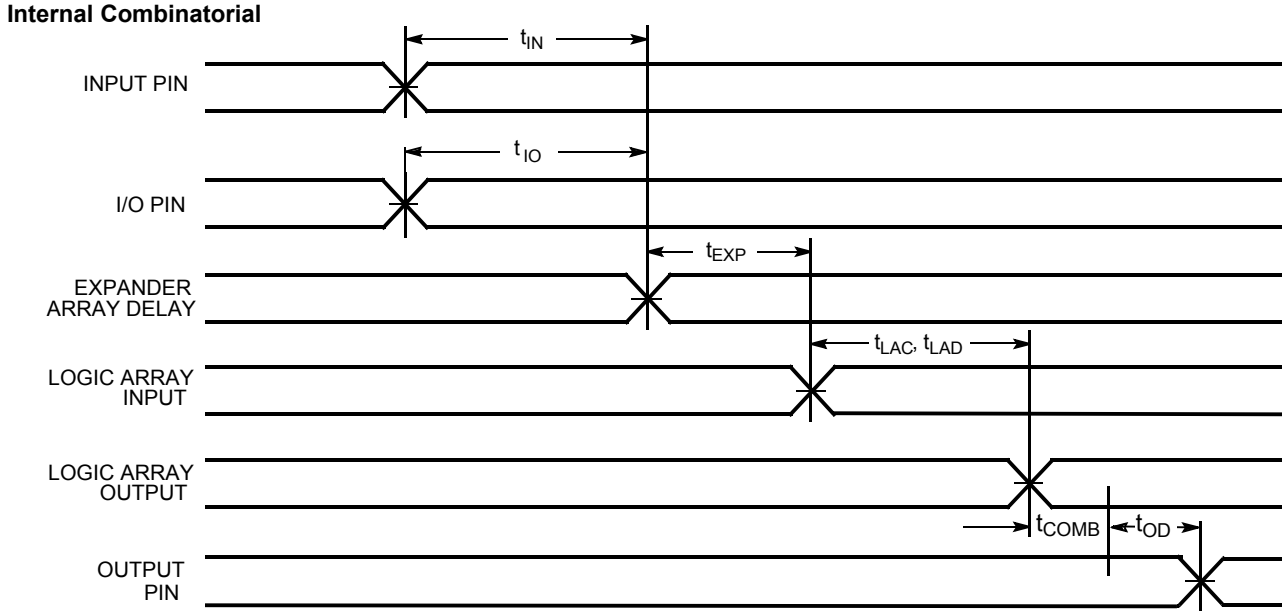


Internal Synchronous

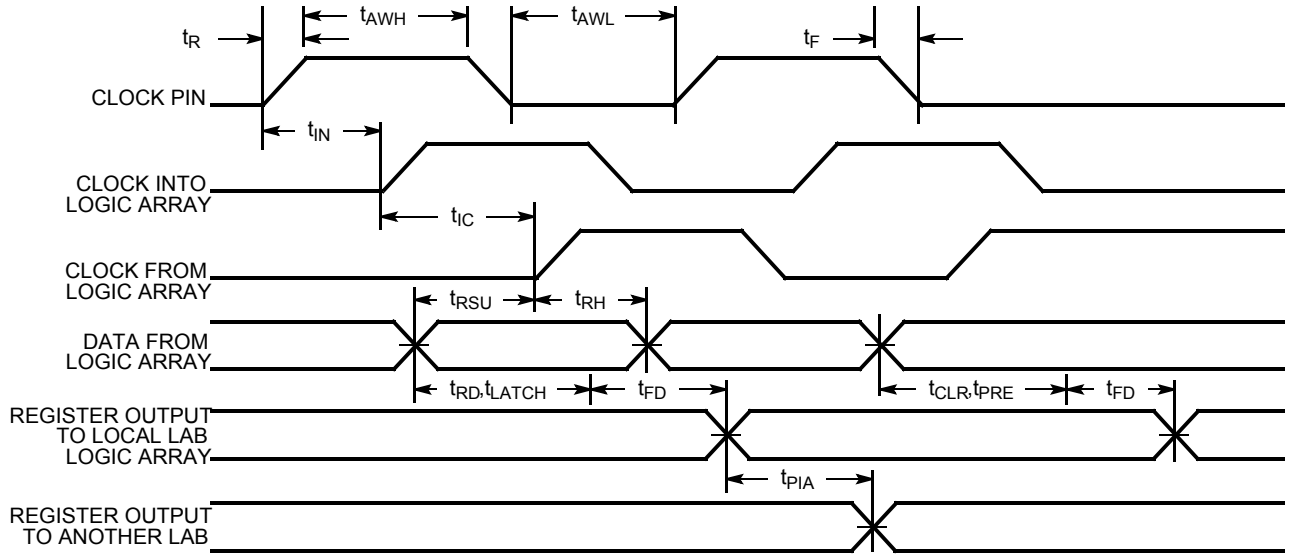


Switching Waveforms (continued)

Internal Combinatorial

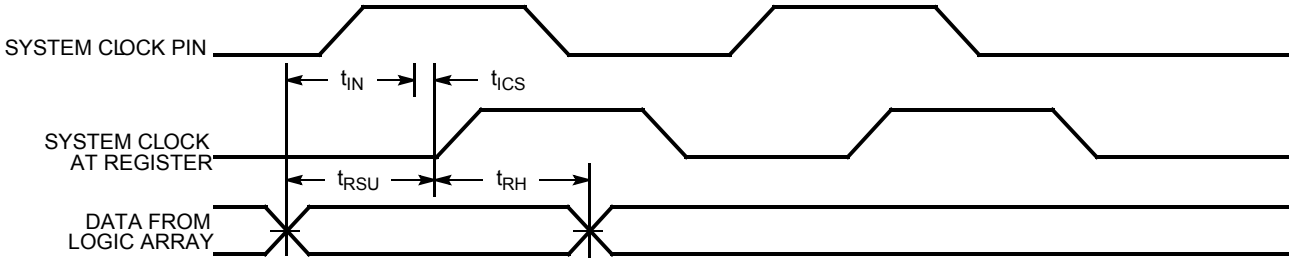


Internal Asynchronous



Switching Waveforms (continued)

Internal Synchronous

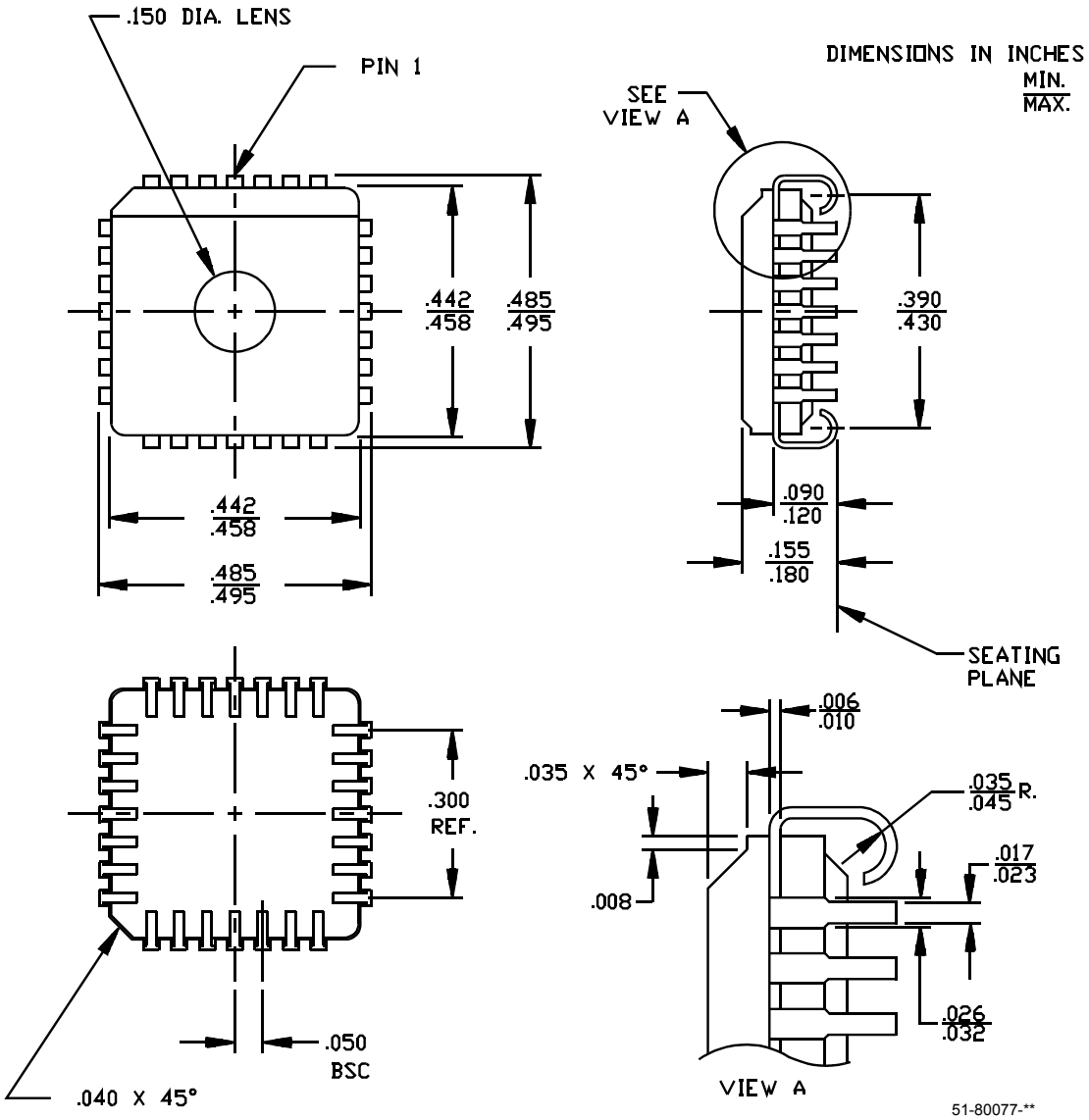


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C344B-15HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344B-15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B-15PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B-15WC/WI	W22	28-Lead Windowed CerDIP	
20	CY7C344B-20HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344B-20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B-20PC/PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C344B-20WC/WI	W22	28-Lead Windowed CerDIP	
25	CY7C344B-25HC/HI	H64	28-Lead Windowed Leaded Chip Carrier	Commercial/Industrial
	CY7C344B-25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
	CY7C344B-25PC/PI	P21	28-Lead (300-Mil) Molded DIP	

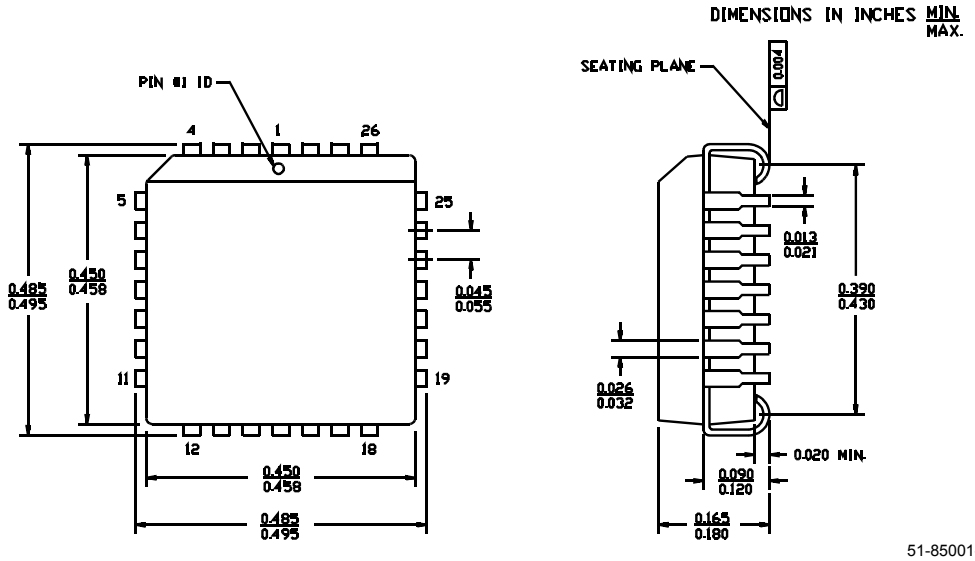
Package Diagrams

28-Pin Windowed Leaded Chip Carrier H64



Package Diagrams (continued)

28-Lead Plastic Leaded Chip Carrier J64



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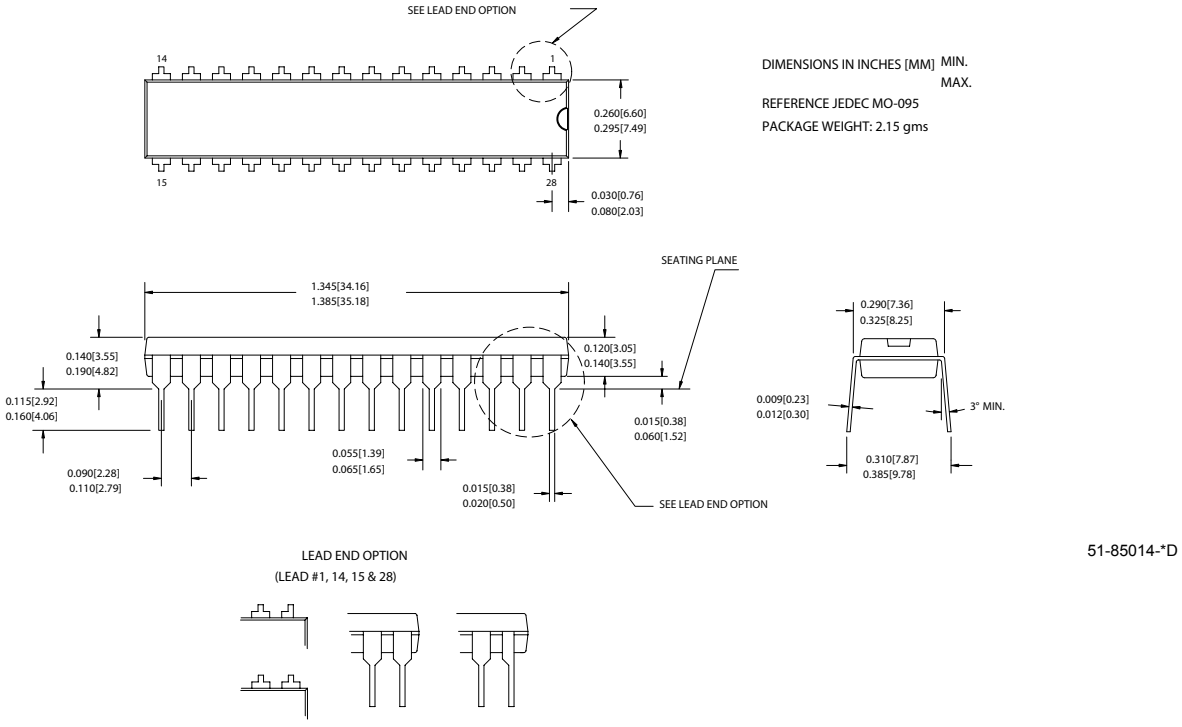
28-Lead (300-Mil) PDIP P21



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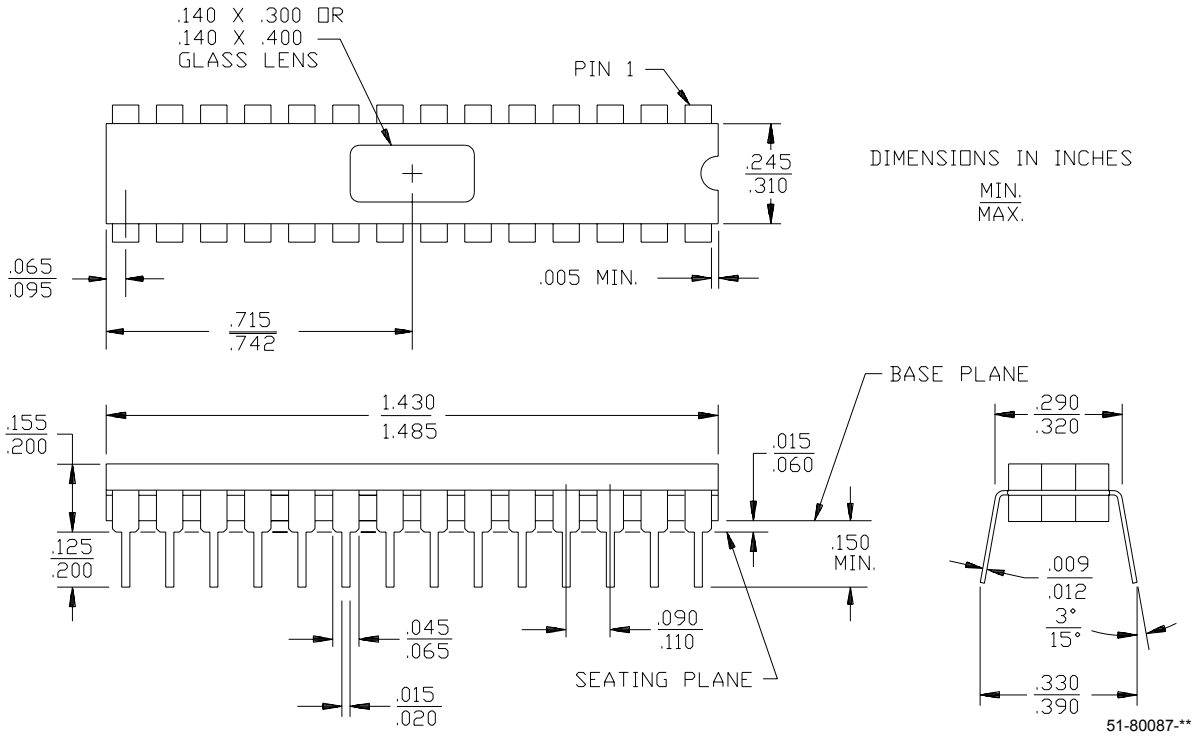
Package Diagrams (continued)

28-Lead (300-Mil) Windowed CerDIP W22
MIL-STD-1835 D-15 Config. A



Document History Page

Document Title: CY7C344 32-Macrocell MAX® EPLD Document Number: 38-03036				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106381	06/15/01	SZV	Change from Spec #: 38-00860 to 38-03036
*A	122235	12/28/02	RBI	Power-up requirements added to Operating Range Information
*B	213375	See ECN	FSG	Added note to title page: “Use Ultra37000 For All New Designs”
*C	238565	See ECN	KKV	Minor change: fixed error in part number in header
*D	373715	See ECN	PCX	Corrected header information