

2-Mbit (256 K × 8) MoBL® Static RAM

Features

- Very high speed: 45 ns
 - □ Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62138CV30
- Ultra low standby power
 - Typical standby current: 1 μA
 - Maximum standby current: 7 μA
- Ultra low active power
 - □ Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 36-ball ball grid array (BGA) package

Functional Description

The CY62138EV30 is a high performance CMOS static RAM organized as 256K words by eight bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life $^{\rm TM}$ (MoBL $^{\rm S}$) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected (CE HIGH).

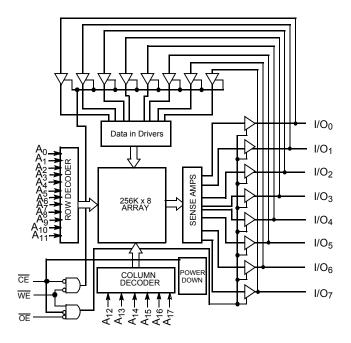
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins $(I/O_0$ through $I/O_7)$ is then written into the location specified on the address pins $(A_0$ through A_{18}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O₀ through I/O₇) are place<u>d in</u> a high impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE LOW and WE LOW).

For a complete list of related documentation, click here.

Logic Block Diagram



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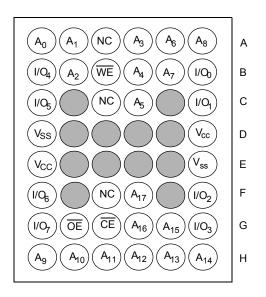
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Pin Configuration

Figure 1. 36-ball FBGA pinout (Top View) [1]



Product Portfolio

				Power Dissipation						
Product	V _{CC} Range (V)		V _{CC} Range (V)		Speed	Operating I _{CC} (mA)			- Standby I _{SB2} (μΑ)	
Floudet				(ns)	f = 1 MHz f = f _{max}		$t = t_{max}$		'SB2 (μΔ)	
	Min	Typ ^[2]	Max		Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max
CY62138EV30LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Notes

- NC pins are not connected on the die.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.



Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested. Storage temperature -65 °C to +150 °C Ambient temperature with power applied 55 °C to +125 °C Supply voltage to ground potential-0.3 V to V_{CC(MAX)} + 0.3 V DC voltage applied to outputs in High Z state $^{[3,\,4]}$ -0.3 V to V $_{CC(MAX)}$ + 0.3 V

DC input voltage [3, 4]0.3 V to	$V_{CC(MAX)} + 0.3 V$
Output current into outputs (LOW)	20 mA
Static discharge voltage(per MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 200 mA

Operating Range

Product	Range	Ambient Temperature	V cc ^[5]
CY62138EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

5	5	T	. P.O.	CY62138EV30-45			11!4
Parameter	Description	Test Co	naitions	Min	Typ ^[6]	Max	Unit
V _{OH}	Output HIGH voltage	$I_{OH} = -0.1 \text{ mA}$	V _{CC} = 2.20 V	2.0	_	_	V
		$I_{OH} = -1.0 \text{ mA}$	V _{CC} = 2.70 V	2.4	_	_	V
V _{OL}	Output LOW voltage	I _{OL} = 0.1 mA	V _{CC} = 2.20 V	_	_	0.4	V
		I _{OL} = 2.1 mA	V _{CC} = 2.70 V	_	_	0.4	V
V _{IH}	Input HIGH voltage	$V_{CC} = 2.2 \text{ V to } 2.7$	7 V	1.8	_	V _{CC} + 0.3	V
		V _{CC} = 2.7 V to 3.6	V	2.2	_	V _{CC} + 0.3	V
V _{IL}	Input LOW voltage	V _{CC} = 2.2 V to 2.7 V V _{CC} = 2.7 V to 3.6 V		-0.3	_	0.6	V
				-0.3	_	0.8	V
I _{IX}	Input leakage current	$GND \le V_1 \le V_{CC}$		-1	_	+1	μА
I _{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$	Output disabled	-1	_	+1	μА
I _{CC}	V _{CC} Operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC_{max}}$	_	15	20	mA
		f = 1 MHz	I _{OUT} = 0 mA CMOS levels	_	2	2.5	mA
I _{SB1} ^[7]	Automatic CE power down current – CMOS inputs	$\overline{\text{CE}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V}, \\ \text{V}_{\text{IN}} \le 0.2 \text{ V}, \text{ f} = \text{f}_{\text{m}} \\ \text{data only}), \text{ f} = 0 \text{ (C} \\ = 3.60 \text{ V}$	_{ax} (Addr <u>ess</u> and	-	1	7	μА
I _{SB2} ^[7]	Automatic CE power down current – CMOS inputs	$\overline{\text{CE}} \ge V_{\text{CC}} - 0.2 \text{ V}$ $V_{\text{IN}} \ge V_{\text{CC}} - 0.2 \text{ V}$ $f = 0, V_{\text{CC}} = 3.60$	′ or V _{IN} <u><</u> 0.2 V,	_	1	7	μΑ

Notes

- N_{IL(min.)} = -2.0 V for pulse durations less than 20 ns.
 V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC}(min.) and 200 μs wait time after V_{CC} stabilization.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
- 7. Chip enable (CE) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.



Capacitance

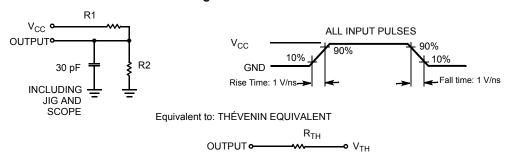
Parameter [8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = V_{CC(typ.)}$	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	36-ball BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	72	°C/W
$\Theta_{\sf JC}$	Thermal resistance (junction to case)		8.86	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Note

^{8.} Tested initially and after any design or process changes that may affect these parameters.



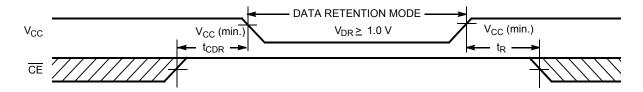
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[9]	Max	Unit
V_{DR}	V _{CC} for data retention		1	_	-	V
I _{CCDR} [10]	Data retention current	$V_{CC} = 1 \text{ V}, \overline{CE} \ge V_{CC} - 0.2 \text{ V}, \ V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$	_	0.8	3	μА
t _{CDR} ^[11]	Chip deselect to data retention time		0	-	-	ns
t _R ^[12]	Operation recovery time		45	_	-	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- 10. Chip enable (CE) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \ge 100~\mu s$ or stable at $V_{CC(min.)} \ge 100~\mu s$.

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Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	45	ns	11!4
Parameter 119, 111	Description		Max	Unit
Read Cycle				
t _{RC}	Read cycle time	45	-	ns
t _{AA}	Address to data valid	_	45	ns
t _{OHA}	Data hold from address change	10	1	ns
t _{ACE}	CE LOW to data valid	_	45	ns
t _{DOE}	OE LOW to data valid	_	22	ns
t _{LZOE}	OE LOW to Low Z ^[15]	5	_	ns
t _{HZOE}	OE HIGH to High Z [15, 16]	_	18	ns
t _{LZCE}	CE LOW to Low Z [15]	10	_	ns
t _{HZCE}	CE HIGH to High Z [15, 16]	_	18	ns
t _{PU}	CE LOW to power-up	0	-	ns
t _{PD}	CE HIGH to power-up	_	45	ns
Write Cycle [17]			_	•
t _{WC}	Write cycle time	45	_	ns
t _{SCE}	CE LOW to write end	35	_	ns
t _{AW}	Address setup to write end	35	_	ns
t _{HA}	Address hold from write end	0	_	ns
t _{SA}	Address setup to write start	0	_	ns
t _{PWE}	WE pulse width	35	_	ns
t _{SD}	Data setup to write end	25	_	ns
t _{HD}	Data hold from write end	0	_	ns
t _{HZWE}	WE LOW to High Z [15, 16]	_	18	ns
t _{LZWE}	WE HIGH to Low Z [15]	10	_	ns

Notes

<sup>Notes
13. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
14. Test conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of V_{CC(typ)}/2, input pulse levels of 0 to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} for any given device.
16. t_{HZCE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.</sup>



Switching Waveforms

Figure 4. Read Cycle No. 1: Address Transition Controlled [18, 19]

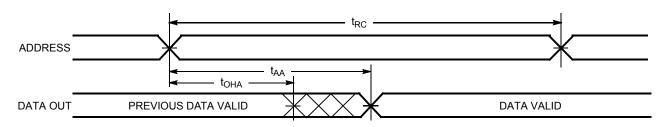
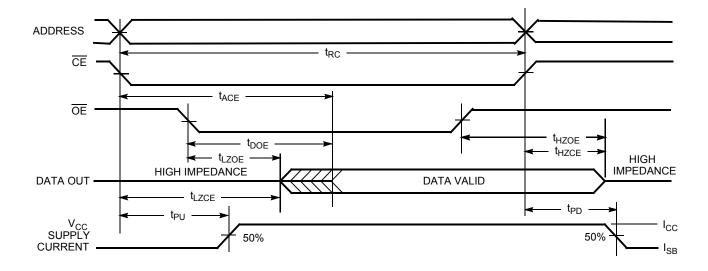


Figure 5. Read Cycle No. 2: $\overline{\text{OE}}$ Controlled [20, 21]



Notes

18. <u>Device</u> is continuously selected. OE, CE = V_{IL}.

19. <u>WE</u> is HIGH for read cycle.

20. WE is HIGH for read cycle.

21. Address valid prior to or coincident with CE transition LOW.



Switching Waveforms (continued)

Figure 6. Write Cycle No. 1: WE Controlled [22, 23]

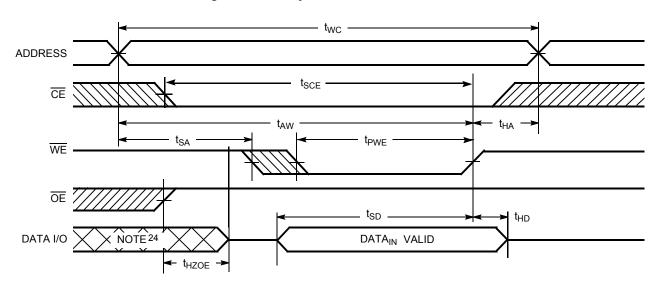
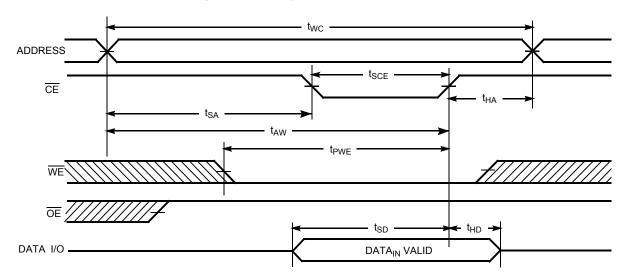


Figure 7. Write Cycle No. 2: $\overline{\text{CE}}$ Controlled [22, 23]



Notes

22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

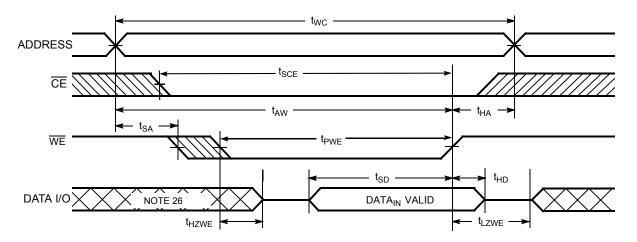
23. If \overline{CE} goes HIGH simultaneously with WE HIGH, the output remains in high impedance state.

24. During this period, the I/Os are in output state and input signals should not be applied.



Switching Waveforms (continued)

Figure 8. Write Cycle No. 3: WE Controlled, OE LOW [25]





Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H ^[27]	Х	Х	High Z	Deselect/power-down	Standby (I _{SB})
L	Н	L	Data out (I/O ₀ –I/O ₇)	Read	Active (I _{CC})
L	Н	Н	High Z	Output disabled	Active (I _{CC})
L	L	Х	Data in (I/O ₀ –I/O ₇)	Write	Active (I _{CC})

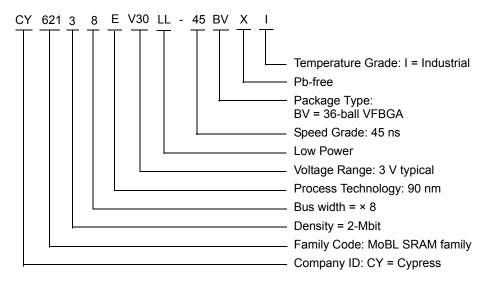
Note
27. Chip enable (CE) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138EV30LL-45BVXI	51-85149	36-ball VFBGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial

Ordering Code Definitions



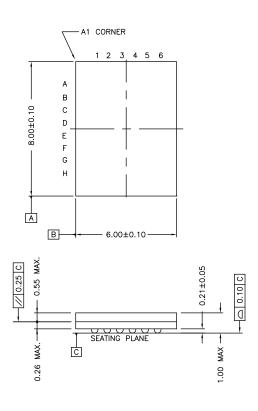
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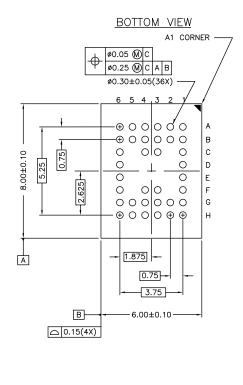


Package Diagram

Figure 9. 36-ball VFBGA (6 × 8 × 1.0 mm) BV36A Package Outline, 51-85149

TOP VIEW





51-85149 *E

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Acronyms

Acronym	Description		
BGA	ball gird array		
CE	chip enable		
CMOS	complementary metal oxide semiconductor		
FBGA	fine-pitch ball gird array		
I/O	input/output		
OE	output enable		
SRAM	static random access memory		
VFBGA	very fine ball gird array		
WE	write enable		

Document Conventions

Units of Measure

Symbol	Unit of Measure		
°C	degree Celsius		
MHz	megahertz		
μΑ	microampere		
μS	microsecond		
mA	milliampere		
mm	millimeter		
ns	nanosecond		
pF	picofarad		
Ω	ohm		
V	volt		
W	watt		

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Document History Page

Rev.	ECN No.	Orig. of	Submission	Description of Change
		Change	Date	·
**	237432	AJU	See ECN	New data sheet
*A	427817	NXR	See ECN	Removed 35 ns Speed Bin Removed "L" version Removed "L" version Removed 32-pin TSOPII package from product Offering. Changed ball C3 from DNU to NC. Removed the redundant footnote on DNU. Moved Product Portfolio from Page # 3 to Page #2. Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f = 1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max} =1/t_{RC} Changed I_{SB1} and I_{SB2} Typ. values from 0.7 μ A to 1 μ A and Max. values from 2.5 μ A to 7 μ A. Changed VCC stabilization time in footnote #7 from 100 μ s to 200 μ s Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed VDR from 1.5V to 1V on Page# 4. Changed I_{CCDR} from 1 μ A to 3 μ A in the Data Retention Characteristics table on Page # 4. Corrected I_{R} in Data Retention Characteristics from 100 μ s to I_{RC} ns Changed I_{CDR} , I_{LZCE} , I_{LZWE} from 6 ns to 10 ns Changed I_{CDR} , I_{HZCE} , I_{HZWE} from 15 ns to 18 ns Changed I_{SCE} and I_{AW} from 40 ns to 35 ns Changed I_{SCE} and I_{AW} from 40 ns to 35 ns Changed I_{PWE} from 25 ns to 35 ns Updated the Ordering Information table and replaced Package Name column with Package Diagram.
*B	2604685	VKN / PYRS	11/12/08	Added footnote 7 related to I _{SB2} and I _{CCDR}
*C	3143896	RAME	01/17/2011	Updated Datasheet as per new template Added Ordering Code Definitions Added Acronyms and Units of Measure table Converted all tablenotes to Footnote Updated Package Diagram 51-85149 from *C to *D
*D	3284728	AJU	06/16/2011	Removed the Note "For best practice recommendations, refer to the Cypress application note "SRAM System Design Guidelines" on http://www.cypress.com." in page 1 and its reference in Functional Description Updated in new template.
*E	3806123	TAVA	11/08/2012	Updated Data Retention Waveform (Updated Figure 3 (Changed " $V_{DR} \ge 1.5 V_{DR} \ge 1.0 V$ ")). Updated Package Diagram (spec 51-85149 (Changed revision from *D to *E)
*F	4099016	VINI	08/19/2013	Updated Switching Characteristics: Added Note 13 and referred the same note in "Parameter" column. Updated in new template. Completing Sunset Review.
*G	4576475	VINI	11/19/2014	Added related documenation hyperlink in page 1.

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