CY7C1061G Automotive

16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
  - t_{AA} = 10 ns
- Temperature range
  - Automotive-E: –40 °C to 125 °C
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
  - I_{CC} = 90-mA typical at 100 MHz
  - I_{SB2} = 20-mA typical
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

CY7C1061G[1] is a high-performance CMOS fast static RAM automotive part with embedded ECC. ECC logic can detect and correct single-bit error in read data word during read cycles.

This device has single chip enable input and is accessed by asserting the chip enable input (CE) LOW.

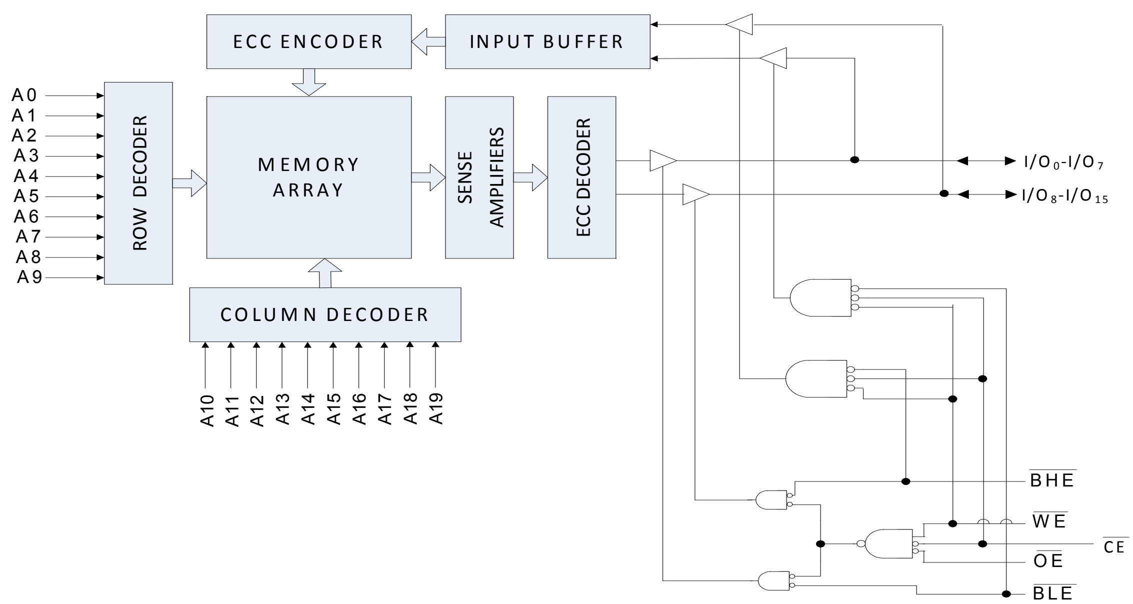
To perform data writes, assert the Write Enable (WE) input LOW and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable (BHE) and Byte Low Enable (BLE), inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. BHE controls I/O_8 through I/O_{15} and BLE controls I/O_0 through I/O_7.

To perform data reads, assert the Output Enable (OE) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (CE HIGH), or control signals are de-asserted (OE, BLE, BHE). Refer to the below logic block diagram.

The CY7C1061G automotive device is available in 48-ball VFBGA and 48-pin TSOP I packages.

Logic Block Diagram – CY7C1061G



Note
1. The device does not support automatic write-back on error detection.

Contents

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout [2]

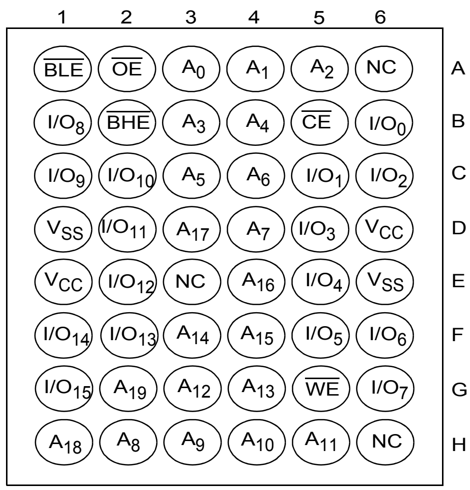
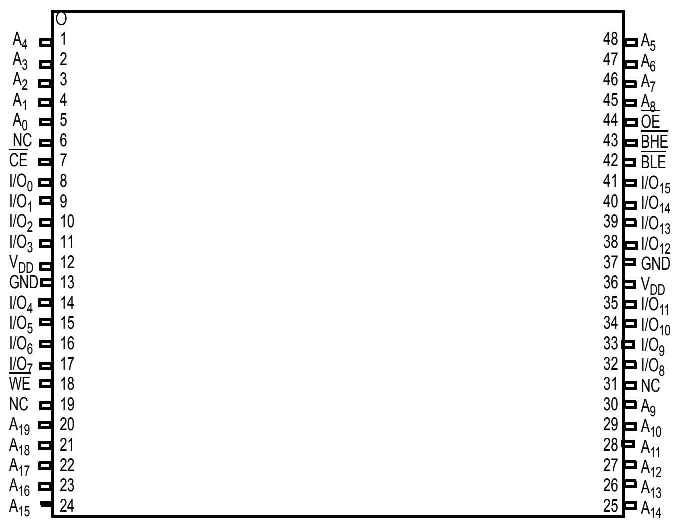


Figure 2. 48-pin TSOP I (12 × 18.4 × 1 mm) pinout [2]



Product Portfolio

Product	Range	V_{CC} Range (V)	Speed (ns)	Current Consumption			
				Operating I_{CC} (mA) $f = f_{max}$		Standby, I_{SB2} (mA)	
				Typ[3]	Max	Typ[3]	Max
CY7C1061G30	Automotive	2.2 V–3.6 V	10	90	160	20	50

Notes
2. NC pins are not connected internally to the die.
3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND .... –0.5 V to +6.0 V

DC voltage applied to outputs in High-Z State [4] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage [4] .... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch-up current .... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Automotive-E	–40 °C to +125 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the operating range of –40 °C to 125 °C

Parameter	Description		Test Conditions		10 ns			Unit
					Min	Typ [5]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.0	–	–	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH} [4]	Input HIGH voltage	2.2 V to 2.7 V	–		2.0	–	V_{CC} + 0.3	V
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	
V_{IL} [4]	Input LOW voltage	2.2 V to 2.7 V	–		–0.3	–	0.6	V
		2.7 V to 3.6 V	–		–0.3	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–5.0	–	+5.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–5.0	–	+5.0	µA
I_{CC}	Operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = f_{MAX} = 1/t_{RC}	–	90.0	160.0	mA
I_{SB1}	Automatic CE power down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	60.0	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	20.0	50.0	mA

Notes
4. V_{IL} (min) = –2.0 V and V_{IH} (max) = V_{CC} +2 V for pulse durations of less than 2 ns.
5. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, T_A = 25 °C.

Capacitance

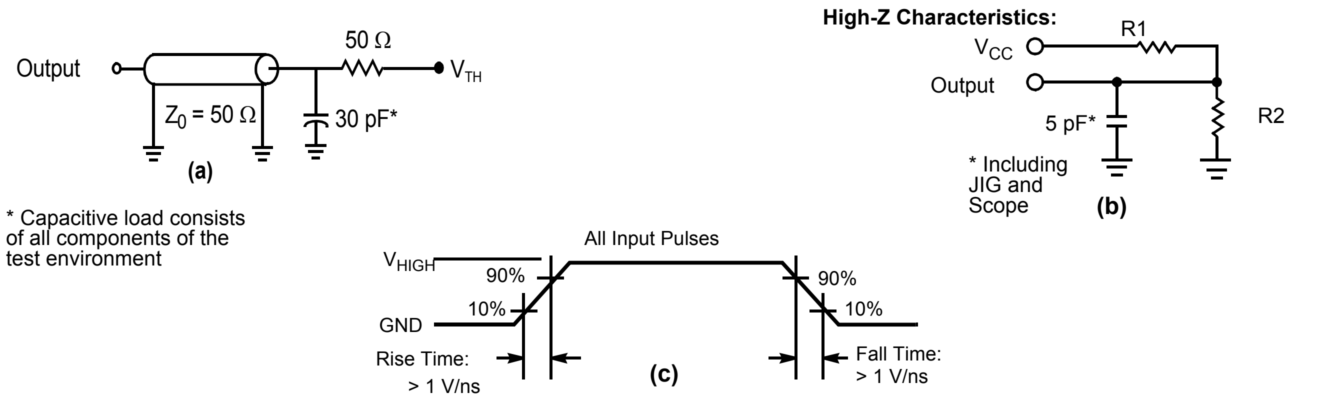
Parameter [6]	Description	Test Conditions	All Packages	Unit
C_{IN}	Input capacitance	$T_A = 25\,°C$, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	31.50	57.99	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.75	13.42	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [7]



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{TH}	1.5	V
V_{HIGH}	3	V

Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full-device AC operation assumes a 100-μs ramp time from 0 to V_{CC}(min) and 100-μs wait time after V_{CC} stabilizes to its operational value.

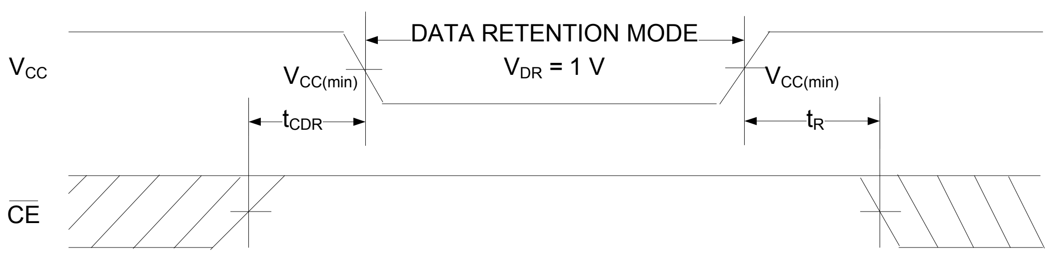
Data Retention Characteristics

Over the operating range of –40 °C to 125 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	50.0	mA
t_{CDR}[8]	Chip deselect to data retention time	–	0	–	ns
t_R[8]	Operation recovery time	$V_{CC} \geq 2.2$ V	10.0	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform [9]



Notes
8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 100 µs or stable at V_{CC}(min) ≥ 100 µs.

AC Switching Characteristics

Over the operating range of –40 °C to 125 °C

Parameter [10]	Description	10 ns		Unit
		Min	Max	
Read Cycle				
t_{POWER}	V_{CC}(stable) to the first access[11]	100.0	-	µs
t_{RC}	Read cycle time	10.0	–	ns
t_{AA}	Address to data	–	10.0	ns
t_{OHA}	Data hold from address change	3.0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data	–	10.0	ns
t_{DOE}	$\overline{OE}$ LOW to data	–	5.0	ns
t_{LZOE}	$\overline{OE}$ LOW to low-Z [12, 13]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high-Z [12, 13]	–	5.0	ns
t_{LZCE}	$\overline{CE}$ LOW to low-Z [12, 13]	3.0	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high-Z [12, 13]	–	5.0	ns
t_{PU}	$\overline{CE}$ LOW to power-up [14]	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [14]	–	10.0	ns
t_{DBE}	Byte enable to data valid	–	5.0	ns
t_{LZBE}	Byte enable to low-Z [12, 13]	0	–	ns
t_{HZBE}	Byte disable to high-Z [12, 13]	–	6.0	ns
Write Cycle [15, 16]				
t_{WC}	Write cycle time	10.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7.0	–	ns
t_{AW}	Address setup to write end	7.0	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	ns
t_{SD}	Data setup to write end	5.0	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low-Z [12, 13]	3.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high-Z [12, 13]	–	5.0	ns
t_{BW}	Byte Enable to write end	7.0	–	ns

Notes

10. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use the output loading shown in part (a) of Figure 3 on page 5, unless specified otherwise.
11. t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed.
12. t_{HZOE}, t_{HZCE}, t_{HZWE}, and t_{HZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 3 on page 5. Hi-Z, Lo-Z transition is measured ±200 mV from steady state voltage.
13. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
14. These parameters are guaranteed by design and are not tested.
15. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{BHE}$, or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
16. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY7C1061G (Address Transition Controlled) [17, 18]

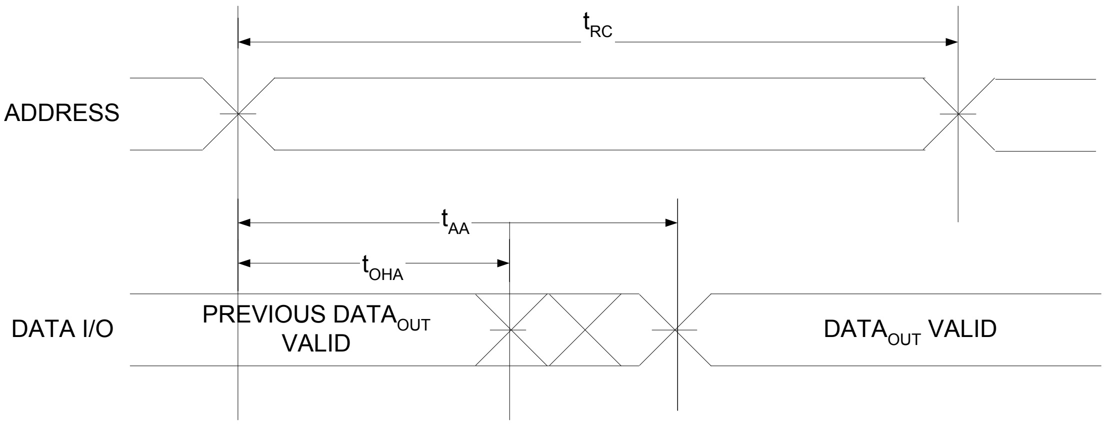
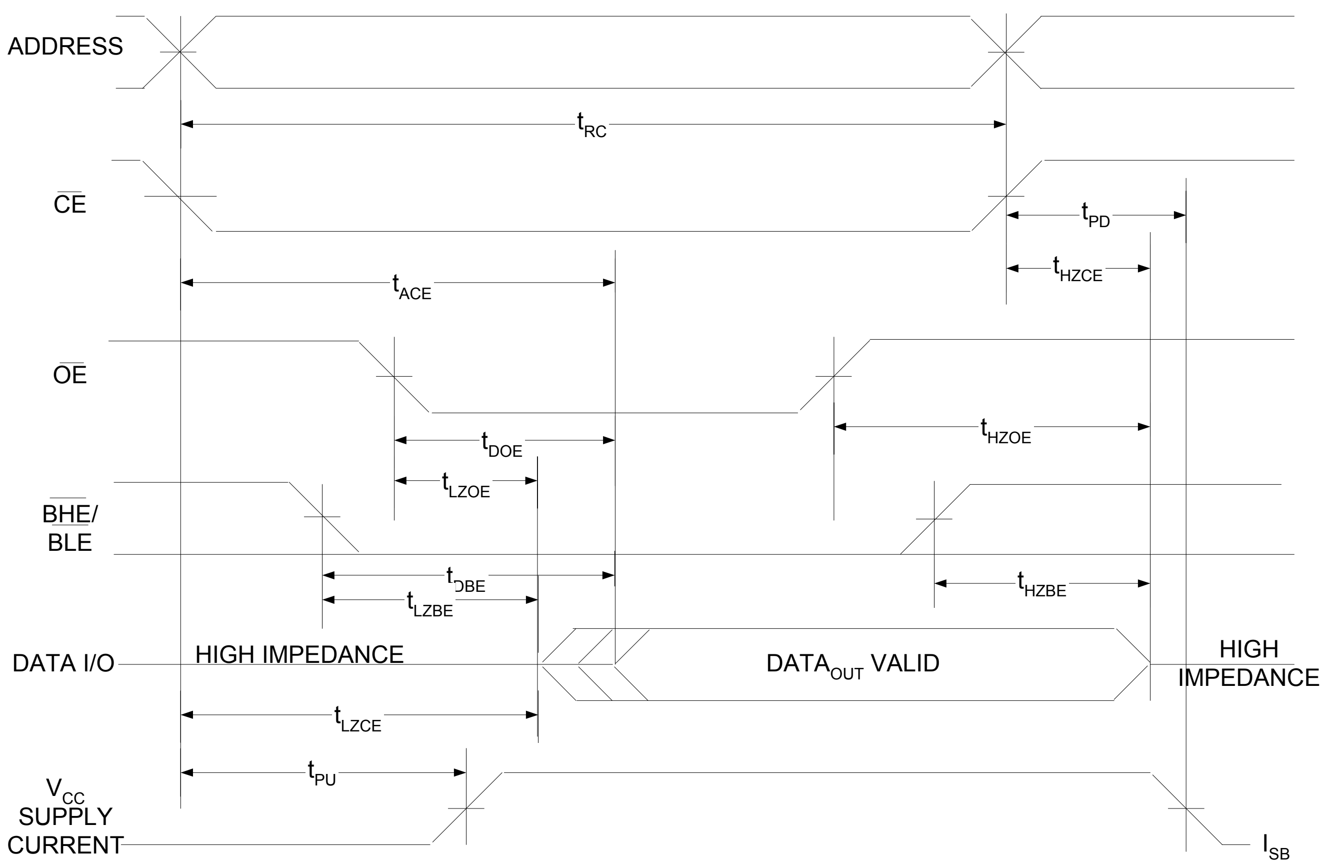


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [18, 19]



Notes

17. The device is continuously selected, $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
18. $\overline{WE}$ is HIGH for read cycle.
19. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [20, 21]

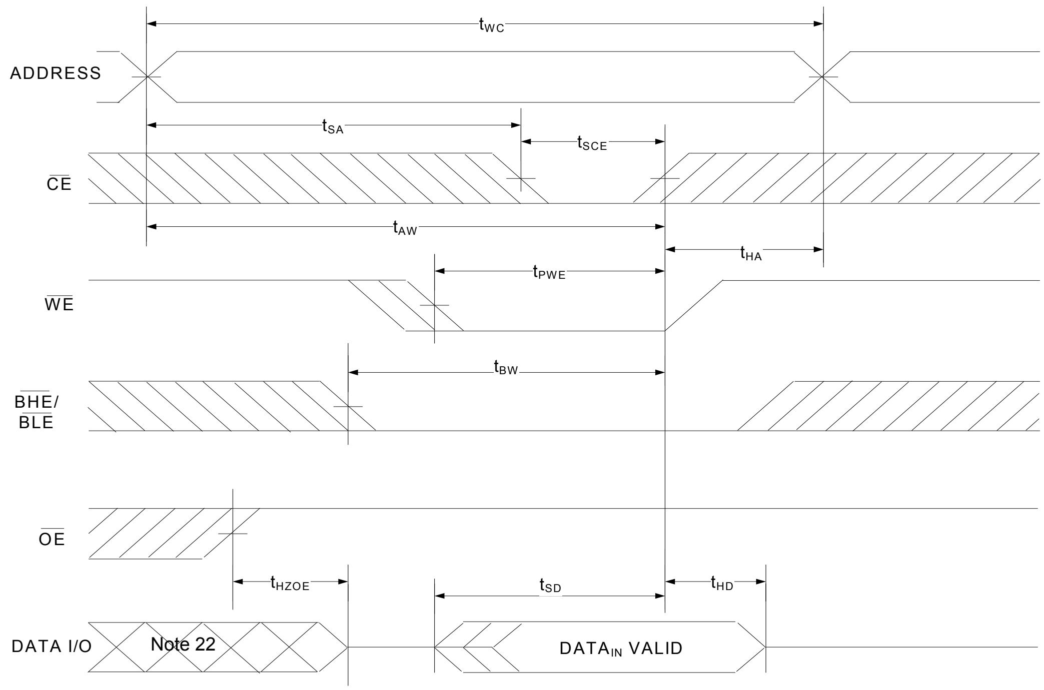
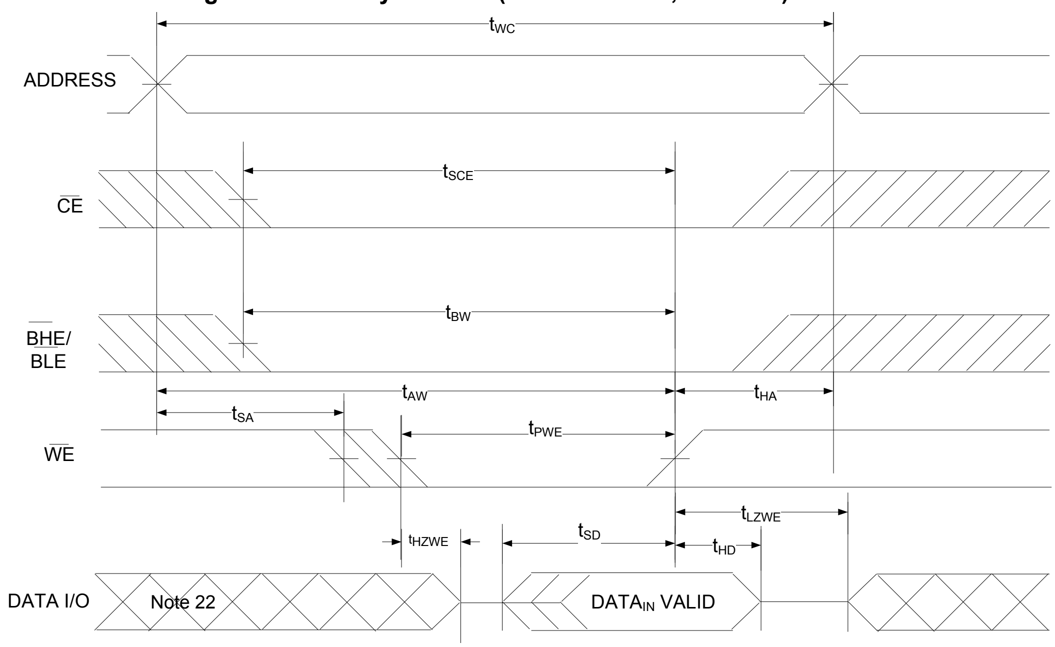


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [20, 21, 23]

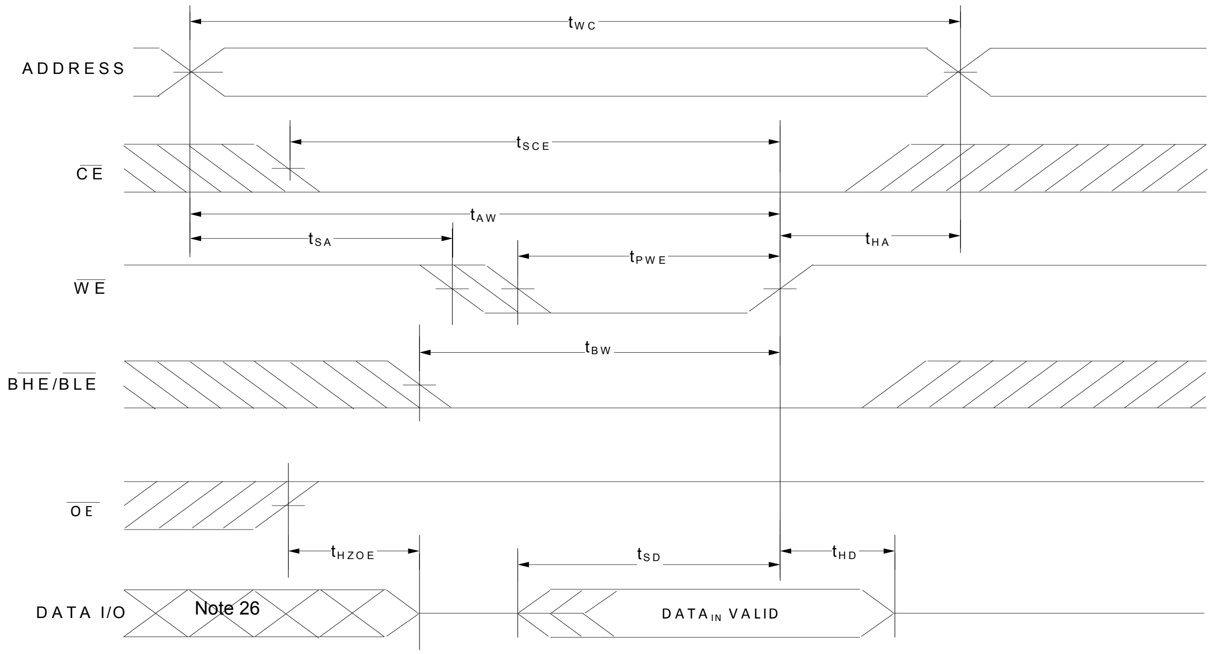


Notes

20. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. Data I/O is in high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
22. During this period, the I/Os are in output state. Do not apply input signals.
23. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled) [24, 25]

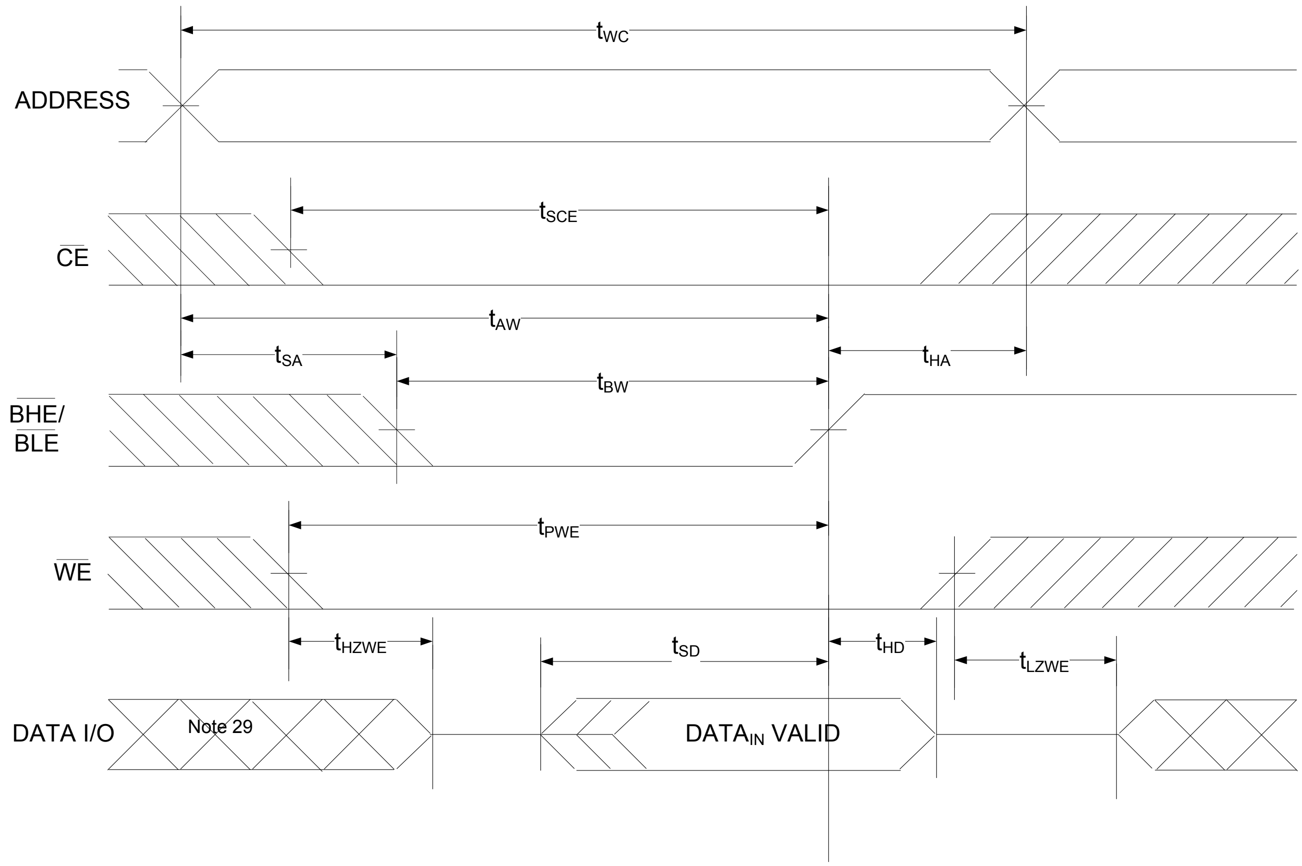


Notes

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
25. Data I/O is in high impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
26. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [27, 28]



Notes

27. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and $\overline{BHE}$ or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
28. Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
29. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

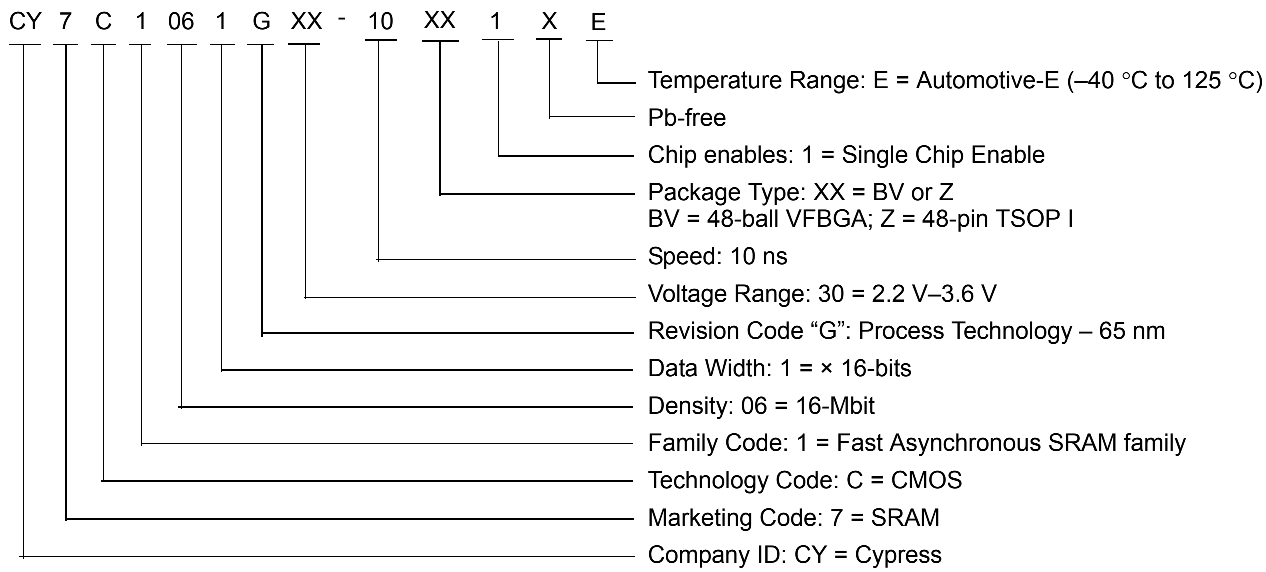
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X[30]	X[30]	X[30]	X[30]	High Z	High Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	High Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	X	L	L	H	Data in	High Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Note
30. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1061G30-10BV1XE	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free)	Automotive-E
		CY7C1061G30-10ZXE	51-85183	48-pin TSOP I (12 × 18.4 × 1.0 mm) (Pb-free)	

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

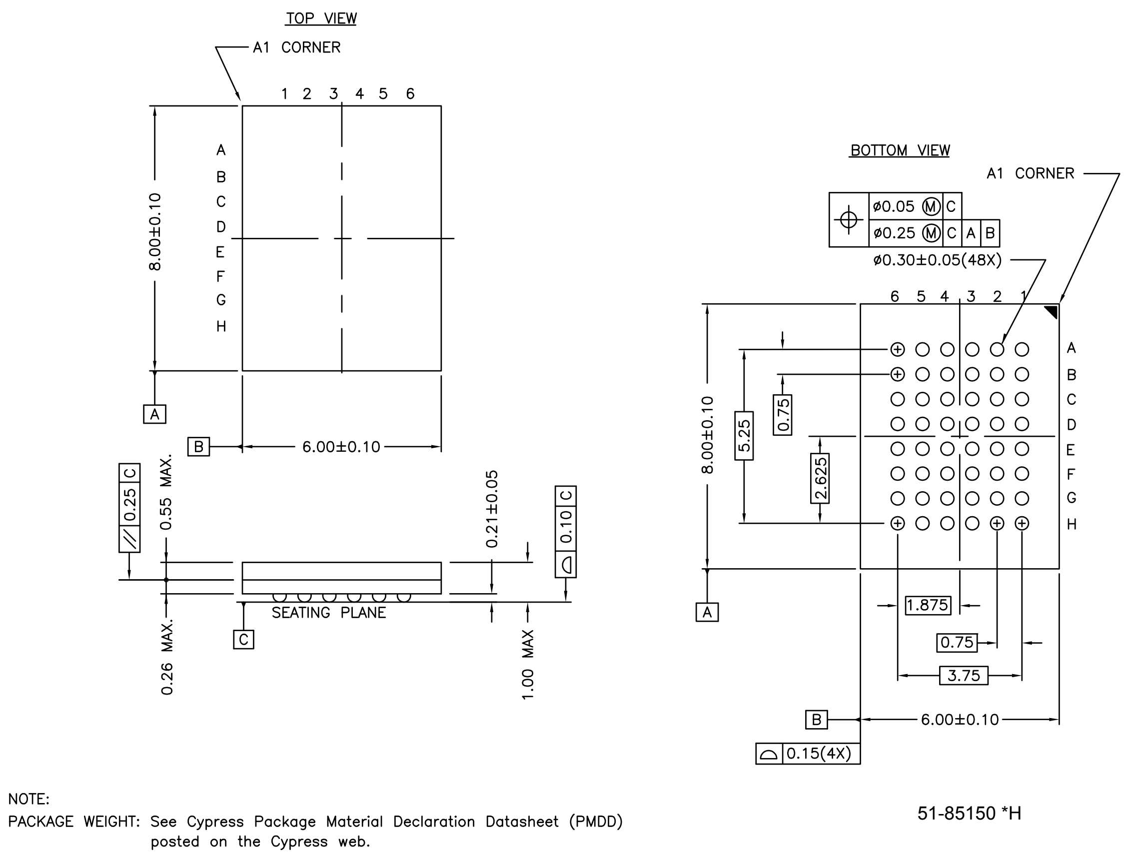
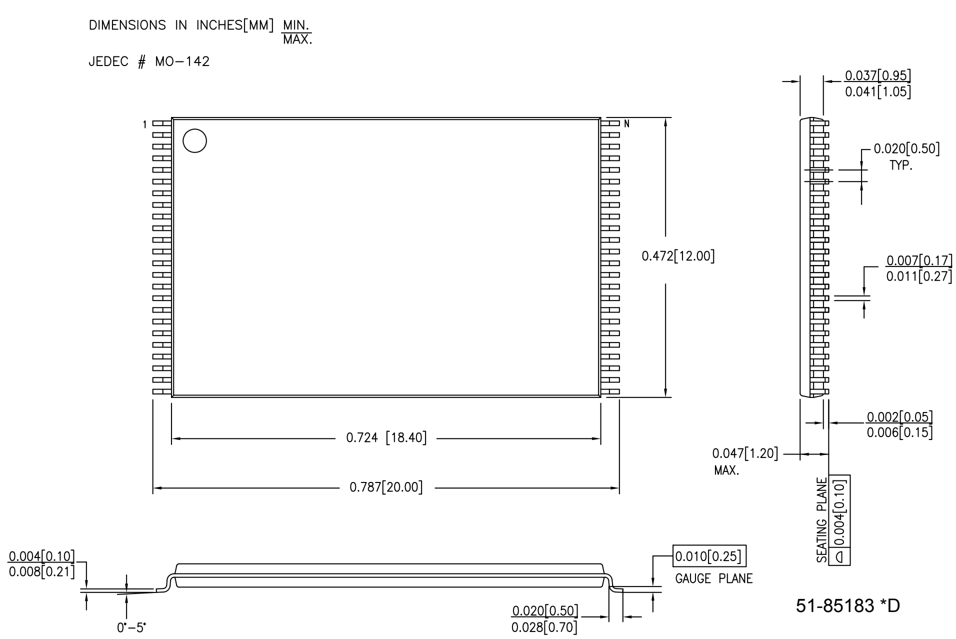


Figure 12. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1061G Automotive, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-84821				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3825225	MEMJ	11/29/2012	New data sheet.
*A	4003550	NILE	05/20/2013	Updated Document Title to read as “CY7C1061G Automotive, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC)”. Updated Features. Updated Functional Description. Removed “Logic Block Diagram – CY7C1061GE”. Updated Logic Diagram for Single Chip Enable. Updated Pin Configurations: Updated Pin diagram to have BV1XE without ERR pin Updated Product Portfolio. Updated Operating Range. Updated Capacitance. Updated Thermal Resistance. Updated Data Retention Characteristics. Updated AC Switching Characteristics: Removed 12 ns, 17 ns speed bin related information and included 10 ns speed bin related information. Updated Switching Waveforms. Removed “ERR Output – CY7C1061GE”. Updated Package Diagrams: Added 48-pin TSOP I Package Diagram (Figure 11).
*B	4292074	MEMJ	02/28/2014	Updated Features: Mentioned frequency of measurement for I_{CC} (typical). Updated Functional Description: Replaced “an error detection” with “a single-bit error detection”. Added Note 1 (for ECC) and referred the same note in CY7C1061G. Updated Product Portfolio: Replaced CY7C1061G with CY7C1061G30. Updated Operating Range: Replaced Automotive with Automotive-E. Updated DC Electrical Characteristics: Added typical value for I_{CC} parameter (90 mA). Added typical value for I_{SB2} parameter (20 mA). Added Note 5 and referred the same note in “Typ” column. Updated AC Switching Characteristics: Added t_{POWER} parameter and its details. Added Note 11 and referred the same note in description of t_{POWER} parameter. Added Note 13 and referred the same note in description of t_{LZOE}, t_{HZOE}, t_{LZCE}, t_{HZCE}, t_{LZBE}, t_{HZBE}, t_{LZWE}, and t_{HZWE} parameters. Added Note 16 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 22 and referred the same note in Figure 7 and Figure 8. Added Note 23 and referred the same note in Figure 8. Added Figure 9. Added Note 26 and referred the same note in Figure 9 (to indicate that I/Os are in output state). Added Note 29 and referred the same note in Figure 10 (to indicate that I/Os are in output state).

Document History Page (continued)

Document Title: CY7C1061G Automotive, 16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-84821				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B (cont.)	4292074	MEMJ	02/28/2014	Updated Truth Table: Added Note 30 and referred the same note in “X” corresponding to Power down mode. Added condition to place outputs in disable state by making both $\overline{BHE}$ and $\overline{BLE}$ HIGH. Added Errata. Updated to new template.
*C	4330547	AJU	04/02/2014	No technical updates.
*D	4397546	AJU	06/03/2014	Updated AC Switching Characteristics: Updated Note 12 (Removed t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE}; and added Hi-Z, Lo-Z transition).
*E	4469360	NILE	09/18/2014	No technical updates.
*F	4576640	VINI	11/21/2014	No technical updates.
*G	4800949	NILE	09/30/2015	Updated Logic Block Diagram – CY7C1061G. Updated Package Diagrams: spec 51-85183 – Changed revision from *C to *D. Removed Errata. Updated to new template.
*H	4983893	NILE	10/28/2015	Changed status from Preliminary to Final.

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