

128K x 8 Static RAM

Features

- High speed
 - $t_{AA} = 12 \text{ ns}$
- Low active power
 - 495 mW (max. 12 ns)
- Low CMOS standby power
 - 55 mW (max.) 4 mW
- 2.0V Data Retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 , and \overline{OE} options

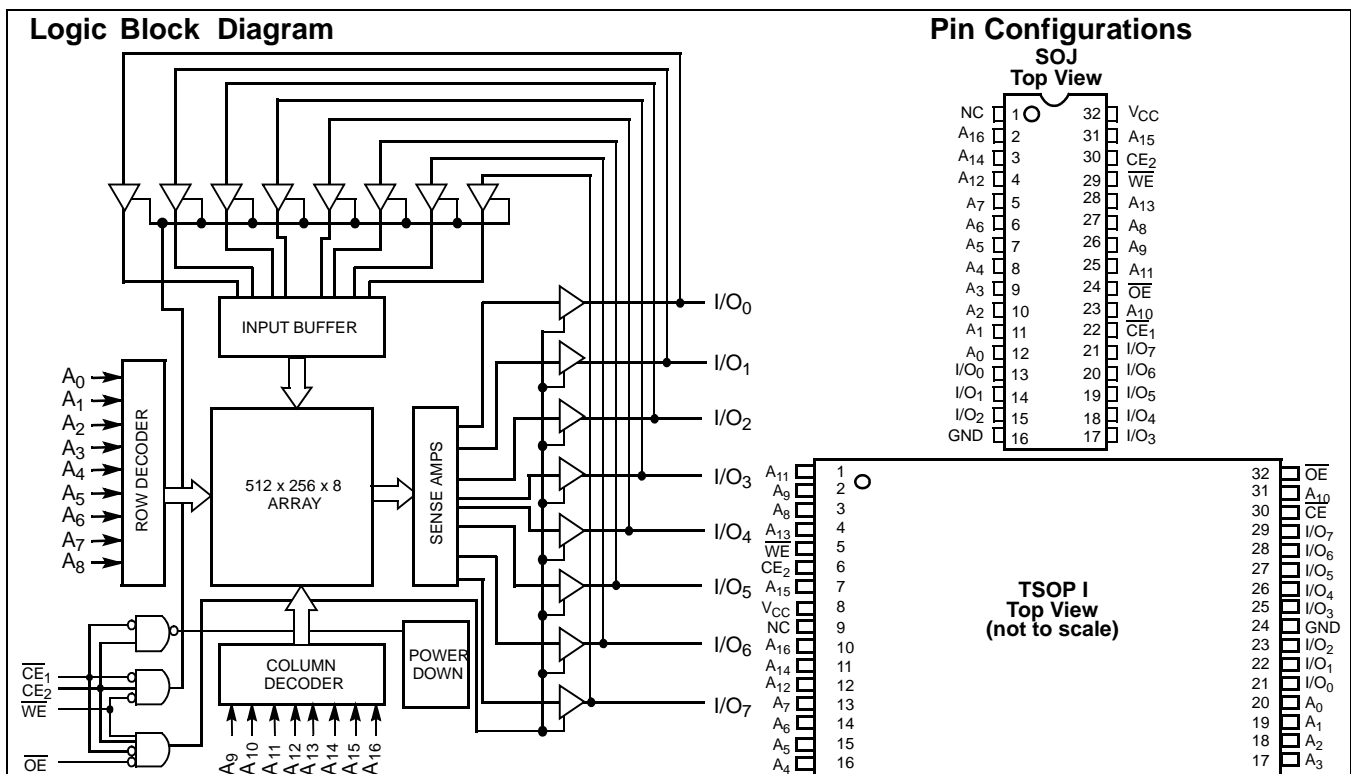
Functional Description^[1]

The CY7C109BN/CY7C1009BN is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}_1), an active HIGH Chip Enable (\overline{CE}_2), an active LOW Output Enable (\overline{OE}), and three-state drivers. Writing to the device is accomplished by taking Chip Enable One (\overline{CE}_1) and Write Enable (\overline{WE}) inputs LOW and Chip Enable Two (\overline{CE}_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable One (\overline{CE}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) and Chip Enable Two (\overline{CE}_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, \overline{CE}_2 HIGH, and \overline{WE} LOW).

The CY7C109BN is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009BN is available in a 300-mil-wide SOJ package. The CY7C1009BN and CY7C109BN are functionally equivalent in all other respects.



Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Selection Guide

| | | 7C109B-12 7C1009B-12 | 7C109B-15 7C1009B-15 | 7C109B-20 7C1009B-20 | Unit |
|------------------------------|---|-------------------------|-------------------------|-------------------------|------|
| Maximum Access Time | | 12 | 15 | 20 | ns |
| Maximum Operating Current | | 90 | 80 | 75 | mA |
| Maximum CMOS Standby Current | | 10 | 10 | 10 | mA |
| | L | 2 | 2 | 2 | mA |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[2] -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State^[2] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[2] -0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | -40°C to +85°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C109BN-12 7C1009BN-12 | | 7C109BN-15 7C1009BN-15 | | 7C109BN-20 7C1009BN-20 | | Unit |
|------------------|--|---|---------------------------|-----------------------|---------------------------|-----------------------|---------------------------|-----------------------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} + 0.3 | 2.2 | V _{CC} + 0.3 | 2.2 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage ^[2] | | -0.3 | 0.8 | -0.3 | 0.8 | -0.3 | 0.8 | V |
| I _{IX} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | -1 | +1 | -1 | +1 | -1 | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _I ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | -5 | +5 | μA |
| I _{OS} | Output Short Circuit Current ^[3] | V _{CC} = Max., V _{OUT} = GND | | -300 | | -300 | | -300 | mA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} | | 90 | | 80 | | 75 | mA |
| I _{SB1} | Automatic CE Power-Down Current —TTL Inputs | Max. V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 45 | | 40 | | 30 | mA |
| I _{SB2} | Automatic CE Power-Down Current —CMOS Inputs | Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0 | | 10 | | 10 | | 10 | mA |
| | | | L | 2 | | 2 | | 2 | mA |

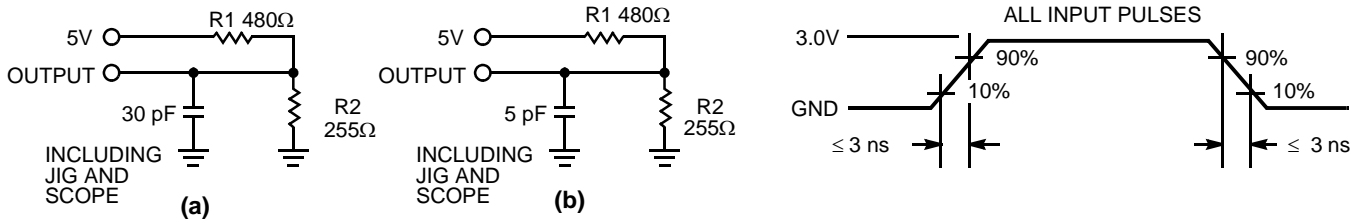
Capacitance^[4]

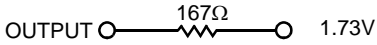
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V | 9 | pF |
| C _{OUT} | Output Capacitance | | 8 | pF |

Notes:

- Minimum voltage is -2.0V for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics^[5] Over the Operating Range

| Parameter | Description | 7C109BN-12 7C1009BN-12 | | 7C109BN-15 7C1009BN-15 | | 7C109BN-20 7C1009BN-20 | | Unit |
|----------------------------------|--|---------------------------|------|---------------------------|------|---------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | |
| t _{RC} | Read Cycle Time | 12 | | 15 | | 20 | | ns |
| t _{AA} | Address to Data Valid | | 12 | | 15 | | 20 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | 3 | | ns |
| t _{ACE} | \overline{CE}_1 LOW to Data Valid, CE_2 HIGH to Data Valid | | 12 | | 15 | | 20 | ns |
| t _{DOE} | \overline{OE} LOW to Data Valid | | 6 | | 7 | | 8 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z | 0 | | 0 | | 0 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[6, 7] | | 6 | | 7 | | 8 | ns |
| t _{LZCE} | \overline{CE}_1 LOW to Low Z, CE_2 HIGH to Low Z ^[7] | 3 | | 3 | | 3 | | ns |
| t _{HZCE} | \overline{CE}_1 HIGH to High Z, CE_2 LOW to High Z ^[6, 7] | | 6 | | 7 | | 8 | ns |
| t _{PU} | \overline{CE}_1 LOW to Power-Up, CE_2 HIGH to Power-Up | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE}_1 HIGH to Power-Down, CE_2 LOW to Power-Down | | 12 | | 15 | | 20 | ns |
| Write Cycle^[8] | | | | | | | | |
| t _{WC} | Write Cycle Time ^[9] | 12 | | 15 | | 20 | | ns |
| t _{SCE} | \overline{CE}_1 LOW to Write End, CE_2 HIGH to Write End | 10 | | 12 | | 15 | | ns |
| t _{AW} | Address Set-Up to Write End | 10 | | 12 | | 15 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 10 | | 12 | | 12 | | ns |
| t _{SD} | Data Set-Up to Write End | 7 | | 8 | | 10 | | ns |
| t _{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t _{LZWE} | \overline{WE} HIGH to Low Z ^[7] | 3 | | 3 | | 3 | | ns |
| t _{HZWE} | \overline{WE} LOW to High Z ^[6, 7] | | 6 | | 7 | | 8 | ns |

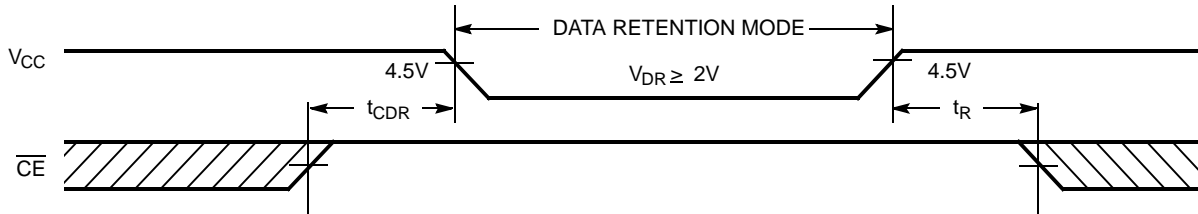
Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range (Low Power version only)

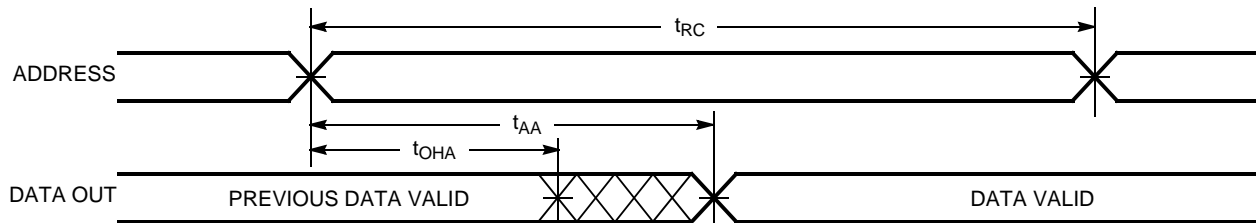
| Parameter | Description | Conditions | Min. | Max. | Unit |
|------------|--------------------------------------|---|------|------|---------|
| V_{DR} | V_{CC} for Data Retention | No input may exceed $V_{CC} + 0.5V$ | 2.0 | | V |
| I_{CCDR} | Data Retention Current | $V_{CC} = V_{DR} = 2.0V$, $CE_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, | | 150 | μA |
| t_{CDR} | Chip Deselect to Data Retention Time | $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ | 0 | | ns |
| t_R | Operation Recovery Time | | 200 | | μs |

Data Retention Waveform

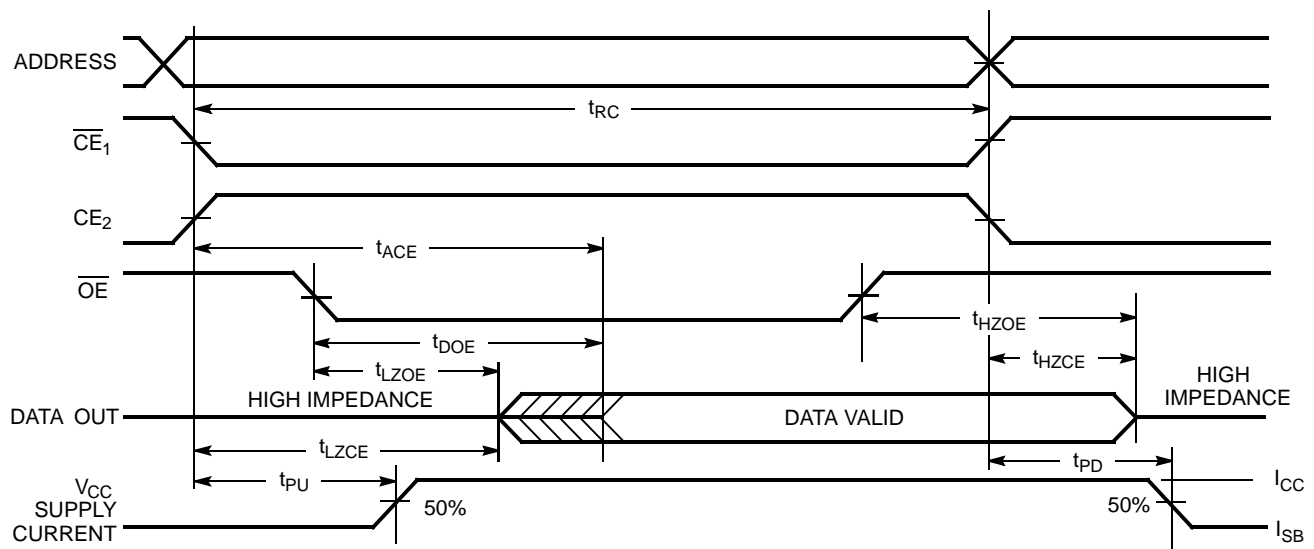


Switching Waveforms

Read Cycle No. 1 [10, 11]



Read Cycle No. 2 (OE Controlled) [11, 12]

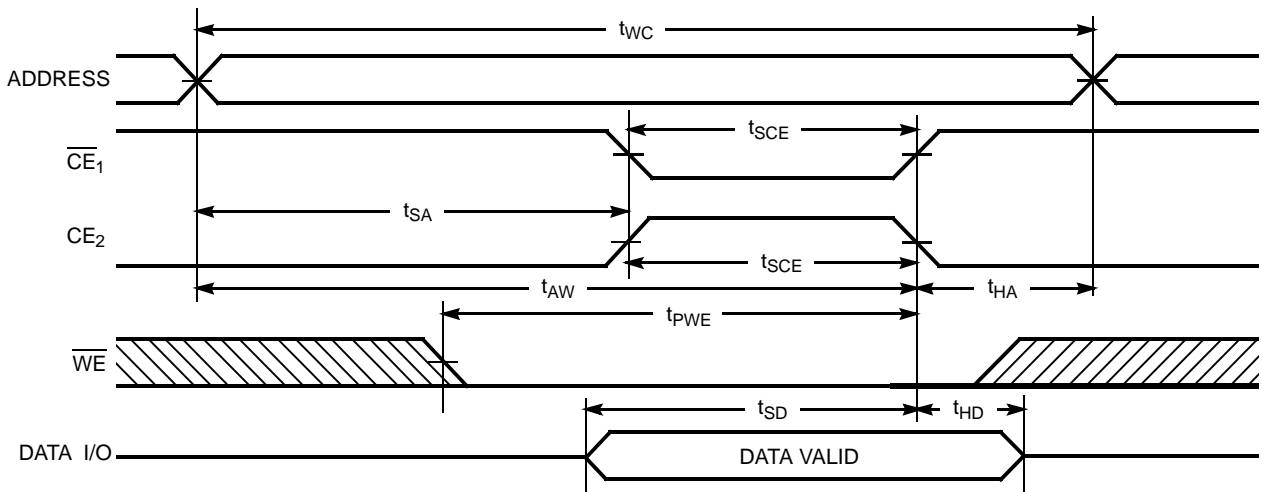


Notes:

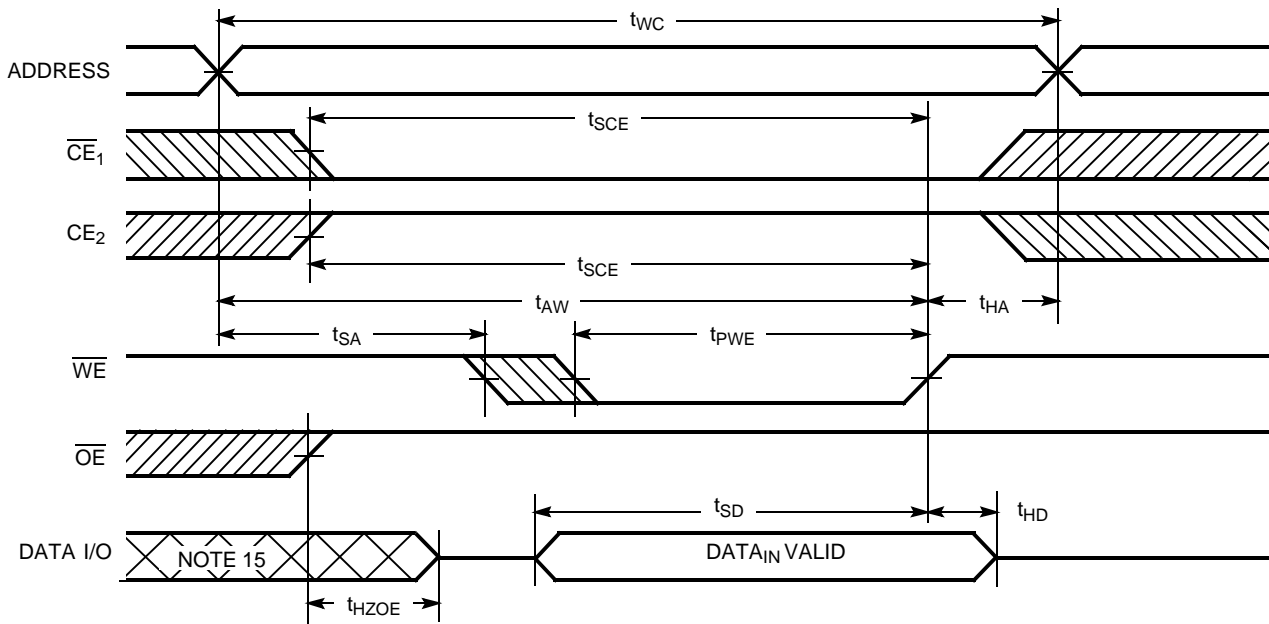
- 10. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- 11. WE is HIGH for read cycle.
- 12. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{CE}_1 or CE_2 Controlled)^[13, 14]



Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[13, 14]

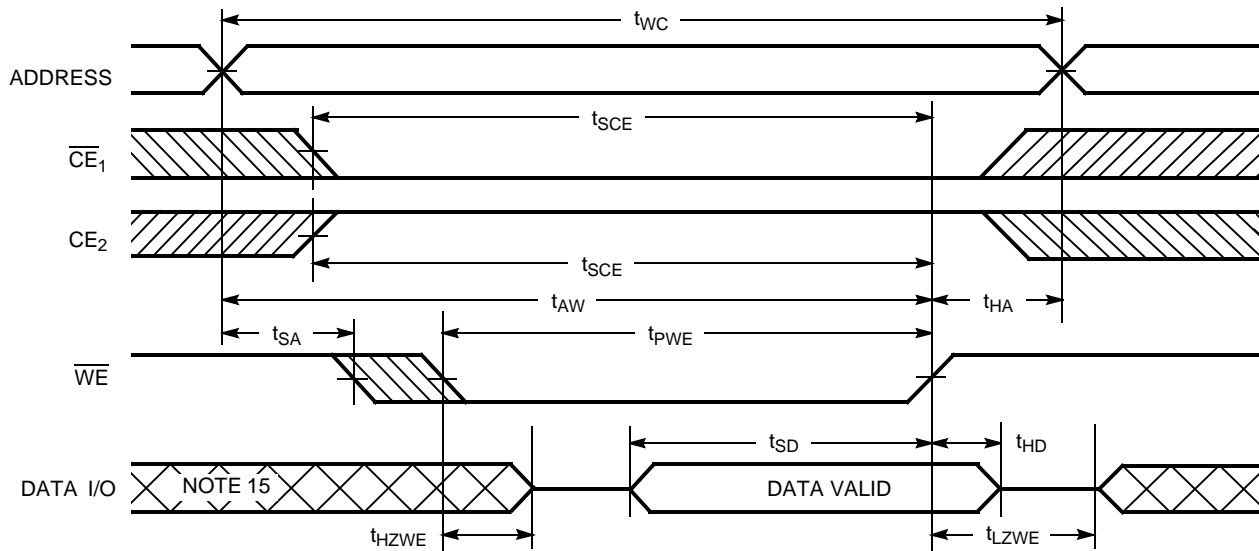


Notes:

- 13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 14. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
- 15. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[14]



Truth Table

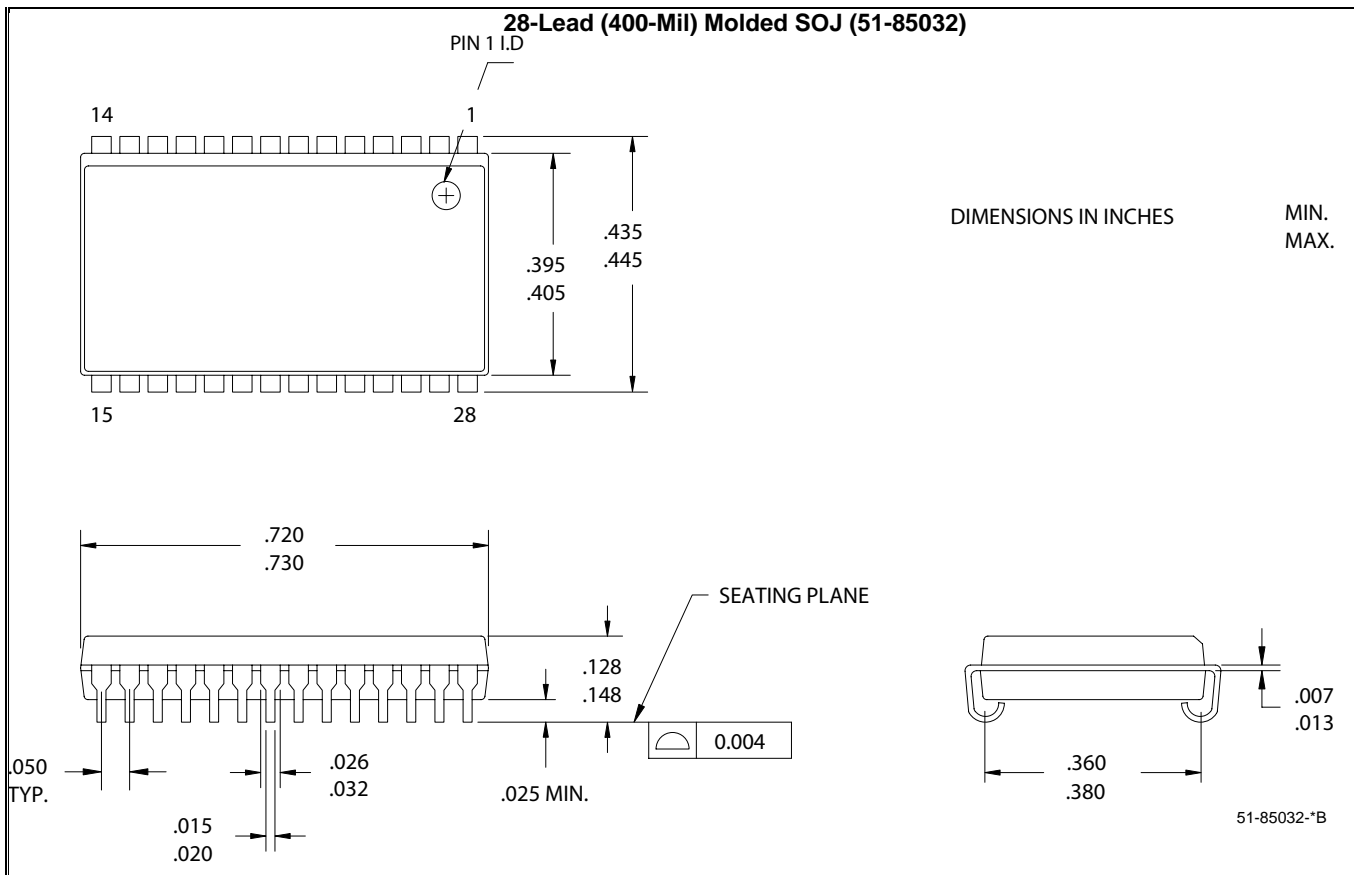
| \overline{CE}_1 | \overline{CE}_2 | \overline{OE} | \overline{WE} | I/O ₀ -I/O ₇ | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|------------------------------------|----------------------------|----------------------------|
| H | X | X | X | High Z | Power-Down | Standby (I _{SB}) |
| X | L | X | X | High Z | Power-Down | Standby (I _{SB}) |
| L | H | L | H | Data Out | Read | Active (I _{CC}) |
| L | H | X | L | Data In | Write | Active (I _{CC}) |
| L | H | H | H | High Z | Selected, Outputs Disabled | Active (I _{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|-----------------|-----------------|-------------------------------|-----------------|
| 12 | CY7C109BN-12VC | 51-85032 | 32-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1009BN-12VC | 51-85031 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109BN-12ZC | 51-85056 | 32-Lead TSOP Type I | |
| | CY7C109BN-12ZXC | 51-85056 | 32-Lead TSOP Type I (Pb-free) | |
| 15 | CY7C109BNL-15VC | 51-85032 | 32-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C109BN-15VC | 51-85032 | 32-Lead (400-Mil) Molded SOJ | |
| | CY7C1009BN-15VC | 51-85031 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109BN-15ZC | 51-85056 | 32-Lead TSOP Type I | |
| | CY7C109BN-15ZXC | 51-85056 | 32-Lead TSOP Type I (Pb-free) | |
| | CY7C109BN-15VI | 51-85032 | 32-Lead (400-Mil) Molded SOJ | Industrial |
| | CY7C1009BN-15VI | 51-85031 | 32-Lead (300-Mil) Molded SOJ | |
| 20 | CY7C109BN-20VC | 51-85032 | 32-Lead (400-Mil) Molded SOJ | Commercial |
| | CY7C1009BN-20VC | 51-85031 | 32-Lead (300-Mil) Molded SOJ | |
| | CY7C109BN-20VI | 51-85032 | 32-Lead (400-Mil) Molded SOJ | Industrial |
| | CY7C109BN-20ZC | 51-85056 | 32-Lead TSOP Type I | Commercial |
| | CY7C109BN-20ZXC | 51-85056 | 32-Lead TSOP Type I (Pb-free) | |

Please contact local sales representative regarding availability of these parts

Package Diagrams

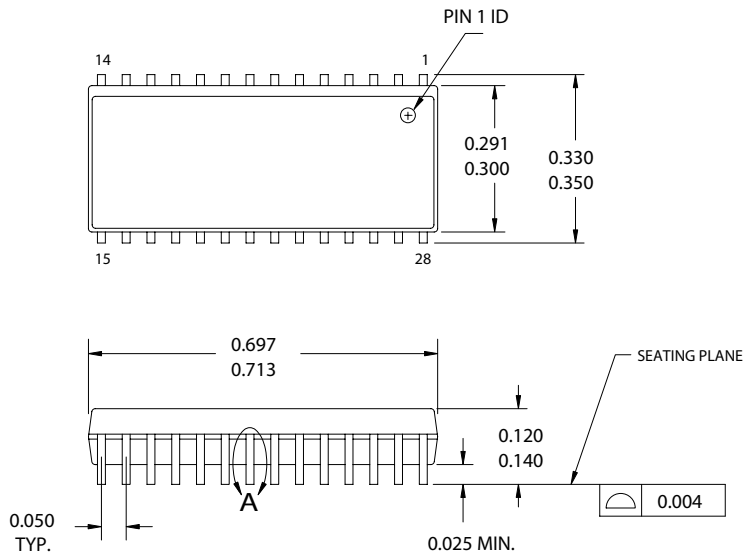


Package Diagrams (continued)

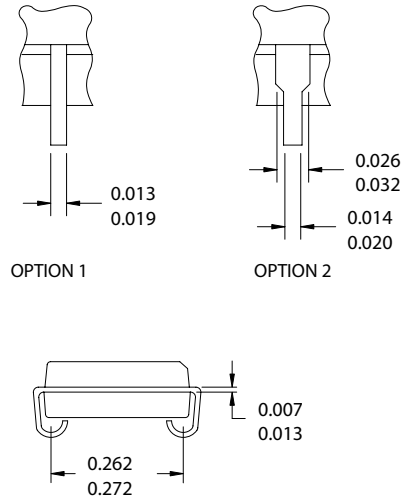
28-Lead (300-Mil) Molded SOJ (51-85031)

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES
MIN.
MAX.



DETAIL A
EXTERNAL LEAD DESIGN

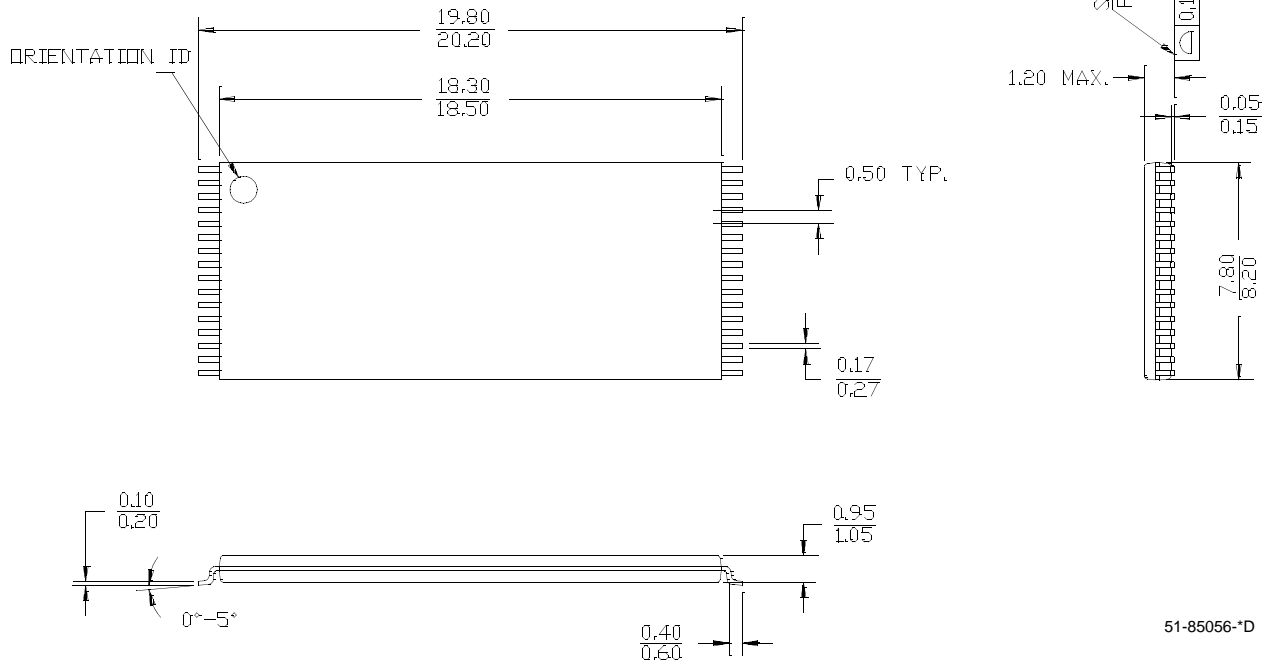


51-85031-°C

32-Lead TSOP I (8x20 mm) (51-85056)

DIMENSION IN MM

MIN.
MAX.



51-85056-°D

All product and company names mentioned in this document may be the trademarks of their respective holders.

Document History Page

| Document Title: CY7C109BN/CY7C1009BN 128K x 8 Static RAM Document Number: 001-06430 | | | | |
|--|----------------|-------------------|------------------------|------------------------------|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 423847 | See ECN | NXR | New Data Sheet |