

## Features

- High Speed
  - $t_{AA} = 15 \text{ ns}$
- Low Active Power
  - 440 mW (maximum 15 ns)
- Low CMOS Standby Power
  - 55 mW (maximum) 4 mW
- 2.0V Data Retention
- Automatic Power Down when deselected
- TTL-compatible Inputs and Outputs
- Easy Memory Expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  options

## Functional Description

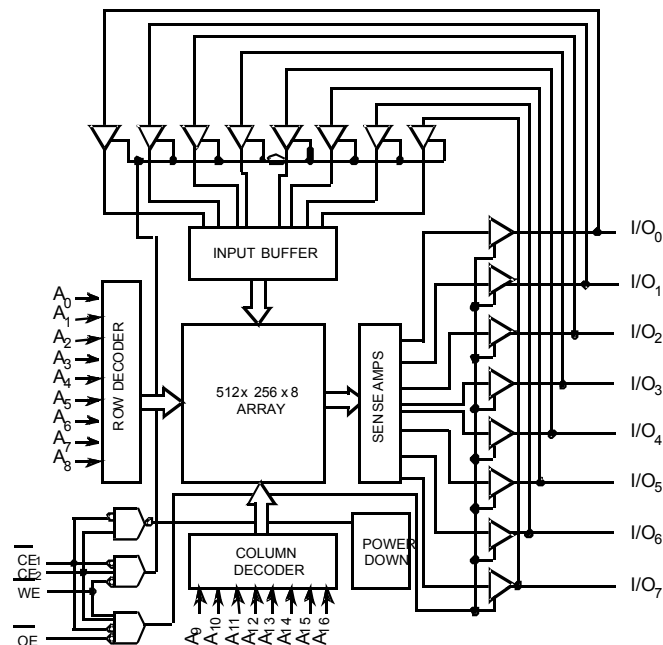
The CY7C109BN/CY7C1009BN<sup>[1]</sup> is a high performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $CE_2$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW and Chip Enable Two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) and Chip Enable Two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The CY7C109BN is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009BN is available in a 300-mil-wide SOJ package. The CY7C1009BN and CY7C109BN are functionally equivalent in all other respects.

## Logic Block Diagram

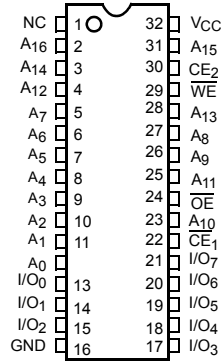


### Note

1. For guidelines on SRAM system design, refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

## Pin Configurations

Figure 1. 32-Pin SOJ (TopView)



## Selection Guide

Description	7C109B-15 7C1009B-15	7C109B-20 7C1009B-20	Unit
Maximum Access Time	15	20	ns
Maximum Operating Current	80	75	mA
Maximum CMOS Standby Current	10	10	mA
	L	2	mA

**Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> ..... -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
- Latch Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C109BN-15 7C1009BN-15		7C109BN-20 7C1009BN-20		Unit
			Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max, V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		80		75	mA
I <sub>SB1</sub>	Automatic CE Power Down Current —TTL Inputs	Max V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>IH</sub> or CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40		30	mA
I <sub>SB2</sub>	Automatic CE Power Down Current —CMOS Inputs	Max V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		10		10	mA
		L		2		2	mA

**Capacitance**

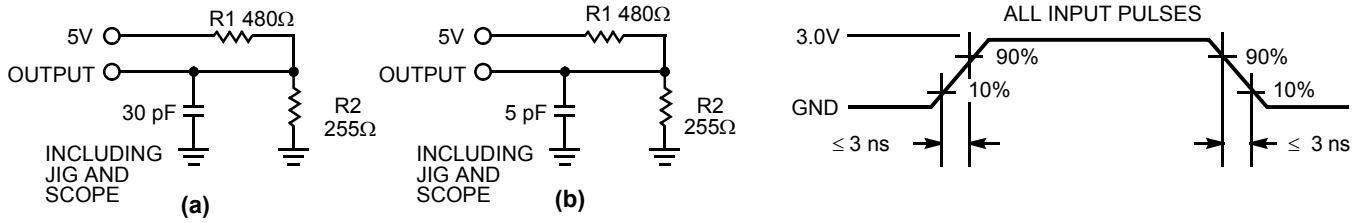
The following are the input and output capacitance test conditions.<sup>[4]</sup>

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Notes**

2. Minimum voltage is -2.0V for pulse durations of less than 20 ns.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

Figure 2. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT  
 OUTPUT ○ — 167Ω — 1.73V

Switching Characteristics<sup>[5]</sup> Over the Operating Range

Parameter	Description	7C109BN-15 7C1009BN-15		7C109BN-20 7C1009BN-20		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	15		20		ns
t <sub>AA</sub>	Address to Data Valid		15		20	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		ns
t <sub>ACE</sub>	CE <sub>1</sub> LOW to Data Valid, CE <sub>2</sub> HIGH to Data Valid		15		20	ns
t <sub>DOE</sub>	OE LOW to Data Valid		7		8	ns
t <sub>LZOE</sub>	OE LOW to Low Z	0		0		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[6, 7]</sup>		7		8	ns
t <sub>LZCE</sub>	CE <sub>1</sub> LOW to Low Z, CE <sub>2</sub> HIGH to Low Z <sup>[7]</sup>	3		3		ns
t <sub>HZCE</sub>	CE <sub>1</sub> HIGH to High Z, CE <sub>2</sub> LOW to High Z <sup>[6, 7]</sup>		7		8	ns
t <sub>PU</sub>	CE <sub>1</sub> LOW to Power Up, CE <sub>2</sub> HIGH to Power Up	0		0		ns
t <sub>PD</sub>	CE <sub>1</sub> HIGH to Power Down, CE <sub>2</sub> LOW to Power Down		15		20	ns
<b>Write Cycle<sup>[8]</sup></b>						
t <sub>WC</sub>	Write Cycle Time <sup>[9]</sup>	15		20		ns
t <sub>SCE</sub>	CE <sub>1</sub> LOW to Write End, CE <sub>2</sub> HIGH to Write End	12		15		ns
t <sub>AW</sub>	Address Setup to Write End	12		15		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	WE Pulse Width	12		12		ns
t <sub>SD</sub>	Data Setup to Write End	8		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[7]</sup>	3		3		ns
t <sub>HZWE</sub>	WE LOW to High Z <sup>[6, 7]</sup>		7		8	ns

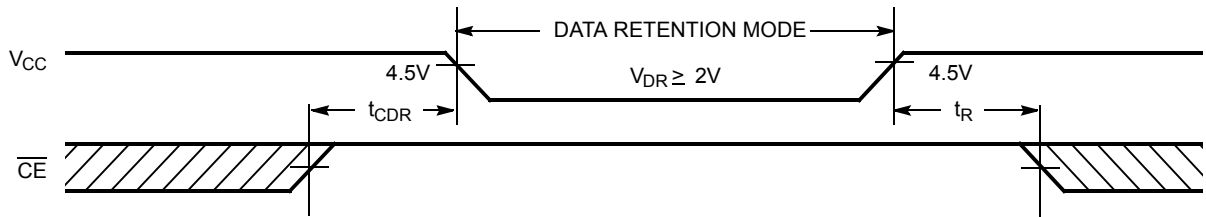
Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of CE<sub>1</sub> LOW, CE<sub>2</sub> HIGH, and WE LOW. CE<sub>1</sub> and WE must be LOW and CE<sub>2</sub> HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Data Retention Characteristics** Over the Operating Range (Low Power version only)

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	No input may exceed $V_{CC} + 0.5V$	2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $CE_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ ,		150	$\mu A$
$t_{CDR}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R$	Operation Recovery Time		200		$\mu s$

Figure 3. Data Retention Waveform



**Switching Waveforms**

Figure 4. Read Cycle No. 1<sup>[10, 11]</sup>

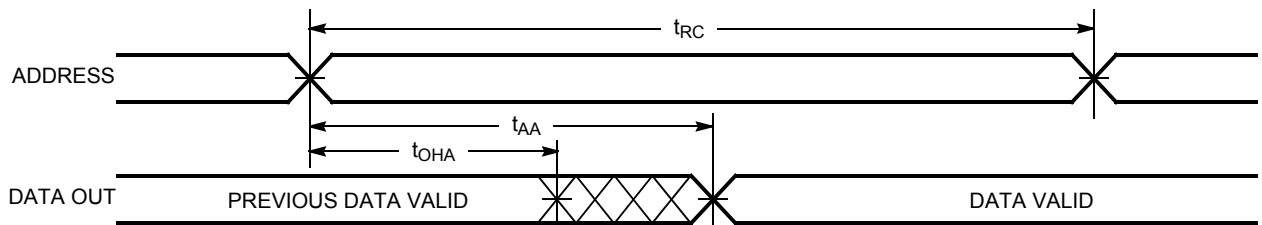
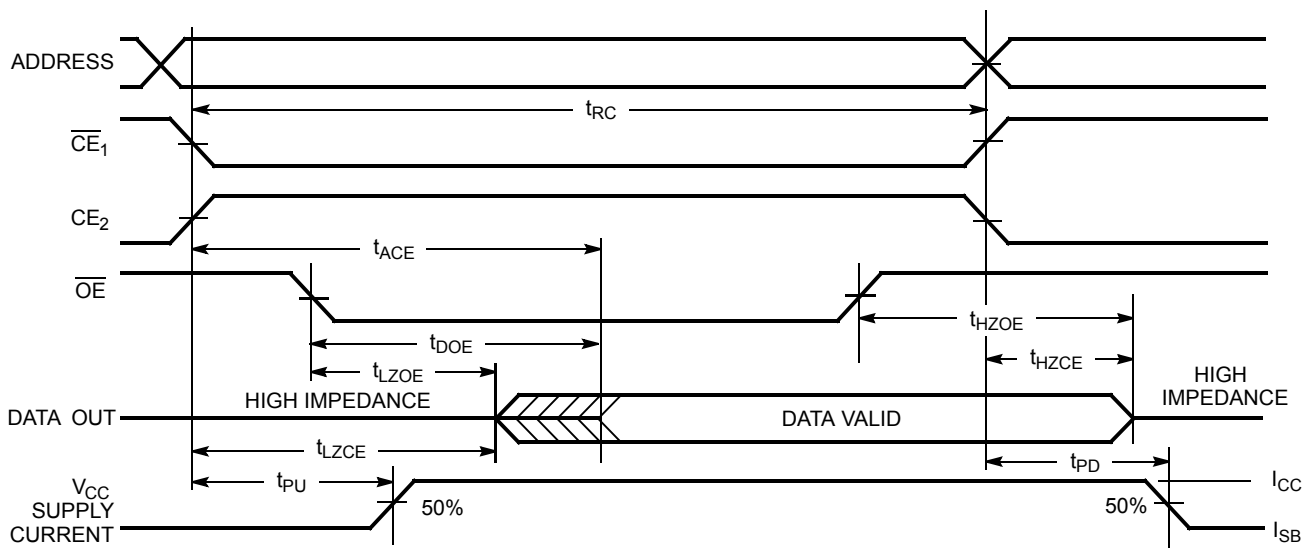


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11, 12]</sup>



**Notes**

- 10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 11. WE is HIGH for read cycle.
- 12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[13, 14]</sup>

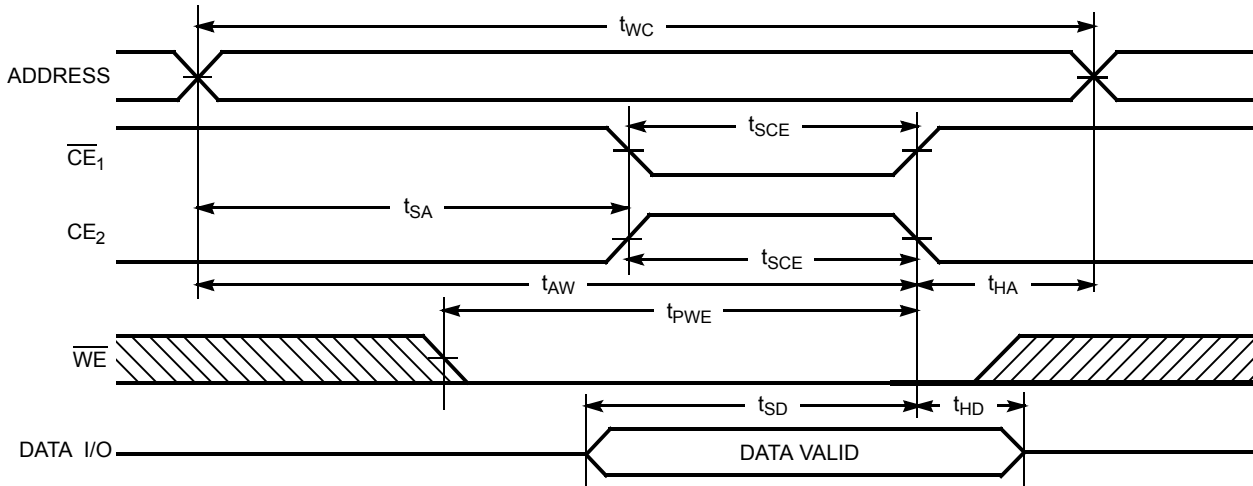
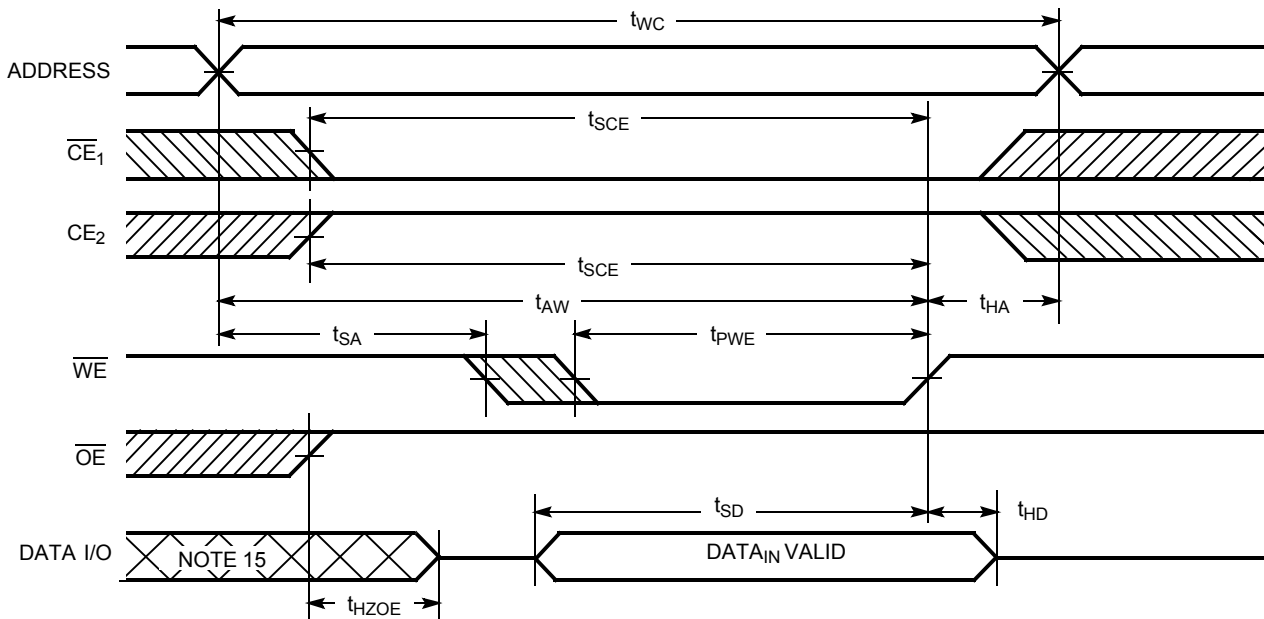


Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13, 14]</sup>

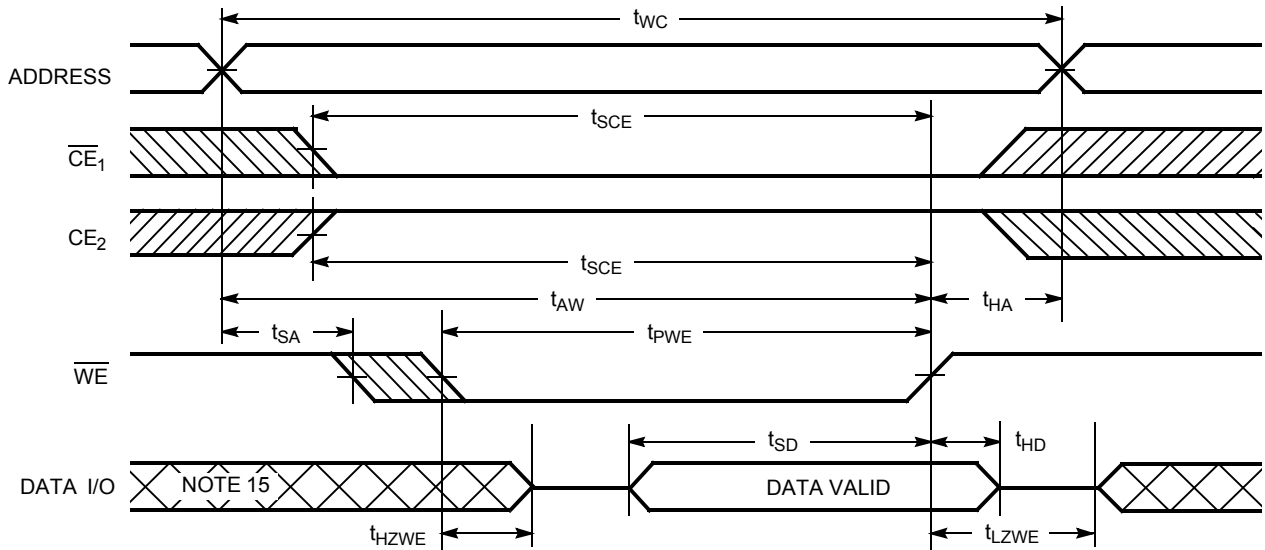


Notes

- 13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 14. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 15. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14]</sup>



Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power Down	Standby (I <sub>SB</sub> )
X	L	X	X	High Z	Power Down	Standby (I <sub>SB</sub> )
L	H	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	H	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

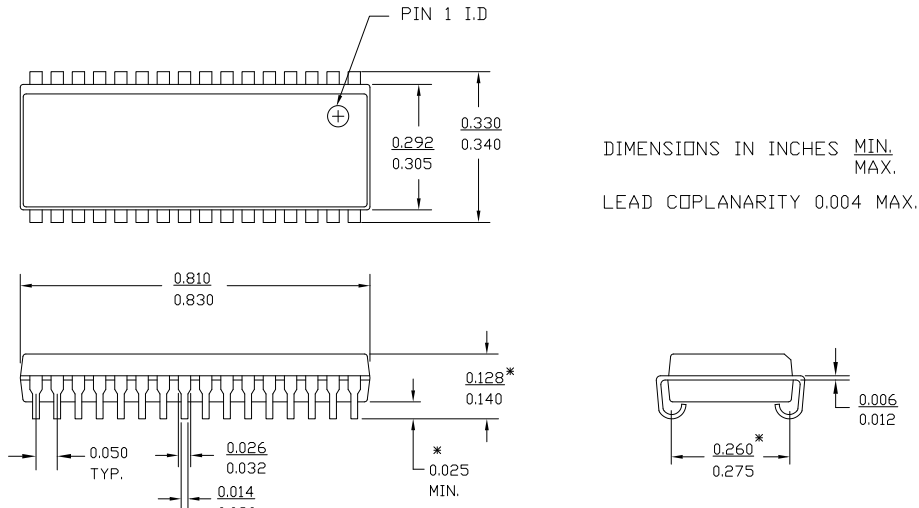
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1009BN-15VI	51-85041	32-Pin (300-Mil) Molded SOJ	Industrial
20	CY7C109BN-20VI	51-85033	32-Pin (400-Mil) Molded SOJ	Industrial

Contact your local sales representative regarding availability of these parts

Package Diagrams

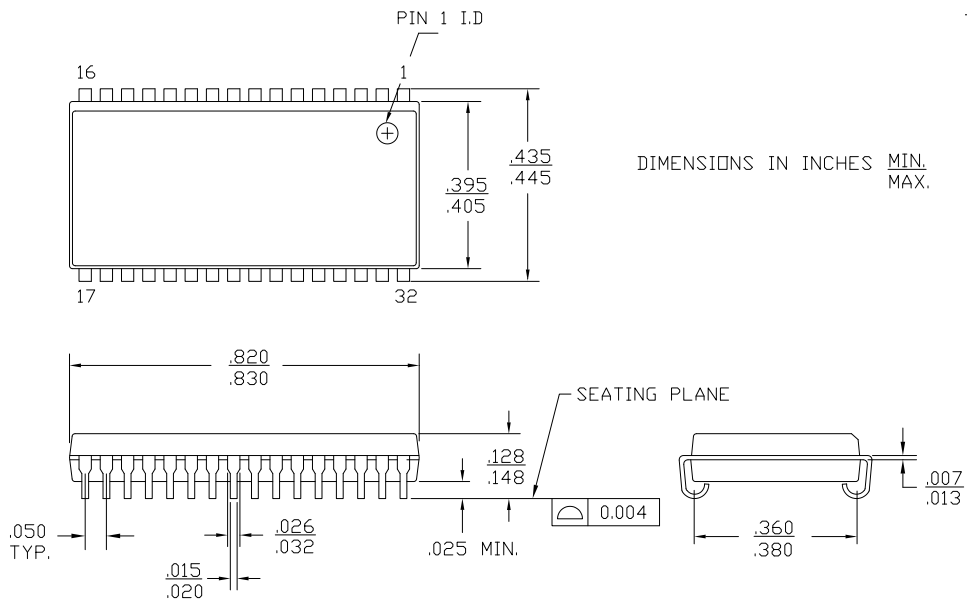
Figure 9. 32-Pin (300-Mil) Molded



51-85041 \*B

Figure 10. 32-Pin (400-Mil) Molded SOJ

32 Lead (400 MIL) Molded SOJ V33



51-85033 \*C



## Document History Page

Document Title: CY7C109BN/CY7C1009BN 128K x 8 Static RAM				
Document Number: 001-06430				
REV.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	423847	NXR	See ECN	New Data Sheet
*A	2755340	NXR	08/24/2009	Removed -12 from product offering as 12ns parts are not active Corrected Package Diagram Updated ordering Information
*B	2904565	AJU	04/05/10	Removed inactive part number from the ordering information table. Updated package diagrams.

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