1-Mbit (128 K × 8) Static RAM

Features

- Pin- and function-compatible with CY7C1018CV33
- High speed
  - t_{AA} = 10 ns
- Low Active Power
  - I_{CC} = 60 mA @ 10 ns
- Low CMOS Standby Power
  - I_{SB2} = 3 mA
- 2.0V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Center power/ground pinout
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Available in Pb-free 32-pin 300-Mil wide Molded SOJ

Functional Description

The CY7C1018DV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

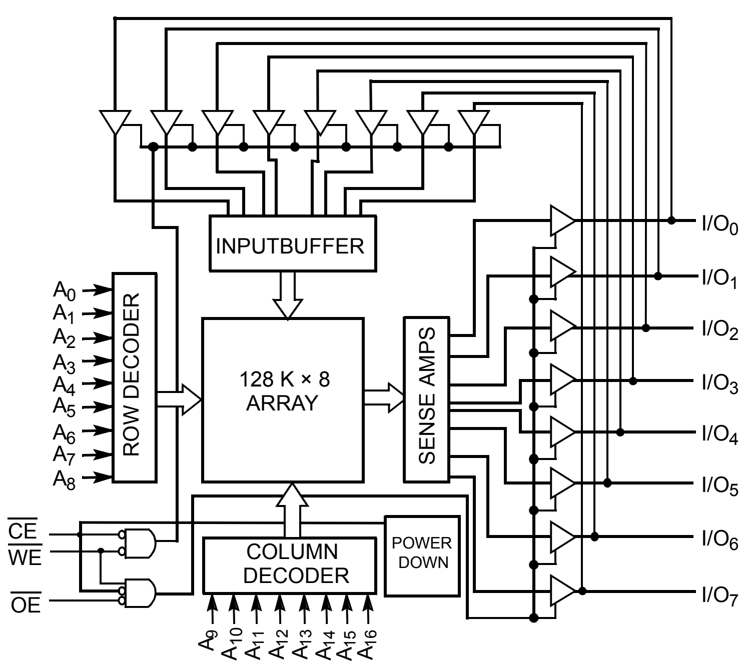
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1018DV33 is available in Pb-free 32-pin 300-Mil wide Molded SOJ.

Logic Block Diagram



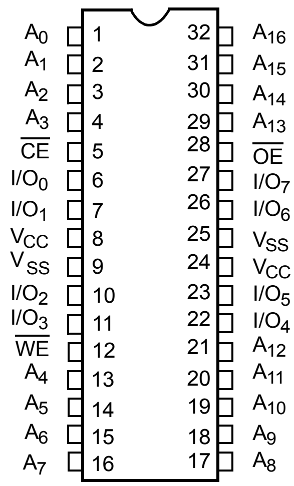
Contents

Selection Guide

	-10 (Industrial)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	60	mA
Maximum Standby Current	3	mA

Pin Configuration

Figure 1. 32-pin SOJ Top View



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with
Power Applied .... –55 °C to +125 °C

Supply Voltage on
V_{CC} to Relative GND [1] ....–0.3 V to + 4.6 V

DC Voltage Applied to Outputs [1]
in High Z State ....–0.3 V to V_{CC} + 0.3 V

DC Input Voltage [1] ....–0.3 V to V_{CC} + 0.3 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .... > 2001V

Latch-up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V	10 ns

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10 (Industrial)		Unit
				Min	Max	
V_{OH}	Output HIGH Voltage	Min V_{CC}, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW Voltage	Min V_{CC}, I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage [1]			–0.3	0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_{IN} \leq V_{CC}$		–1	+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_{IN} \leq V_{CC}$, Output Disabled		–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	100 MHz	–	60	mA
			83 MHz	–	55	mA
			66 MHz	–	45	mA
			40 MHz	–	30	mA
I_{SB1}	Automatic CE Power-down Current–TTL Inputs	Max V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}		–	10	mA
I_{SB2}	Automatic CE Power-down Current–CMOS Inputs	Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3 V, $V_{IN} \geq V_{CC}$ – 0.3 V or $V_{IN} \leq$ 0.3 V, f = 0		–	3	mA

Note
1. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 1 V for pulse durations of less than 5 ns.

Capacitance

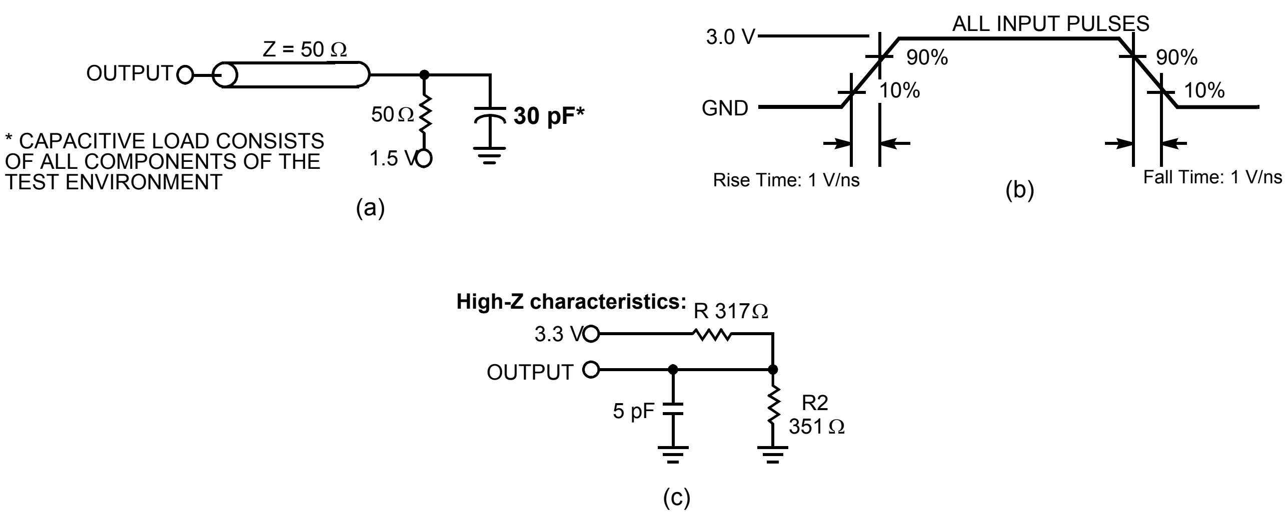
Parameter [2]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter [2]	Description	Test Conditions	32-pin SOJ	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.61	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		40.53	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [3]



Notes
2. Tested initially and after any design or process changes that may affect these parameters.
3. AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

AC Switching Characteristics

Over the Operating Range

Parameter [4]	Description	-10 (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{power}[5]	V_{CC}(typical) to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [6]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [6, 7]	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [6]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [6, 7]	–	5	ns
t_{PU}[8]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}[8]	$\overline{CE}$ HIGH to power-down	–	10	ns
Write Cycle [9, 10]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	8	–	ns
t_{AW}	Address set-up to write end	8	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data set-up to write end	5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [6]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [6, 7]	–	5	ns

Notes

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
5. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.
8. This parameter is guaranteed by design and is not tested.
9. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
10. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

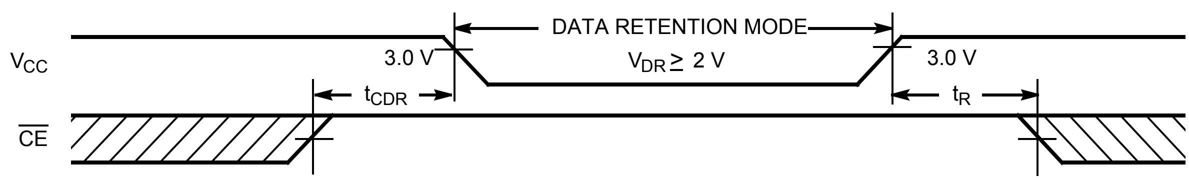
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	3	mA
t_{CDR} [11]	Chip Deselect to Data Retention Time		0	–	ns
t_R[12]	Operation Recovery Time		t_{RC}	–	ns

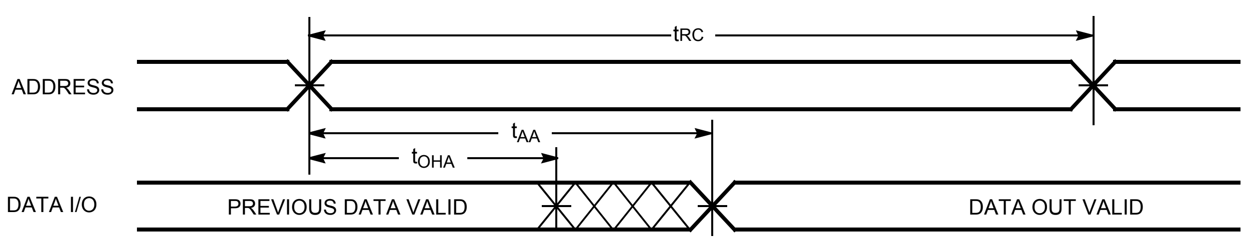
Data Retention Waveform

Figure 3. Data Retention Waveform



Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [13, 14]



Notes

11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.
13. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
14. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [15, 16]

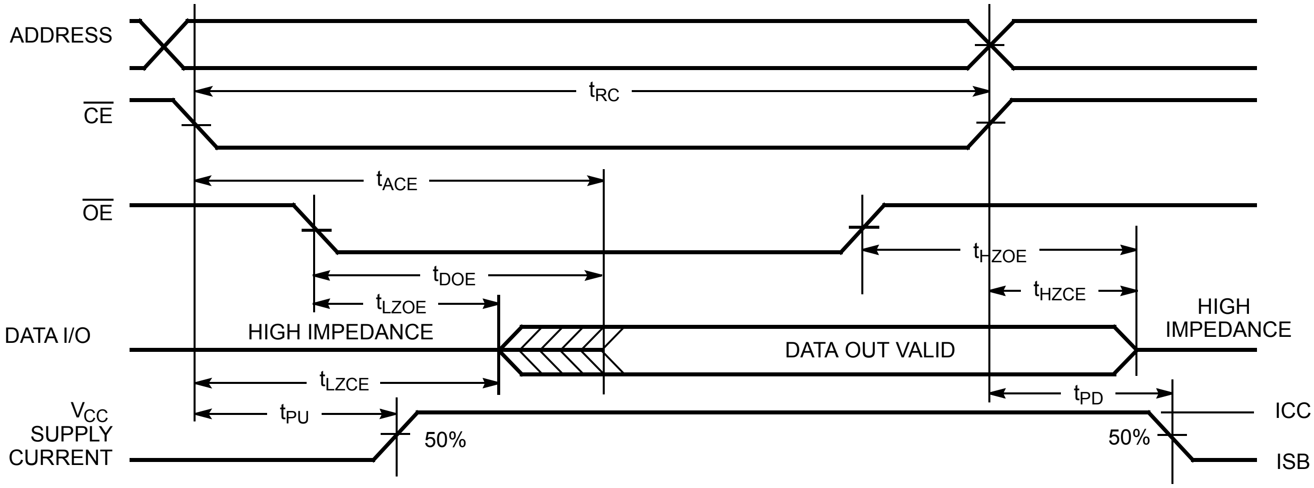
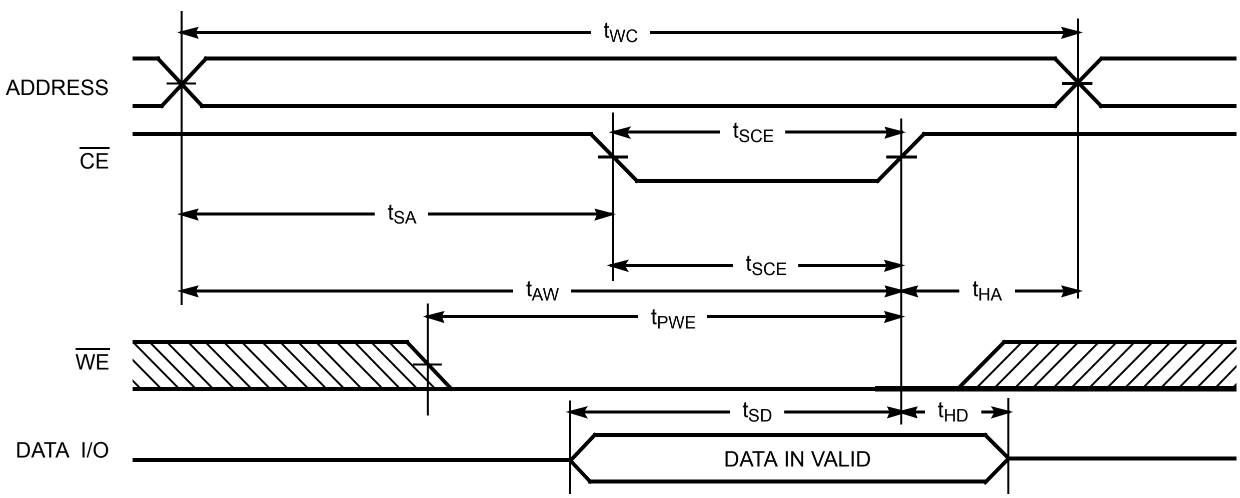


Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18]



Notes

15. $\overline{WE}$ is HIGH for Read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [19, 20]

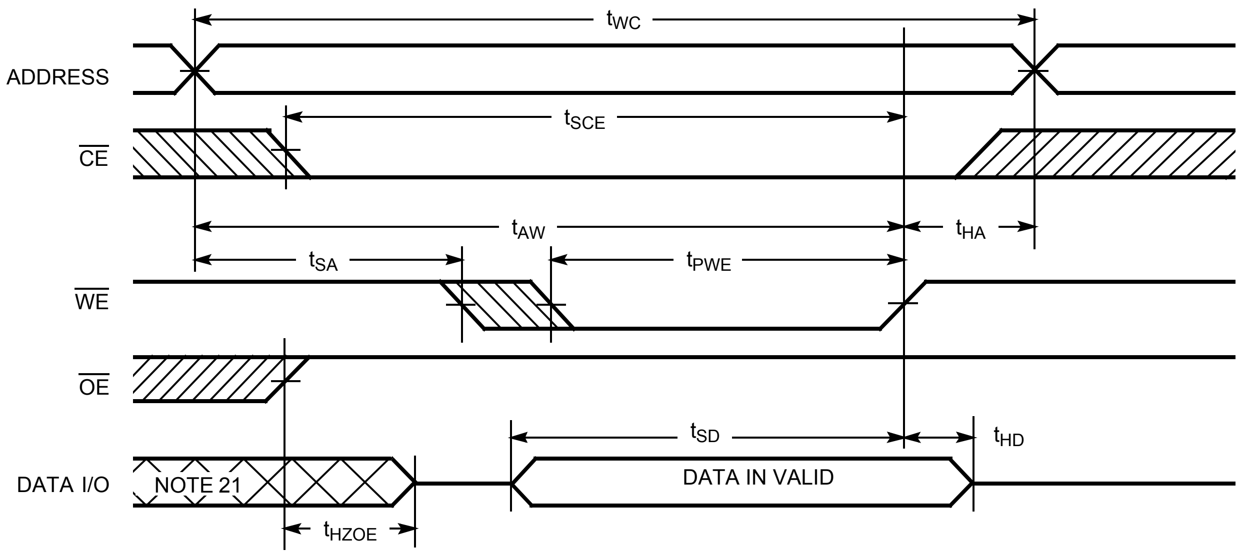
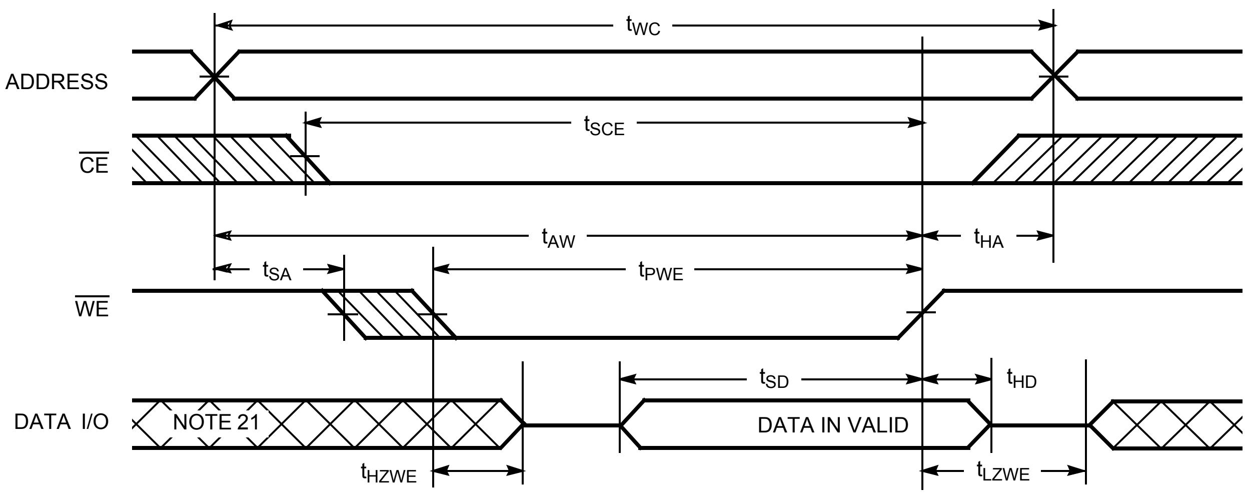


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [20, 22]



Notes

19. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
20. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
21. During this period the I/Os are in the output state and input signals should not be applied.
22. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1018DV33-10VXI	51-85041	32-pin (300-Mil) Molded SOJ (Pb-free)	Industrial

Ordering Code Definitions

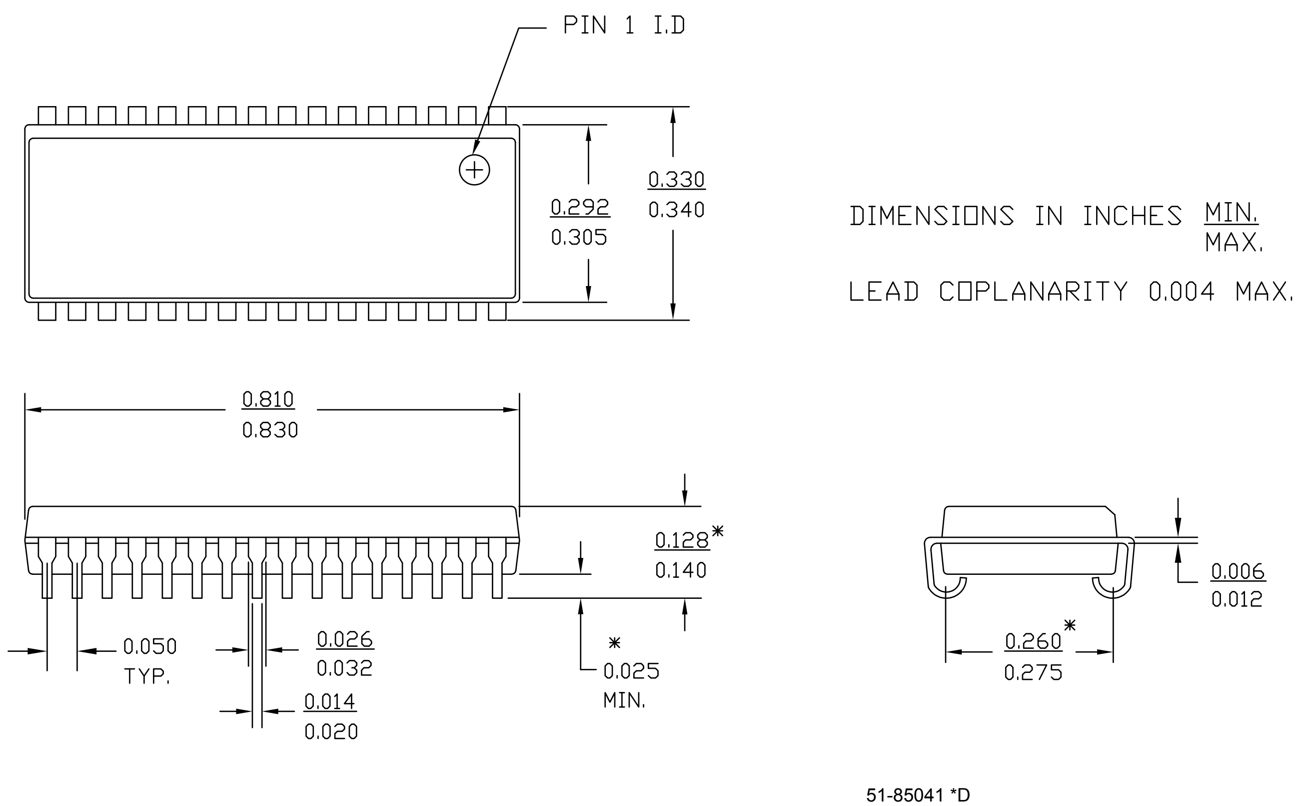
CY 7 C 1 01 8 D V33 - 10 V X I

- I — Temperature Range: I = Industrial
- X — Pb-free
- V — Package Type: V = 32-pin Molded SOJ
- 10 — Speed: 10 ns
- V33 — Voltage range: V33 = 3 V to 3.6 V
- D — Process Technology: D = C9, 90 nm
- 8 — Bus width: × 8
- 01 — 01 = 1-Mbit density
- 1 — 1 = Fast Asynchronous SRAM family
- C — Technology Code: C = CMOS
- 7 — Marketing Code: 7 = SRAM
- CY — Company ID: CY = Cypress

Please contact your local Cypress sales representative for availability of these parts.

Package Diagram

Figure 9. 32-pin SOJ (300 Mils) V32.3 (Catalog 32.3 Molded SOJ) Package Outline, 51-85041



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1018DV33, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05465				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	238471	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in the Ordering Information
*B	262950	See ECN	RKF	Added Data Retention Characteristics table Added T_{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307598	See ECN	RKF	Reduced Speed bins to -8 and -10 ns
*D	520647	See ECN	VKN	Changed status from Preliminary to Final. Removed Commercial Operating range Removed 8 ns speed bin Added I_{CC} values for the frequencies 83 MHz, 66 MHz and 40 MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V_{CC} + 2 V to V_{CC} + 1 V in footnote #2
*E	3104943	12/08/2010	AJU	Added Ordering Code Definitions. Updated Package Diagram.
*F	3414435	10/19/2011	TAVA	Updated Functional Description (Removed the Note “For guidelines on SRAM system designs, please refer to the ‘System Design Guidelines’ Cypress application note, available on the internet at www.cypress.com.” and its reference in Functional Description. Updated DC Electrical Characteristics. Updated Switching Waveforms. Updated Package Diagram. Added Acronyms and Units of Measure. Updated to new template.
*G	4578060	11/24/2014	MEMJ	Updated Package Diagram: spec 51-85041 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.

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