12-Bit Integrated Multiformat SDTV/HDTV Video Decoder and RGB Graphics Digitizer

ADV7402

FEATURES

Three 110 MHz Noise Shaped Video® 12-bit ADCs
1.8 V digital core, 3.3 V analog and digital I/O power supplies
12 analog input channel mux
NTSC/PAL/SECAM color standards support
525p/625p/720p/1080i component HDTV support
Digitizes RGB graphics up to 1280 ×1024 @ 60 Hz (SXGA)
24-bit digital input port supports data from DVI/HDMI Rx IC
Any-to-any 3 × 3 color space conversion matrix

APPLICATIONS

LCD/DLP™ rear projection HDTVs
PDP HDTVs
CRT HDTVs
LCD/DLP front projectors
LCD TV (HDTV ready)
HDTV STBs with PVR
Hard disk based video recorders
Multiformat scan converters
DVD recorders with progressive scan input support

GENERAL DESCRIPTION

The ADV7402 is a high quality, single chip, multiformat video decoder and graphics digitizer. This multiformat decoder supports the conversion of PAL, NTSC, and SECAM standards in the form of composite or S-video into a digital ITU-R BT.656 format. The ADV7402 also supports the decoding of a component RGB/YPrPb video signal into a digital YCrCb or RGB pixel output stream. The support for component video includes standards such as 525i, 625i, 525p, 625p, 720p, 1080i, 1250i, and many other HD and SMPTE standards. Graphic digitization is also supported by the ADV7402; it is capable of digitizing RGB graphics signals from VGA to SXGA rates and converting them into a digital RGB or YCrCb pixel output stream.

The ADV7402 contains two main processing sections. The first is the standard definition processor (SDP), which processes all PAL, NTSC, and SECAM signal types. The second is the component processor (CP), which processes YPrPb and RGB component formats, including RGB graphics. For more specific descriptions of the ADV7402 features, see the Detailed Functionality and Detailed Description sections.

FUNCTIONAL BLOCK DIAGRAM

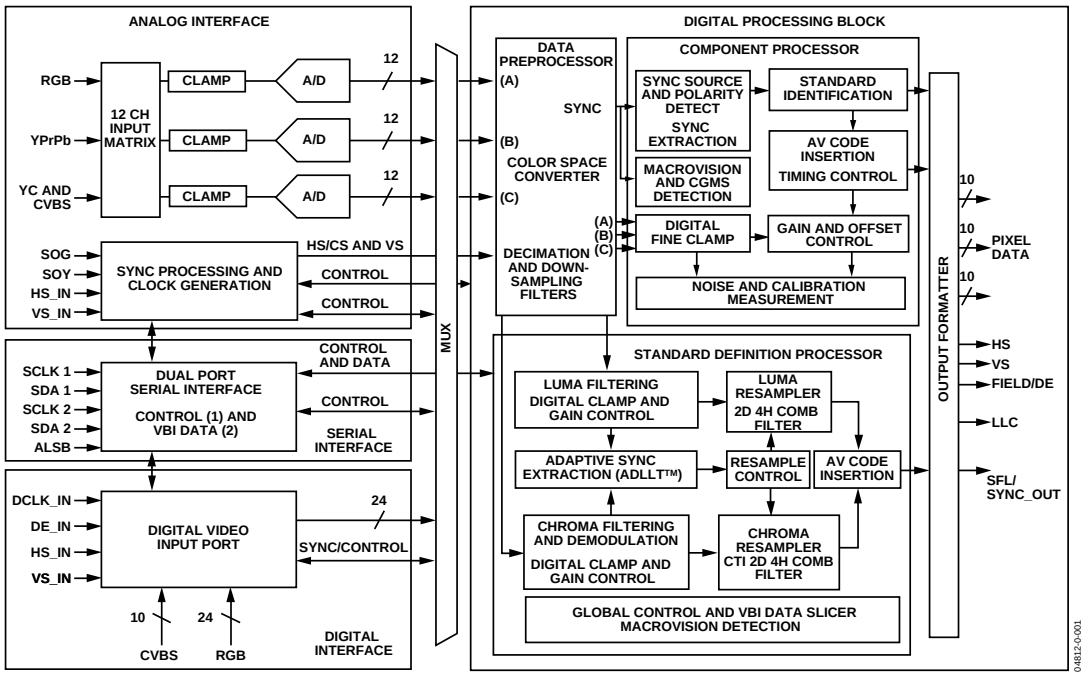

Figure 1.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

5/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS[1, 2]

@ AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.65 V to 2.0 V, nominal input range 1.6 V. Operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[3]						
Resolution (each ADC)	N				12	Bits
Integral Nonlinearity	INL	BSL at 27 MHz (at a 12-bit level)		±2.0	±8.0	LSB
Integral Nonlinearity	INL	BSL at 54 MHz (at a 12-bit level)		−2.0/+2.5		LSB
Integral Nonlinearity	INL	BSL at 74 MHz (at a 10-bit level)		−0.75/+1.0		LSB
Integral Nonlinearity	INL	BSL at 110 MHz (at a 10-bit level)		−3.0/+5.8		LSB
Differential Nonlinearity	DNL	At 27 MHz (at a 12-bit level)		−0.7/+0.85	−0.95/+2.5	LSB
Differential Nonlinearity	DNL	At 54 MHz (at a 12-bit level)		−0.75/+0.9		LSB
Differential Nonlinearity	DNL	At 74 MHz (at a 10-bit level)		±0.5		LSB
Differential Nonlinearity	DNL	At 110 MHz (at a 10-bit level)		−0.7/+5.0		LSB
DIGITAL INPUTS[4]						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}	HS_IN, VS_IN low trigger mode	0.7			V
Input Low Voltage	V_{IL}	HS_IN, VS_IN low trigger mode			0.4	V
Input Current	I_{IN}	Pins listed in Note 5	−60		+60	µA
		All other pins	−10		+10	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}	Pins listed in Note 6			60	µA
		All other pins			10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS						
Digital Core Power Supply	D_{VDD}		1.65	1.8	2	V
Digital I/O Power Supply	D_{VDDIO}		3.0	3.3	3.6	V
PLL Power Supply	P_{VDD}		1.65	1.8	2	V
Analog Power Supply	A_{VDD}		3.15	3.3	3.45	V
Digital Core Supply Current	I_{DVDD}	CVBS I/P sampling at 54 MHz		82		mA
		Graphics RGB sampling at 110 MHz		62		mA
Digital I/O Supply Current	I_{DVDDIO}	CVBS I/P sampling at 54 MHz		2		mA
		Graphics RGB sampling at 110 MHz		17		mA
PLL Supply Current	I_{PVDD}	54 MHz		10.5		mA
		110 MHz		6		mA
Analog Supply Current	I_{AVDD}	CVBS I/P sampling at 54 MHz		85		mA
		Graphics RGB sampling at 110 MHz		218		mA
Power-Down Current	I_{PWRDN}			1.5		mA
Green Mode Power-Down	I_{PWRDNG}	Sync bypass function		12.5		mA
Power-Up Time	T_{PWRUP}			20		ms

[1] The min/max specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: −25°C to +70°C.
[3] All ADC linearity tests performed at input range of full scale − 12.5%, and at zero scale + 12.5%.
[4] Guaranteed by characterization.
[5] Pins: 1, 2, 3, 13, 14, 16, 19, 24, 29, 30, 31, 32, 33, 34, 35, 45, 79, 83, 84, 87, 88, 95, 96, 97, 100.
[6] Pins: 4, 7, 8, 9, 10, 13, 14, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 41, 42, 43, 44, 45, 83, 84, 87, 88, 91, 92, 93, 94, 95, 96, 97, 98, 99.

VIDEO SPECIFICATIONS[1, 2, 3]

@ AVDD= 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.65 V to 2.0 V.
Operating temperature range, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS I/P, modulated 5 step		0.4	0.6	degree
Differential Gain	DG	CVBS I/P, modulated 5 step		0.4	0.6	%
Luma Nonlinearity	LNL	CVBS I/P, 5 step		0.4	0.7	%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp	61	63		dB
SNR Unweighted		Luma flat field	64	65		dB
Analog Front End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
F_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock in Time				60		line
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		field
Horizontal Lock Time				100		line
CHROMA SPECIFICATIONS						
Hue Accuracy	HUE			1		degree
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.4		%
Chroma Phase Error				0.3		degree
Chroma Luma Intermodulation				0.1		%
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V I/P		1		%
Luma Contrast Accuracy		CVBS, 1 V I/P		1		%

[1] The min/max specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: −25°C to +70°C.
[3] Guaranteed by characterization.

TIMING CHARACTERISTICS[1, 2, 3]

@ AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.65 V to 2.0 V. Operating temperature range, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Crystal Nominal Frequency				27.0		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			14.8		110	kHz
LLC1 Frequency Range			12.825		110	MHz
I^2C PORT						
SCLK Frequency					400	kHz
SCLK Min Pulse Width High	t_1		0.6			µs
SCLK Min Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Time	t_6				300	ns
SCLK and SDA Fall Time	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC1 Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA and CONTROL OUTPUTS						
Data Output Transition Time (SDP)	t_{11}	Negative clk edge to valid data			6	ns
Data Output Transition Time (SDP)	t_{12}	Negative clk edge to invalid data			−0.6	ns
Data Output Transition Time (CP)	t_{13}	Invalid data to negative clk edge			2.2	ns
Data Output Transition Time (CP)	t_{14}	Negative clk edge to valid edge			1.1	ns
DATA and CONTROL INPUTS						
Input Setup Time	t_{19}	HS_IN, VS_IN	9			ns
		DE_IN, Data inputs	2.5			ns
Input Hold Time	t_{20}	HS_IN, VS_IN	7			ns
		DE_IN, Data inputs	0.5			ns

[1] The min/max specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}:−25°C to +70°C.
[3] Guaranteed by characterization.

ANALOG SPECIFICATIONS[1, 2, 3]

@ AVDD = 3.1.5 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.65 V to 2.0 V.
Operating temperature range, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY						
External Clamp Capacitor				0.1		µF
Input Impedance		Clamps switched off		10		MΩ
Voltage Clamp Level				1.7		V
Large Clamp Source Current		SDP only		0.75		mA
Large Clamp Sink Current		SDP only		0.75		mA
Fine Clamp Source Current		SDP only		60		µA
Fine Clamp Sink Current		SDP only		60		µA

[1] The min/max specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}:–25°C to +70°C.
[3] Guaranteed by characterization.

THERMAL SPECIFICATIONS

Table 5.

Thermal Characteristics	Symbol	Test Conditions	Typ	Unit
Junction-to-Case Thermal Resistance	θ_C	4-layer PCB with solid ground plane	7	°C/W
Junction-to-Ambient Thermal Resistance	θ_{JA}	4-layer PCB with solid ground plane (still air)	30	°C/W

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AGND	4 V
DVDD to DGND	2.2 V
PVDD to AGND	2.2 V
DVDDIO to DGND	4 V
DVDDIO to AVDD	−0.3 V to +0.3V
PVDD to DVDD	−0.3 V to +0.3 V
DVDDIO – PVDD	−0.3 V to +2 V
DVDDIO – DVDD	−0.3 V to +2 V
AVDD – PVDD	−0.3 V to +2 V
AVDD – DVDD	−0.3 V to +2 V
Analog Inputs to AGND	AGND − 0.3 V to AVDD + 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	150°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 secs)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

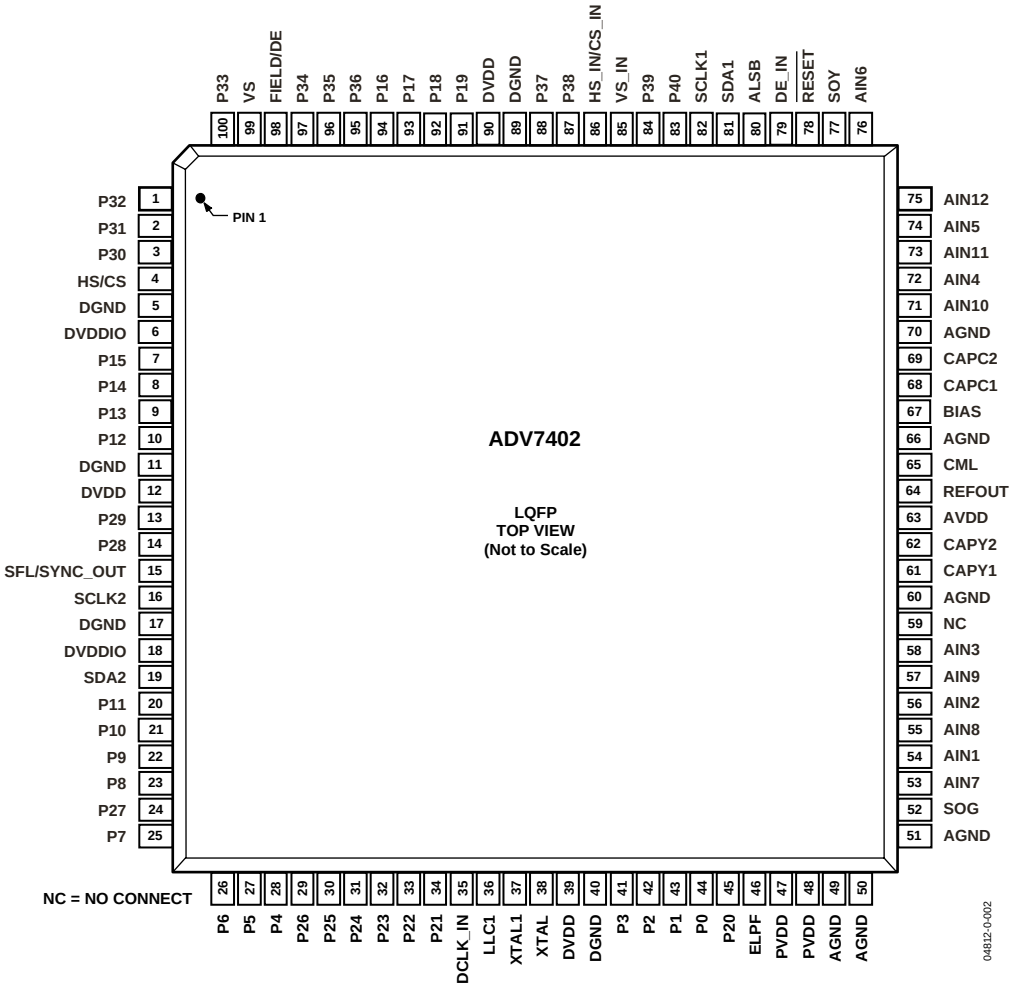

Figure 2. LQFP Top View (not to scale)

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Function
5, 11, 17, 40, 89	DGND	G	Digital ground
49, 50, 51, 60, 66, 70	AGND	G	Analog ground
6, 18	DVDDIO	P	Digital I/O supply voltage (3.3 V).
12, 39, 90	DVDD	P	Digital core supply voltage (1.8 V).
63	AVDD	P	Analog supply voltage (3.3 V).
47, 48	PVDD	P	PLL supply voltage (1.8 V).
54, 56, 58, 72, 74, 76, 53, 55, 57, 71, 73, 75	AIN1–AIN12	I	Analog video input channels.
42, 41, 28, 27, 26, 25, 23, 22, 10, 9, 8, 7, 94, 93, 92, 91	P2–P9, P12–P19	O	Video pixel output port.
44, 43, 21, 20, 45, 34, 33, 32, 31, 30, 29, 24, 14, 13	P0–P1, P10–P11, P20–P29	I/O	Video pixel input/output port.
2, 1, 100, 97, 96, 95, 88, 87, 84, 83	P31–P40	I	Video pixel input port.

Pin No.	Mnemonic	Type	Function
3	P30	NC	No connect pin; this pin can be tied to AGND or AVDD.
4	HS/CS	O	HS is a horizontal synchronization output signal in SDP and CP modes. CS is a digital composite synchronization signal that can be selected while in CP mode.
99	VS	O	VS is a vertical synchronization output signal in SDP and CP modes.
98	FIELD/DE	O	FIELD is a field synchronization output signal in all interlaced video modes. This pin also can be enabled as a DE (data enable) signal in CP mode to allow direct connection to a HDMI/DVI Tx IC.
81, 19	SDA1, SDA2	I/O	I^2C port serial data input/output pin, SDA1 is the data line for the Control port and SDA2 is the data line for the VBI readback port.
82, 16	SCLK1, SCLK2	I	I^2C port serial clock input (max clock rate of 400 kHz). SCLK1 is the clock line for the Control port and SCLK2 is the clock line for the VBI data readback port.
80	ALSB	I	This pin selects the I^2C address for the ADV7402 Control and VBI readback ports. ALSB set to a Logic 0 sets the address for a write to control port of 0x40 and the readback address for the VBI port of 0x21. ALSB set to a logic high sets the address for a write to control port of 0x42 and the readback address for the VBI port of 0x23.
78	$\overline{\text{RESET}}$	I	System reset input, active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7402 circuitry.
36	LLC1	O	This is a line-locked output clock for the pixel data output by the ADV7402 (range is 13.5 MHz to 110 MHz).
38	XTAL	I	Input pin for 27 MHz crystal, or can be overdriven by an external 3.3 V 27 MHz clock oscillator source to clock the ADV7402.
37	XTAL1	O	This pin should be connected to the 27 MHz crystal or left as a no connect if an external 3.3 V 27 MHz clock oscillator source is used to clock the ADV7402. In crystal mode the crystal must be a fundamental crystal.
46	ELPF	O	The recommend external loop filter must be connected to this ELPF pin.
15	SFL/SYNC_OUT	O	SFL (Subcarrier Frequency Lock); this pin contains a serial output stream which can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder. SYNC_OUT is the sliced sync output signal only available in CP mode.
64	REFOUT	O	Internal voltage reference output.
65	CML	O	The CML pin is a common-mode level for the internal ADCs.
61, 62	CAPY1–CAPY2	I	ADC capacitor network.
68, 69	CAPC1–CAPC2	I	ADC capacitor network.
67	BIAS	O	BIAS is an external bias setting pin. Connect the recommended resistor between pin and ground.
86	HS_IN/CS_IN	I	Can be configured in CP mode to be either a digital HS input signal or a digital CS input signal used to extract timing in a 5-wire or 4-wire RGB mode.
85	VS_IN	I	VS input signal used in CP mode for 5-wire timing mode.
79	DE_IN	I	DE_IN is a data enable input signal used in 24-bit digital input port mode, for example, 24-bit RGB data from a DVI Rx IC.
59	NC	NC	No connect pin; this pin can be tied to AGND or AVDD.
35	DCLK_IN	I	Clock input signal used in 24-bit digital input mode and also in digital CVBS input mode.
52	SOG	I	SOG is a sync on green input used in embedded sync mode.
77	SOY	I	SOY is a sync on luma input used in embedded sync mode.

DETAILED FUNCTIONALITY

ANALOG FRONT END

- Three 110 MHz Noise Shaped Video 12-bit ADCs enable the industry's first true 10-bit video decoder.
- 12 analog input channel mux enables multisource connection without the requirement of an external mux.
- Three current and voltage clamp control loops ensure any dc offsets are removed from the video signal.

SDP PIXEL DATA OUTPUT MODES

- 8-/10-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD
- 16-/20-bit YCrCb with embedded time codes and/or HS, VS, and FIELD
- 24-/30-bit YCrCb with embedded time codes and/or HS, VS, and FIELD

CP PIXEL DATA OUTPUT MODES

- Single data rate (SDR) 16-/20-bit 4:2:2 YCrCb for all standards
- Single data rate (SDR) 24-/30-bit 4:4:4 YCrCb/RGB for all standards

COMPOSITE AND S-VIDEO PROCESSING

- Support for NTSC (J, M, 4.43), PAL (B, D, I, G, H, M, N, Nc 60) and SECAM B/D/G/K/L standards in the form of CVBS and S-video
- Super adaptive 2D 5-line comb filters for NTSC and PAL give superior chrominance and luminance separation for composite video
- Full automatic detection and autoswitching of all worldwide standards (PAL/NTSC/SECAM)
- Automatic gain control with white peak mode ensures the video is always processed without loss of the video processing range.
- Adaptive digital line length tracking (ADLLT™)
- Proprietary architecture for locking to weak, noisy, and unstable sources from VCRs and tuners.
- Chroma transient improvement (CTI)
- Luminance digital noise reduction (DNR)
- Color controls include hue, brightness, saturation, contrast, and Cr and Cb offset controls
- Certified Macrovision® copy protection detection on composite and S-video for all worldwide formats (PAL/NTSC/SECAM)
- 4× oversampling (54 MHz) for CVBS and S-video modes
- Line-locked clock output (LLC)
- Letterbox detection supported
- Free-run output mode provides stable timing when no video input is present
- Vertical blanking interval data processor
- Closed captioning (CC) and extended data service (EDS)
- Wide screen signaling (WSS)
- Copy generation management system (CGMS)
- EDTV
- Gemstar™ 1×/2× electronic program guide compatible
- Clocked from a single 27 MHz crystal
- Subcarrier frequency lock (SFL) output for downstream video encoder
- Differential gain typically 0.4%
- Differential phase typically 0.4°

COMPONENT VIDEO PROCESSING

- Formats supported include 525i, 625i, 525p, 625p, 720p, 1080i, and many other HDTV formats
- Automatic adjustments include gain (contrast) and offset (brightness); manual adjustment controls are also supported
- Support for analog component YPrPb/RGB video formats with embedded sync or with separate HS, VS, or CS
- Any-to-any 3 × 3 color space conversion matrix supports YCrCb-to-RGB and RGB-to-YCrCb
- Standard identification (STDI) enables system level component format detection
- Certified Macrovision copy protection detection on component formats (525i, 625i, 525p and 625p)
- Free-run output mode provides stable timing when no video input is present

- Arbitrary pixel sampling support for non-standard video sources

RGB GRAPHICS PROCESSING

- 110 MSPS conversion rate supports RGB input resolutions up to 1280×1024 @ 60 Hz (SXGA)
- Automatic or manual clamp and gain controls for graphics modes
- Contrast and brightness controls
- Sampling PLL clock with 500 ps p-p jitter at 110 MSPS
- 32-phase DLL allows optimum pixel clock sampling
- Automatic detection of sync source and polarity by SSPD block
- Standard identification is enabled by STDI block
- RGB can be color space converted to YCrCb and decimated to a 4:2:2 format for video centric backend IC interfacing.
- Data enable (DE) output signal supplied for direct connection to HDMI/DVI Tx IC

- Arbitrary pixel sampling support for non-standard video sources

DIGITAL VIDEO INPUT PORT

- Supports raw 10-bit CVBS data from digital tuner
- Support for 24-bit RGB input data from DVI Rx chip, output converted to YCrCb 4:2:2
- Support for 24-bit 4:4:4, 20-/16-bit 4:2:2 525i, 625i, 525p, 625p, 1080i, 720p, VGA to SXGA @ 60 Hz input data from HDMI Rx chip, output converted to 16-bit 4:2:2 YCrCb.

GENERAL FEATURES

- HS, VS, and FIELD output signals with programmable position, polarity and width
- Supports two I^2C host port interface (control and VBI)
- Low power consumption: 1.8 V digital core, 3.3 V analog and digital I/O, low power power-down mode, and green PC mode
- 100-pin 14 mm × 14 mm lead Pb-free LQFP package

DETAILED DESCRIPTION

ANALOG FRONT END

The ADV7402 analog front end comprises three 12-bit 110 MHz Noise Shaped Video ADCs that digitize the analog video signal before applying it to the SDP or CP. The analog front end uses differential channels to each ADC to ensure high performance in a mixed-signal application. The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7402. Current and voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping either in the CP or SDP.

The ADCs are configured to run in 4× oversampling mode when decoding composite and S-video inputs; 2× oversampling is performed for component 525i, 625i, 525p, and 625p sources. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external anti-aliasing filters with the benefit of increased signal-to-noise ratio (SNR).

STANDARD DEFINITION PROCESSOR

The SDP section is capable of decoding a large selection of baseband video signals in composite and S-video formats. The video standards supported by the SDP include PAL B/D/I/G/H, PAL60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, SECAM B/D/G/K/L. The ADV7402 can automatically detect the video standard and process it accordingly.

The SDP has a 5 line super adaptive 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standard and signal quality with no user intervention required.

The SDP has specific luminance and chrominance parameter control for brightness, contrast, saturation, and hue.

The ADV7402 implements a patented adaptive-digital-line-length-tracking (ADLLT) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7402 to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, and camcorders. The SDP also contains a chroma transient improvement (CTI) processor. This processor increases the edge rate on chroma transitions, resulting in a sharper video image.

The SDP can process a variety of VBI data services such as closed captioning (CC), wide screen signaling (WSS), copy generation management system (CGMS), EDTV, Gemstar 1×/2× and extended data service (XDS). The ADV7402 SDP section has also a Macrovision 7.1 detection circuit that allows it to detect Types I, II, and III protection levels. The decoder is also fully robust to all Macrovision signal inputs.

COMPONENT PROCESSOR

The CP section is capable of decoding/digitizing a wide range of component video formats in any color space. Component video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, 1250i, VGA up to SXGA @ 60 Hz, and many other standards which are not listed here.

The CP section of the ADV7402 also contains an AGC block. In cases where no embedded sync is present, the video gain can be set manually. The AGC section is followed by a digital clamp circuit that ensures the video signal is clamped to the correct blanking level. Automatic adjustments within the CP include gain (contrast) and offset (brightness); manual adjustment controls are also supported.

A fully programmable any-to-any 3 × 3 color space conversion matrix is placed between the analog front end and the CP section. This enables YPrPb to RGB and RGB to YCrCb conversions. Many other standards of color space may be implemented using the color space converter.

The output section of the CP is highly flexible. It can be configured in single data rate mode (SDR) with one data packet per clock cycle. In SDR mode, a 16-/20-bit 4:2:2 or 24-/30-bit 4:4:4 output is possible. In these modes HS, VS, and FIELD/DE (where applicable) timing reference signals are provided.

The ADV7402 is capable of supporting an external DVI/HDMI receiver. The digital interface expects 24-bit 4:4:4 or 20-/16-bit 4:2:2 bit data (either graphics RGB or component video YCrCb), accompanied by HS, VS, DE and a fully synchronous clock signal. The data is processed in the CP and output as 16-bit 4:2:2 YCrCb data.

The CP section also contains circuitry to enable the detection of Macrovision encoded YPrPb signals for 525i, 625i, 525P and 625P. It is also designed to be fully robust when decoding these types of signals.

VBI extraction of CGMS data is also performed by the CP section of the ADV7402 for interlaced, progressive, and high definition scanning rates. The data extracted can be read back over the I^2C interface.

For more detailed product information about the ADV7402 contact your local ADI sales office, or email video.products@analog.com

TIMING DIAGRAMS

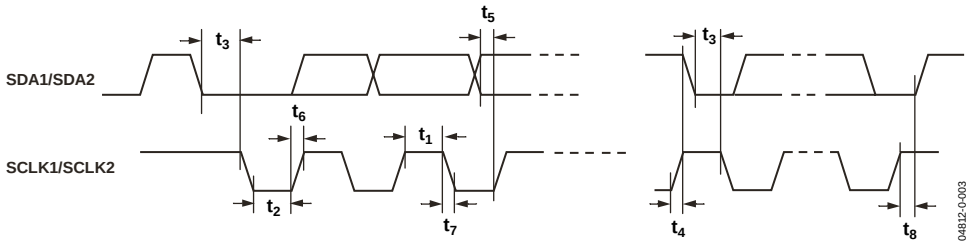

Figure 3. I²C Timing

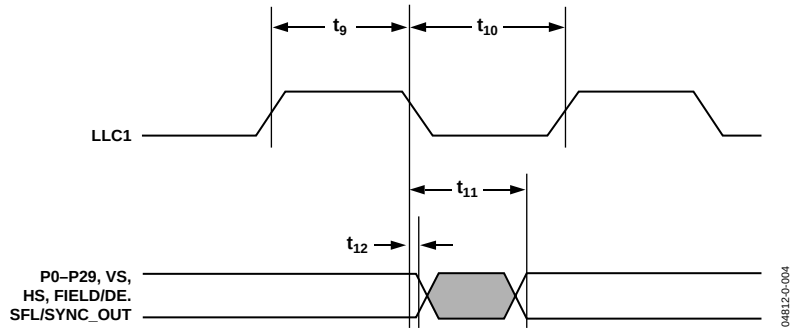

Figure 4. Pixel Port and Control Output Timing (SD Core)

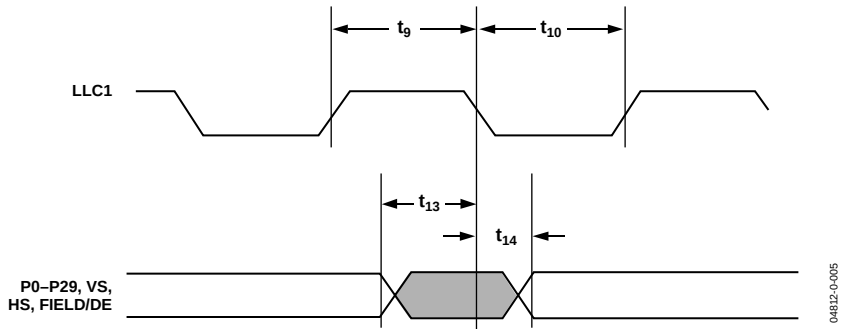

Figure 5. Pixel Port and Control Output Timing (CP Core)

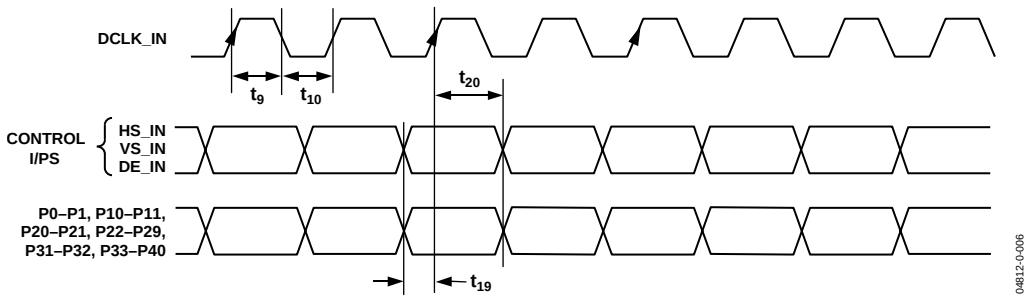

Figure 6. Digital Input Port and Control Input Timing

OUTLINE DIMENSIONS

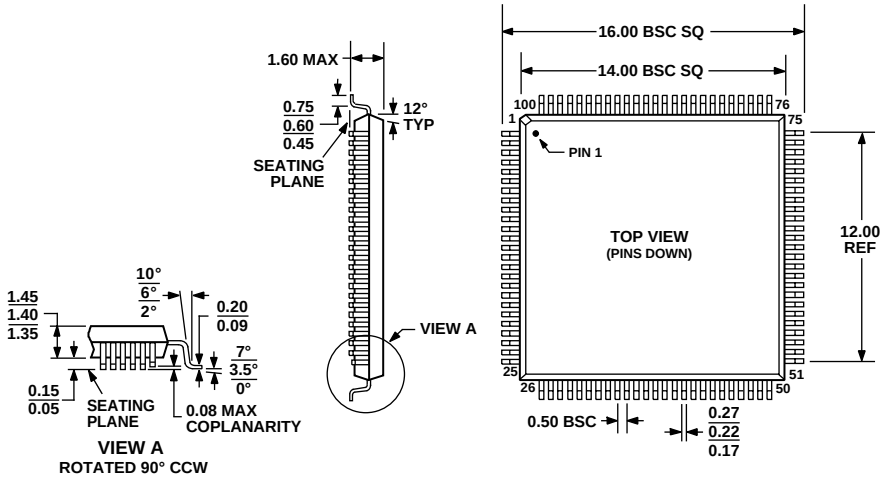

Figure 7. 100-Lead Low Profile Quad Flat Package (LQFP)
(ST-100)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7402KST-110	−25°C to +70°C	LQFP	ST-100
EVAL-ADV7402EBM		Evaluation Board	

Note: The ADV7402 is a Pb-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications, and is able to withstand surface-mount soldering at up to 255°C (±5°C). In addition, it is backward compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with SnPb solder pastes at conventional reflow temperatures of 220°C to 235°C.

NOTES

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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