LTC2286, LTC2287, LTC2288, LTC2290, LTC2291, LTC2292, LTC2293, LTC2294, LTC2295, LTC2296, LTC2297, LTC2298 or LTC2299

DESCRIPTION

Demonstration circuit 816 supports a family of 10/12/14 BIT 10 TO 65 MSPS DUAL ADCs. Each assembly features one of the following devices: LTC2286 thru LTC2298 high speed, high dynamic range ADCs.

Several versions of the 816A demo board supporting the LTC2286-2288 10 BIT, LTC2290-2293 12 BIT and LTC2295-2298 14 BIT series of A/D converters are listed in Table 1. Depending on the required resolution, sample rate and input frequency, the DC816 is supplied with the appropriate A/D and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies below 70 MHz or from 70 MHz to 140MHz for 12 and 14 bit versions. The 10 bit versions are configured with a wider 1MHz to 200MHz front end as the lower resolution 10 bit converters are not as sensitive to noise. For higher input frequencies, contact the factory for support.

Design files for this circuit board are available. Call the LTC factory.

Table 1. DC816A Variants

DC816 VARIANTS	ADC PART NUMBER	RESOLUTION*	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
816A-B	LTC2298	14-Bit	65Msps	1MHz - 70MHz
816A-C	LTC2297	14-Bit	40Msps	1MHz -70MHz
816A-D	LTC2296	14-Bit	25Msps	1MHz - 70MHz
816A-E	LTC2295	14-bit	10Msps	1MHz - 70MHz
816A-G	LTC2298	14-Bit	65Msps	70MHz -170MHz
816A-I	LTC2293	12-Bit	65Msps	1MHz - 70MHz
816A-J	LTC2292	12-Bit	40Msps	1MHz - 70MHz
816A-K	LTC2291	12-Bit	25Msps	1MHz - 70MHz
816A-L	LTC2290	12-Bit	10Msps	1MHz - 70MHz
816A-N	LTC2293	12-Bit	65Msps	70MHz -170MHz
816A-P	LTC2288	10-Bit	65Msps	1MHz - 70MHz
816A-Q	LTC2287	10-Bit	40Msps	1MHz - 70MHz
816A-R	LTC2286	10-Bit	25Msps	1MHz - 70MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Depending on sampling rate and the A/D converter provided, this supply must provide up to 150mA.	Optimized for 3.0V [2.7V ⇔3.6V min/max]
Analog input range	Depending on Sense Pin Voltage	$1V_{PP}$ to $2V_{PP}$
Logic Input Voltages	Minimum Logic High	2.4V
	Maximum Logic Low	0.8V
Logic Output Voltage (74VCX245 output buffer, V_{cc} = 2.5V)	Minimum Logic High @ -1.6mA	2.3V (33•••Series terminations)
	Maximum Logic Low @ 1.6mA	0.7V (33•••Series terminations)
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	50 • Source Impedance, AC coupled or ground referenced (Convert Clock input is capacitor coupled on board and terminated with 50•.)	$2V_{P-P}$ ⇔$2.5V_{P-P}$ Sine Wave or Square wave
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 816 is easy to set up to evaluate the performance of most members of the LTC229X family of Dual A/D converters – LTC2286, LTC2287, LTC2288, LTC2290, LTC2291, LTC2292, LTC2293, LTC2295, LTC2296, LTC2297, or LTC2298. The 80 Msps (LTC2299, LTC2294 and LTC2289) and follow-on higher sample rate versions will not be supported by the DC718, and have a different demo board and higher speed data collection board. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

If a DC718 QuickDATS Data Acquisition and Test System was supplied with the DC816 demonstration circuit, follow the DC718 Quick Start Guide to install the required software and for connecting the DC718 to the DC816 and to a PC running Windows98, 2000 or XP.

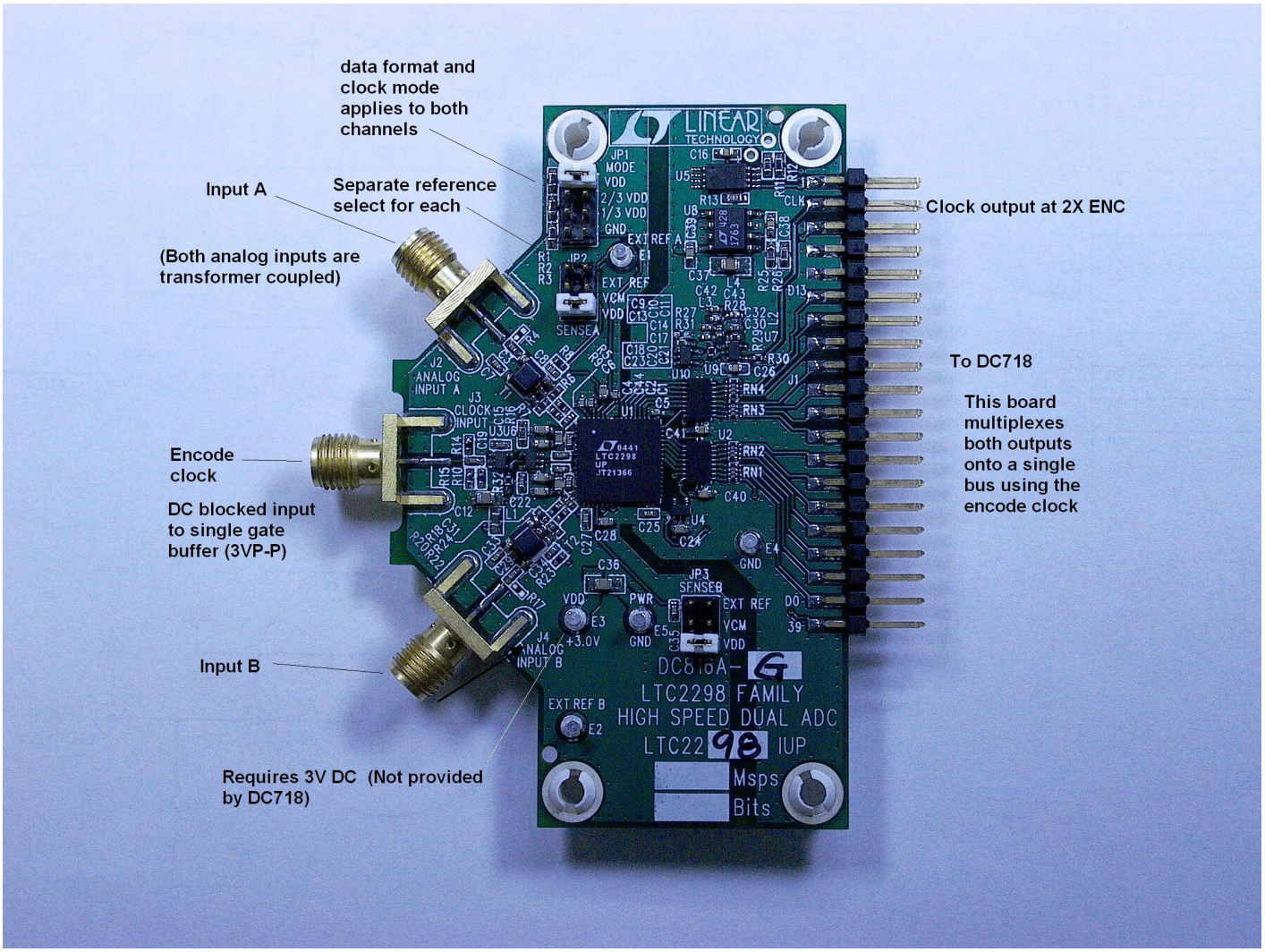

Figure 1. DC816 Setup

DC816 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC816 demonstration circuit board should have the following jumper settings as default: (as per figure 1)

JP1: Mode: Vdd. 2s complement, Clock duty stabilizer off (see data sheet for function of Mode pin.)

JP2: Sense A: Vdd, (2V P-P input range)

JP3: Sense B: Vdd, (2V P-P input range)

APPLYING POWER AND SIGNALS TO THE DC816 DEMONSTRATION CIRCUIT BOARD:

If a DC718 is used to acquire data from the DC816, the DC718 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE applying +3V across the pins marked "+3.0V" and "PWR GND" on the DC816. The DC816 demonstration circuit requires up to 200 mA depending on the sampling rate and the A/D converter supplied.

ENCODE CLOCK

NOTE: As shipped, this is not a logic compatible input. It is terminated with 50 Ohms. For higher conversion rates, the encode clock can be a sinusoidal signal. For lower conversion rates (<25 Msps), this input should be driven with a square wave signal source, as the dvdt at the output of the clock buffer (U3) is less than 2x that at the SMA connector, and is inadequate both in terms of phase noise, as well as ensuring repeatable output timing due to differences in threshold voltages between the ADC, and buffer U6.

Apply an encode clock to the SMA connector on the DC816 demonstration circuit board marked "J3 CLOCK INPUT". This input is connected to ground through a 50• resistor R14, and followed by a blocking capacitor. For the best noise performance, the CLOCK INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be as large as possible, up to $3V_{P-P}$ or 13 dBm. Using band pass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input.

[The Encode Clock can be driven with a 2.5V to 3.3V CMOS Logic Level square wave if R14 is replaced with an acceptable load for the drive capability of the logic. Note that logic devices are generally not able to drive cable. A barrel is recommended for logic drive. If a cable is used, the cable carrying the clock signal must be terminated to maintain the signal integrity of the Encode Clock Source and the signal source must be able to drive the 0 to 2.5V square wave signal into 50••load••

Apply the analog input signals of interest to the SMA connectors on the DC816 demonstration circuit board marked "ANALOG INPUT (A and B)". These inputs are capacitive coupled to Balun transformers ETC1-1-13, or directly coupled through Flux coupled transformers ETC1-1T.

A doubled conversion clock output is available on pin 3 of J2 and the data samples are available on Pins 11-37 for 14 BITS or (15-37 for 12 BITS) of J2 which can be collected via a logic analyzer, cabled to a development system through a SHORT 2 to 4 inch long 40 pin ribbon cable or collected by the DC718 QuickEval-II Data Acquisition Board using the *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC718 was provided, follow the DC718 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

Configure PScope for the appropriate variant of the DC816 demonstration circuit by selecting the correct A/D Converter as installed on the DC816. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, LTC2286, through LTC2298. When evaluating 12 or 10 BIT parts, select the appropriate LTC229X part in the Device List and PScope will automati-

cally blank the last two or four LSBs when using a DC816 supplied with a 14 BIT part.

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. The two channel mode in Pscope provides a page for each channel, and a page showing the frequency domain plots of both channels. An additional window called "X-channel" displays relative phase and amplitude of the two channels. This can be used to gauge cross-talk, or validate relative aperture. Additional information and help for *PScope* is available in the DC718 Quick Start Guide and in the online help available within the *PScope* program itself.

ANALOG INPUT NETWORK

For optimal distortion and noise performance the RC network on the analog inputs are optimized for different analog input frequencies on the different versions of the DC816. For input frequencies below about 70 MHz, the circuit in Fig. 2 is recommended (this is installed on DC816 versions A,B,C,D,E). For input frequencies above 70 MHz and below 170 MHz, the circuit in Fig. 3 is recommended (this is installed on versions F,G).

For input frequencies between 170 and 250MHz, connect the transformer outputs directly to the ADC inputs without the RC filter. For input frequencies between 250 MHz and 500 MHz, the circuit in Fig. 4 is recommended. For input frequencies greater than 250 MHz contact the factory for support.

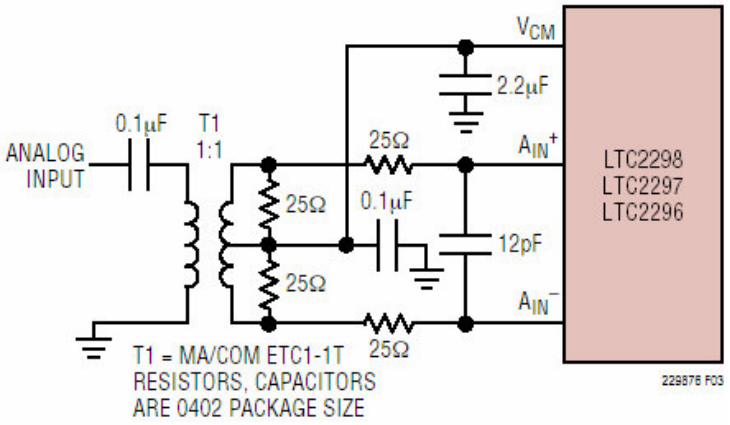

Figure 2. Analog Front End Circuit For 1MHz < A_{IN} < 70MHz (1 of 2)

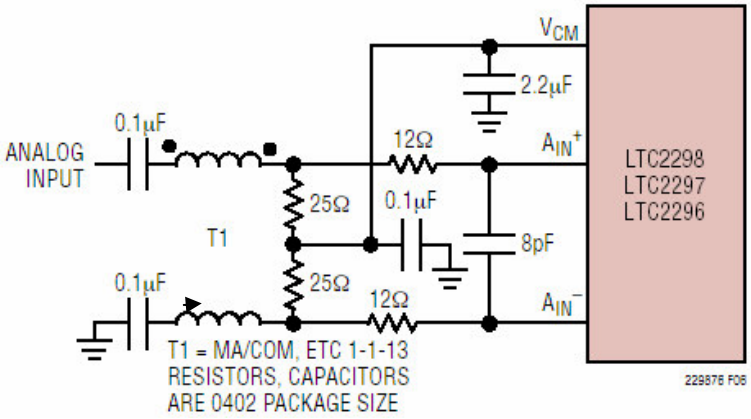

Figure 3. Analog Front End Circuit For 70MHz < A_{IN} < 170MHz (1 of 2)

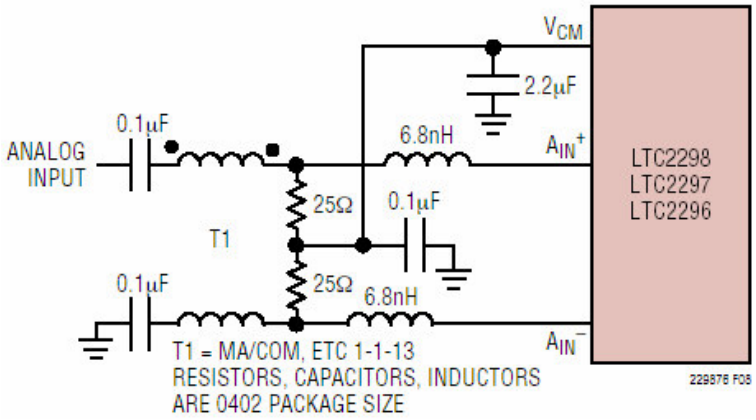

Figure 4. Analog Front End Circuit For 300MHz < A_{IN} < 500MHz

Note that relative aperture measurements require removal of these networks, or the results will simply show the relative phase through the RC network. The measure of relative phase further requires a resistive power divider, and matched cables, or the results will be misleading. Any relative phase measurements should be confirmed by reversing the signals to confirm that the relative delay is not due to the external network.

If relative phase measurements produce results of greater that a fractional psec, please consult the factory for assistance.

Channel to Crosstalk on this demo board better than -110 dB below 140 MHz.