CY7C1471BV33
CY7C1473BV33

72-Mbit (2M × 36/4M × 18) Flow-Through SRAM with NoBL™ Architecture

Features

- No bus latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133 MHz bus operations with zero wait states
- Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow through operation
- Byte write capability
- 3.3 V/2.5 V I/O supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (for 133 MHz device)
- Clock enable ($\overline{CEN}$) pin to enable clock and suspend operation
- Synchronous self-timed writes
- Asynchronous output enable ($\overline{OE}$)
- CY7C1471BV33 available in JEDEC-standard Pb-free 100-pin thin quad flat pack (TQFP), Pb-free and non-Pb-free 165-ball fine-pitch ball grid array (FBGA) package. CY7C1473BV33 available in JEDEC-standard Pb-free 100-pin thin quad flat pack (TQFP)
- Three chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) for simple depth expansion
- Automatic power-down feature available using ZZ mode or CE deselect
- IEEE 1149.1 JTAG boundary scan compatible
- Burst capability – linear or interleaved burst order
- Low standby power

Functional Description

The CY7C1471BV33 and CY7C1473BV33 are 3.3 V, 2M × 36/4M × 18 synchronous flow through burst SRAMs designed specifically to support unlimited true back-to-back read or write operations without the insertion of wait states. The CY7C1471BV33 and CY7C1473BV33 are equipped with the advanced No Bus Latency (NoBL) logic. NoBL™ is required to enable consecutive read or write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133 MHz device).

Write operations are controlled by two or four Byte Write Select (BW_X) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

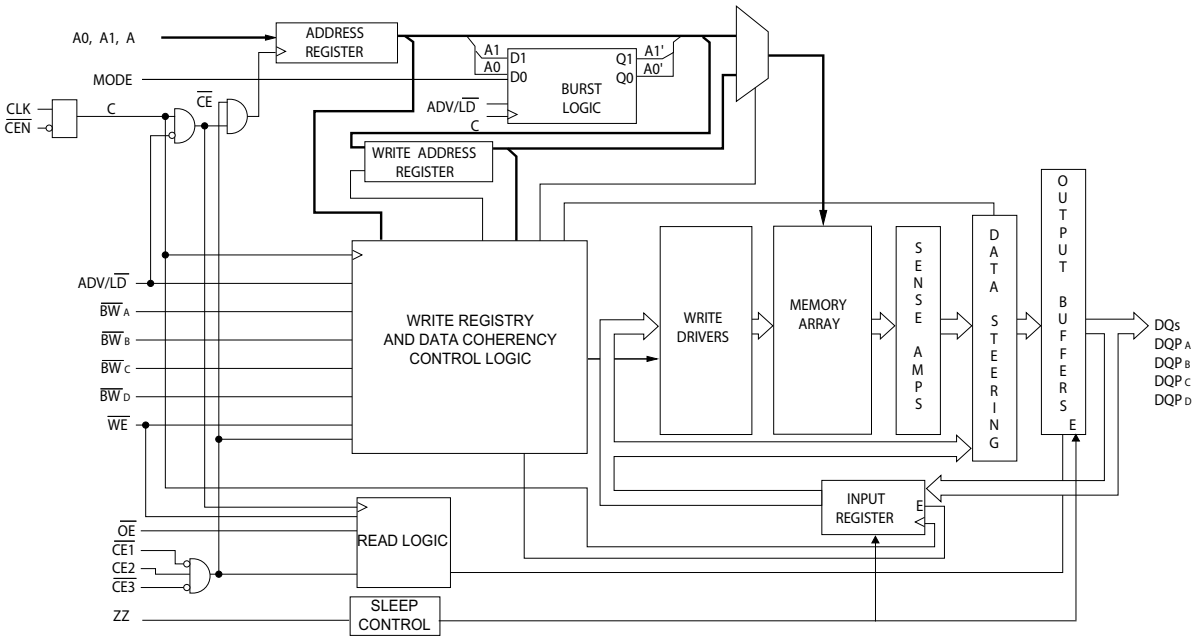
Three synchronous chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

For a complete list of related documentation, click here.

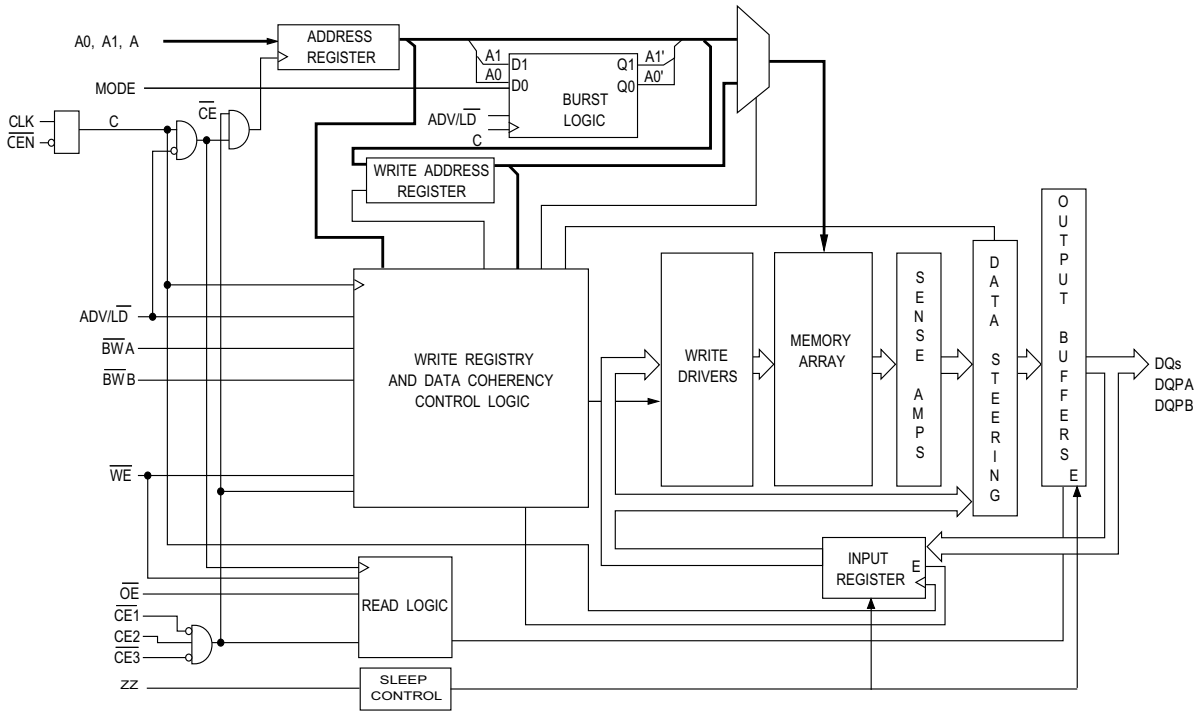
Selection Guide

Description	133 MHz	Unit
Maximum access time	6.5	ns
Maximum operating current	305	mA
Maximum CMOS standby current	120	mA

Logic Block Diagram – CY7C1471BV33



Logic Block Diagram – CY7C1473BV33



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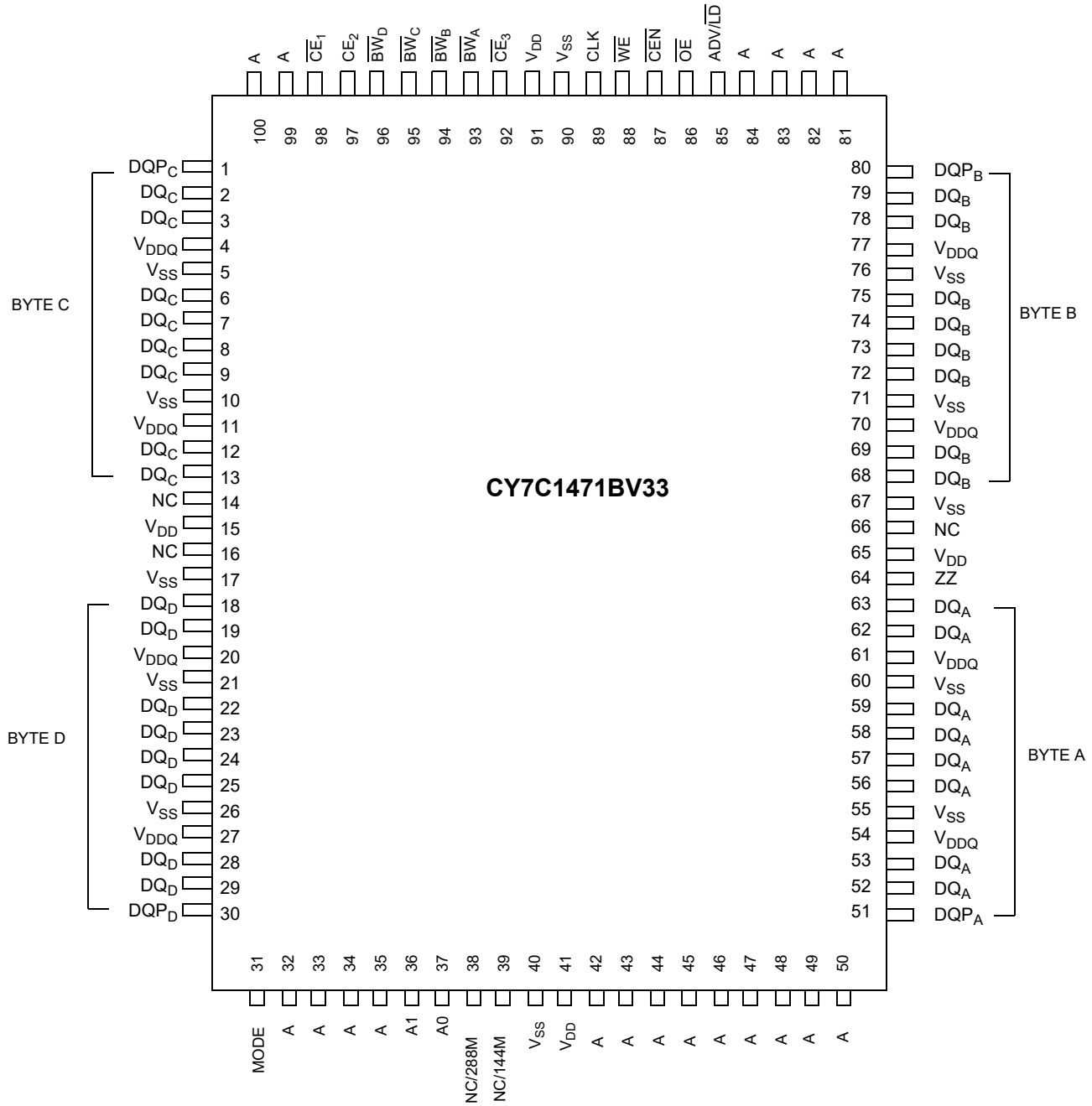
Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout

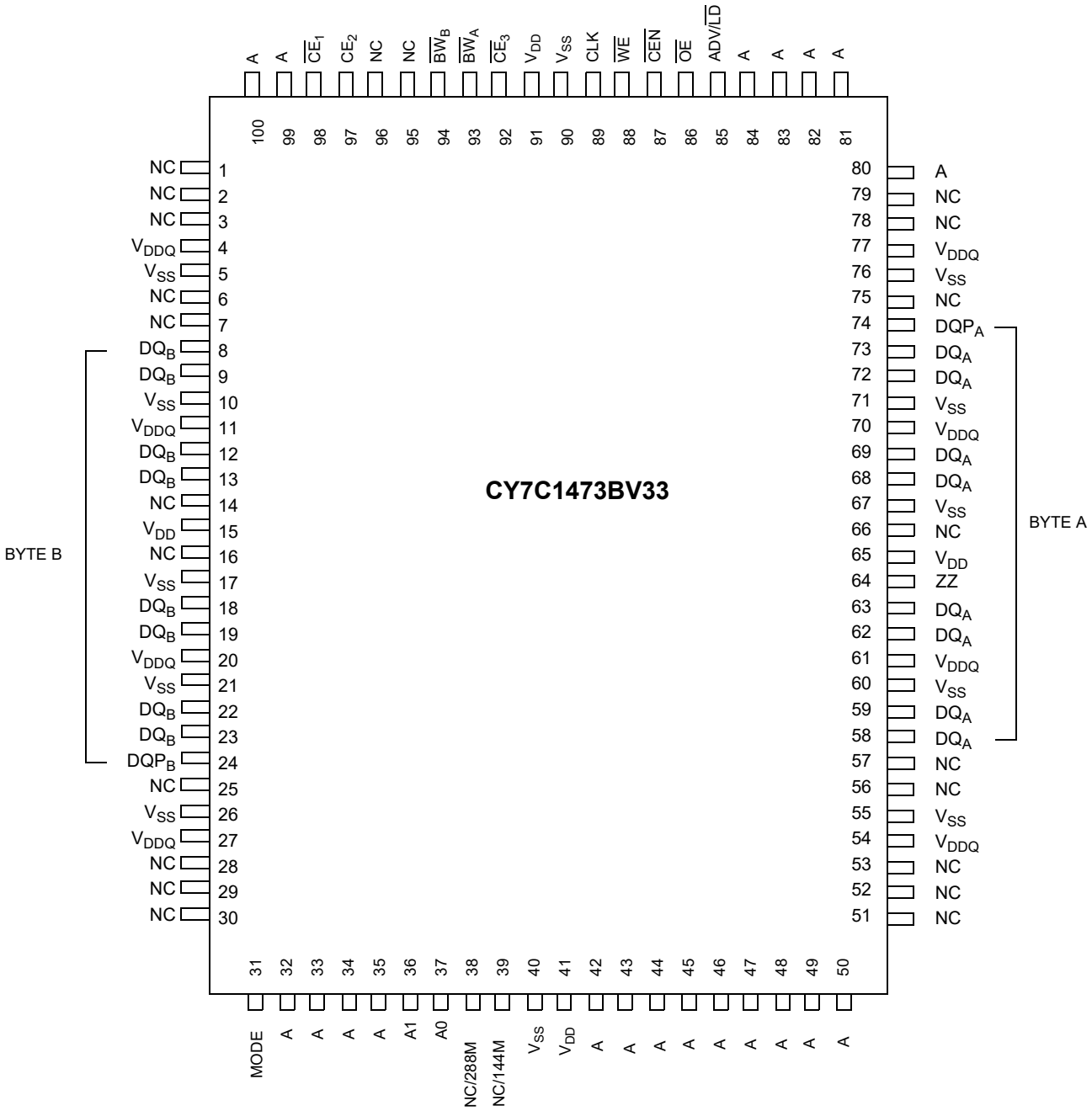
CY7C1471BV33 (2M × 36)



Pin Configurations (continued)

Figure 2. 100-pin TQFP (14 × 20 × 1.4 mm) pinout

CY7C1473BV33 (4M × 18)



Pin Configurations (continued)

Figure 3. 165-ball FBGA (15 × 17 × 1.4 mm) pinout

CY7C1471BV33 (2M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC/1G	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC/144M	A	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ is fed to the two-bit burst counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-Synchronous	**Byte write inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	**Write enable input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/load input**. Advances the on-chip address counter or loads a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After deselection, drive ADV/$\overline{LD}$ LOW to load a new address.
CLK	Input-Clock	**Clock input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device.
CE_2	Input-Synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output enable, asynchronous input, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are enabled to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected.
$\overline{CEN}$	Input-Synchronous	**Clock enable input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Because deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
ZZ	Input-Asynchronous	**ZZ "Sleep" input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull-down.
DQ_s	I/O-Synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and DQP_X are placed in a tri-state condition.The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional data parity I/O lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_X is controlled by BW_X correspondingly.
MODE	Input Strap Pin	**Mode input. Selects the burst order of the device.** When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the device**.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not used, this pin must be left unconnected. This pin is not available on TQFP packages.

Pin Definitions (continued)

Name	I/O	Description
TDI	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be left floating or connected to V_{DD} through a pull-up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input Synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not used, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.

Functional Overview

The CY7C1471BV33, and CY7C1473BV33 are synchronous flow through burst SRAMs designed specifically to eliminate wait states during write-read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

Accesses may be initiated by asserting all three chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). Byte Write Select ($\overline{BW_X}$) can be used to conduct Byte Write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$ must be driven LOW after the device is deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$ is asserted LOW
- $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active
- $\overline{WE}$ is deasserted HIGH
- ADV/$\overline{LD}$ is asserted LOW

The address presented to the address inputs is latched into the Address Register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133 MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW to drive out the requested data. On the subsequent clock, another operation (read/write/deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, output is tri-stated immediately.

Burst Read Accesses

The CY7C1471BV33, and CY7C1473BV33 have an on-chip burst counter that enables the user to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in the Single Read Access section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wrap around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enable inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (3) $\overline{WE}$ is asserted LOW. The address presented to the address bus is loaded into the Address Register. The Write signals are latched into the Control Logic block. The data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and DQP_X.

On the next clock rise the data presented to DQs and DQP_X (or a subset for Byte Write operations, see section Truth Table for Read/Write on page 11 for details), input is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by $\overline{BW_X}$ signals. The CY7C1471BV33, and CY7C1473BV33 provide Byte Write capability that is described in the section Truth Table for Read/Write on page 11. The input $\overline{WE}$ with the selected $\overline{BW_X}$ input selectively writes to only the desired bytes. Bytes not selected during a Byte Write operation remain unaltered. A synchronous self timed write mechanism is provided to simplify the write operations. Byte write capability is included to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1471BV33, and CY7C1473BV33 are common I/O devices, do not drive data into the device when the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQs and DQP_X inputs. Doing so tri-states the output drivers. As a safety precaution, DQs and DQP_X are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1471BV33, CY7C1473BV33 have an on-chip burst counter that enables the user to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load the initial address, as described in section Single Write Accesses on page 8. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. Drive the correct BW_X inputs in each cycle of the burst write to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid and the completion of the operation is not guaranteed. The device must be deselected before entering the “sleep” mode. $\overline{CE_1}$, CE_2, and $\overline{CE_3}$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2 V	–	120	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1471BV33, and CY7C1473BV33 follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-state
Deselect cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-state
Deselect cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-state
Continue deselect cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-state
Read cycle (begin burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data out (Q)
Read cycle (continue burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data out (Q)
NOP/Dummy read (begin burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-state
Dummy read (continue burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-state
Write cycle (begin burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data in (D)
Write cycle (continue burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data in (D)
NOP/Write abort (begin burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-state
Write abort (continue burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-state
Ignore clock edge (stall)	Current	X	X	X	L	X	X	X	X	H	L->H	–
Sleep mode	None	X	X	X	H	X	X	X	X	X	X	Tri-state

Notes
1. X = “Don't Care.” H = Logic HIGH, L = Logic LOW. $\overline{BW_X}$ = L signifies at least one Byte Write Select is active, $\overline{BW_X}$ = Valid signifies that the desired Byte Write Selects are asserted, see section Truth Table for Read/Write on page 11 for details.
2. Write is defined by $\overline{BW_X}$, and $\overline{WE}$. See section Truth Table for Read/Write on page 11.
3. When a Write cycle is detected, all I/Os are tri-stated, even during Byte Writes.
4. The DQs and DQP_X pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. $\overline{CEN}$ = H, inserts wait states.
6. Device powers up deselected with the I/Os in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs and DQP_X = data when $\overline{OE}$ is active.

Truth Table for Read/Write

The read/write truth table for CY7C1471BV33 follows. [8, 9, 10]

Function (CY7C1471BV33)	$\overline{WE}$	$\overline{BW_a}$	$\overline{BW_b}$	$\overline{BW_c}$	$\overline{BW_d}$
Read	H	X	X	X	X
Write – No bytes written	L	H	H	H	H
Write byte A – (DQ_A and DQP_A)	L	L	H	H	H
Write byte B – (DQ_B and DQP_B)	L	H	L	H	H
Write byte C – (DQ_C and DQP_C)	L	H	H	L	H
Write byte D – (DQ_D and DQP_D)	L	H	H	H	L
Write all bytes	L	L	L	L	L

Truth Table for Read/Write

The read/write truth table for CY7C1473BV33 follows. [8, 9, 10]

Function (CY7C1473BV33)	$\overline{WE}$	$\overline{BW_a}$	$\overline{BW_b}$
Read	H	X	X
Write – No bytes written	L	H	H
Write byte a – (DQ_a and DQP_a)	L	L	H
Write byte b – (DQ_b and DQP_b)	L	H	L
Write both bytes	L	L	L

Notes
8. X = "Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{BW}_X$ = L signifies at least one Byte Write Select is active, $\overline{BW}_X$ = Valid signifies that the desired Byte Write Selects are asserted, see section Truth Table for Read/Write on page 11 for details.
9. Write is defined by $\overline{BW}_X$, and $\overline{WE}$. See section Truth Table for Read/Write on page 11.
10. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write is based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1471BV33 incorporate a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1471BV33 contain a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO must be left unconnected. During power-up, the device comes up in a reset state, which does not interfere with the operation of the device.

The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input gives commands to the TAP controller and is sampled on the rising edge of TCK. This ball may be left unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball serially inputs information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram on page 14. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

Test Data-Out (TDO)

The TDO output ball serially clocks data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

During power-up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register is selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 15. During power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary ‘01’ pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows the shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the section Identification Register Definitions on page 18.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Identification Codes on page 18. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail in this section.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which must be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register during power-up or whenever the TAP controller is in a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal when in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that because the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state when performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR command.

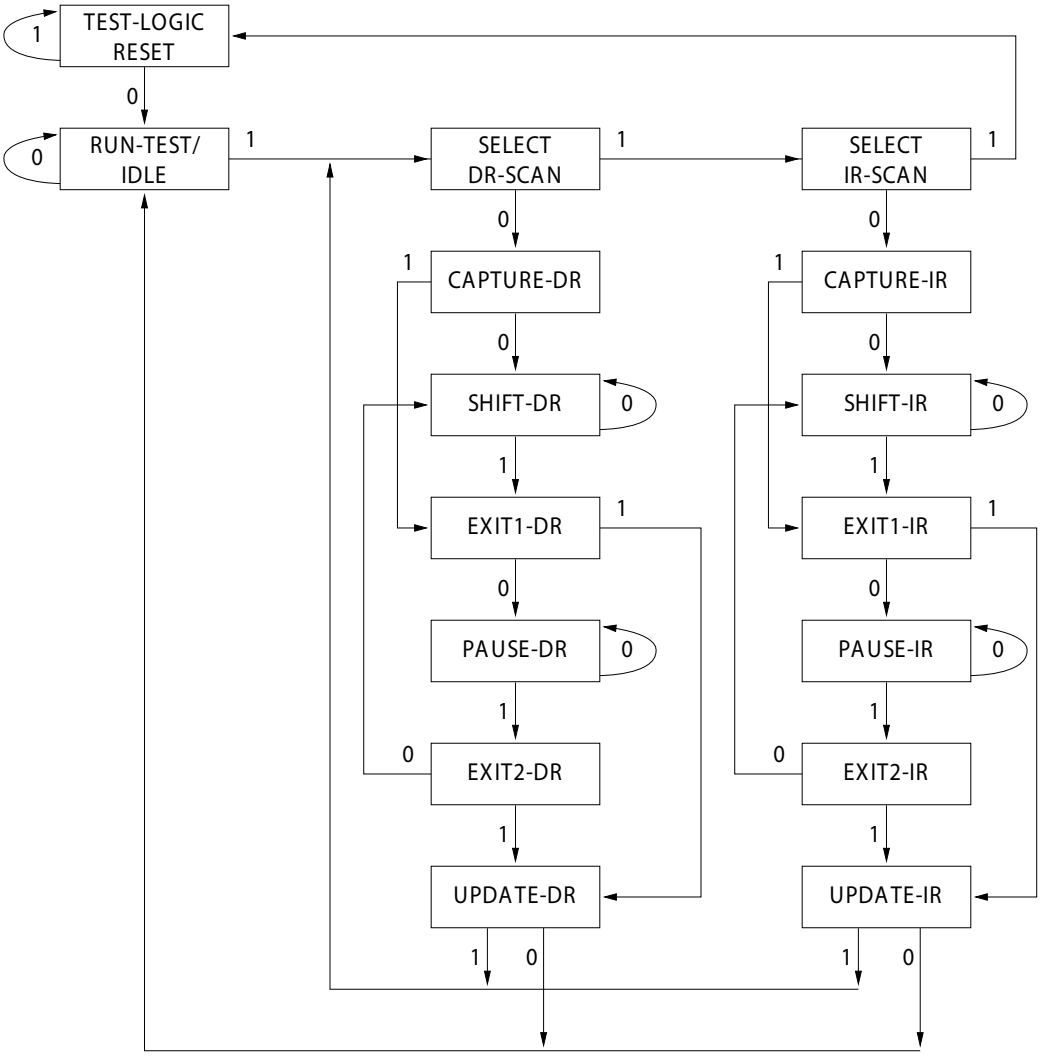
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

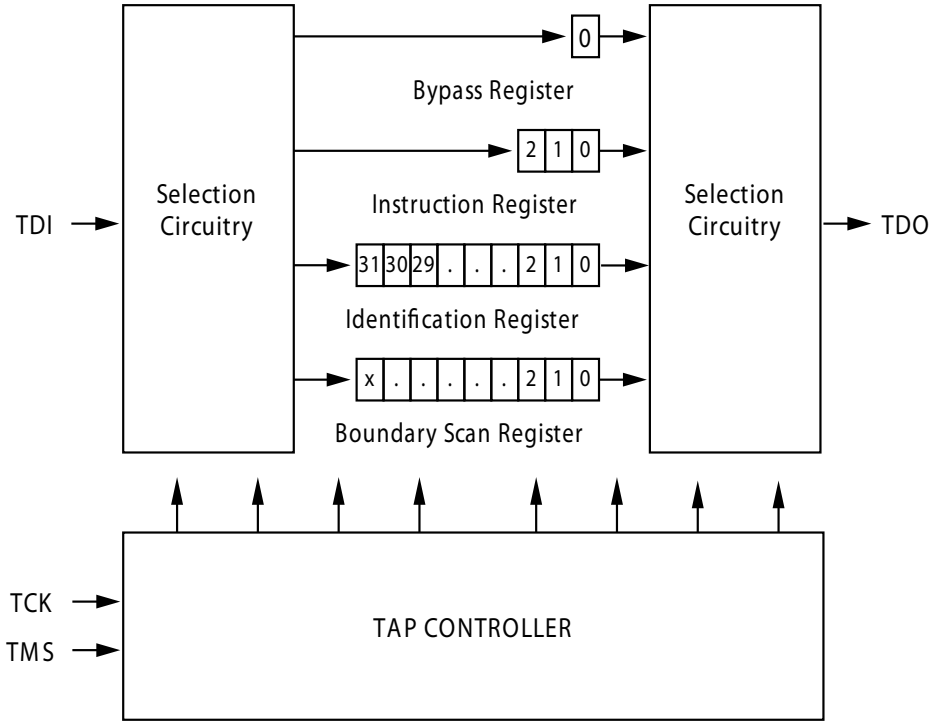
Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



TAP Controller Block Diagram



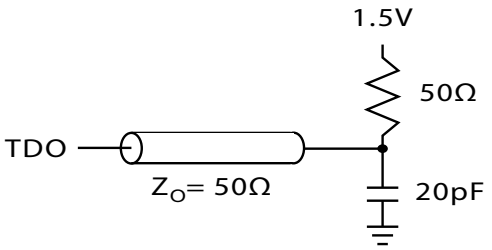
3.3 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 3.3 V
Input rise and fall times ..... 1 ns
Input timing reference levels ..... 1.5 V
Output reference levels ..... 1.5 V
Test load termination supply voltage ..... 1.5 V

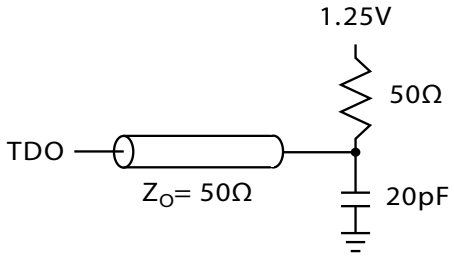
2.5 V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 2.5 V
Input rise and fall time ..... 1 ns
Input timing reference levels ..... 1.25 V
Output reference levels ..... 1.25 V
Test load termination supply voltage ..... 1.25 V

3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.3 V ± 0.165 V unless otherwise noted)

Parameter [11]	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3 V		2.4	–	V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5 V		2.0	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3 V	–	0.4	V
		I_{OL} = 1.0 mA	V_{DDQ} = 2.5 V	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH voltage		V_{DDQ} = 3.3 V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		V_{DDQ} = 3.3 V	–0.3	0.8	V
			V_{DDQ} = 2.5 V	–0.3	0.7	V
I_X	Input load current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note
11. All voltages refer to V_{SS} (GND).

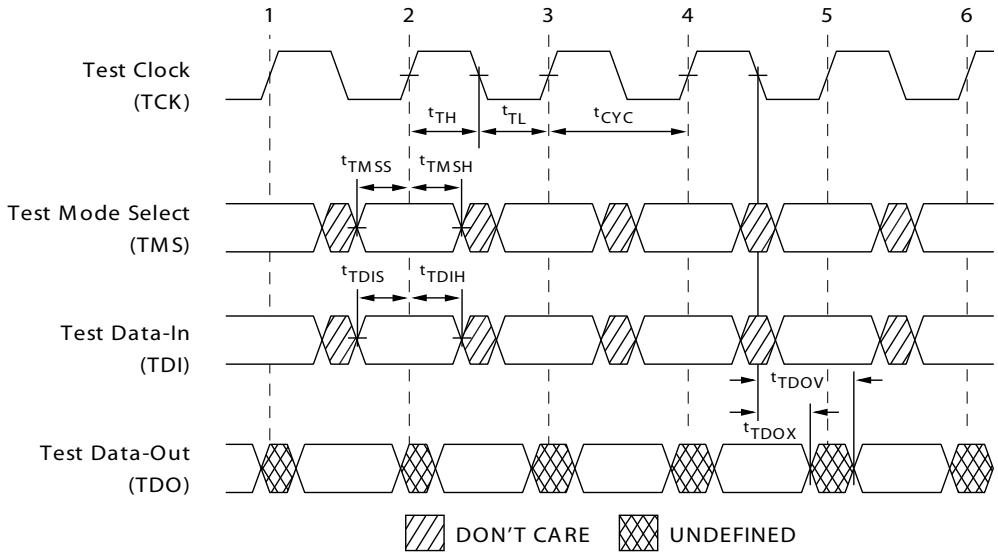
TAP AC Switching Characteristics

Over the Operating Range

Parameter [12, 13]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH time	20	–	ns
t_{TL}	TCK clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	5	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns

TAP Timing

Figure 4. TAP Timing



Notes
12. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
13. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

Identification Register Definitions

Instruction Field	CY7C1471BV33 (2M × 36)	Description
Revision number (31:29)	000	Describes the version number
Device depth (28:24) [14]	01011	Reserved for internal use
Architecture/memory type (23:18)	001001	Defines memory type and architecture
Bus width/density (17:12)	100100	Defines width and density
Cypress JEDEC ID code (11:1)	00000110100	Enables unique identification of SRAM vendor
ID register presence indicator (0)	1	Indicates the presence of an ID register

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction	3
Bypass	1
ID	32
Boundary scan order – 165-ball FBGA	71

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do not use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
RESERVED	101	Do not use: This instruction is reserved for future use.
RESERVED	110	Do not use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note
14. Bit #24 is “1” in the ID Register Definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Exit Order

(2M × 36)

Bit #	165-ball ID
1	C1
2	D1
3	E1
4	D2
5	E2
6	F1
7	G1
8	F2
9	G2
10	J1
11	K1
12	L1
13	J2
14	M1
15	N1
16	K2
17	L2
18	M2
19	R1
20	R2

Bit #	165-ball ID
21	R3
22	P2
23	R4
24	P6
25	R6
26	R8
27	P3
28	P4
29	P8
30	P9
31	P10
32	R9
33	R10
34	R11
35	N11
36	M11
37	L11
38	M10
39	L10
40	K11

Bit #	165-ball ID
41	J11
42	K10
43	J10
44	H11
45	G11
46	F11
47	E11
48	D10
49	D11
50	C11
51	G10
52	F10
53	E10
54	A9
55	B9
56	A10
57	B10
58	A8
59	B8
60	A7

Bit #	165-ball ID
61	B7
62	B6
63	A6
64	B5
65	A5
66	A4
67	B4
68	B3
69	A3
70	A2
71	B2

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND .....–0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND ..... –0.5 V to +V_{DD}

DC voltage applied to outputs in tri-state .....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage .....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range

Parameter [15, 16]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage	For 3.3 V I/O		3.135	V_{DD}	V
		For 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH voltage	For 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		For 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW voltage	For 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		For 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage [15]	For 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		For 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage [15]	For 3.3 V I/O		–0.3	0.8	V
		For 2.5 V I/O		–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}			30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DD}, output disabled		–5	5	µA
I_{DD} [17]	V_{DD} operating supply current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5 ns cycle, 133 MHz	–	305	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	200	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DD} – 0.3 V, f = 0, inputs static	7.5 ns cycle, 133 MHz	–	120	mA
I_{SB3}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	200	mA

Notes

15. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than $t_{CYC}/2$).
16. $T_{Power-up}$: assumes a linear ramp from 0 V to $V_{DD(min.)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.
17. The operation current is calculated with 50% read cycle and 50% write cycle.

Electrical Characteristics (continued)

Over the Operating Range

Parameter [15, 16]	Description	Test Conditions		Min	Max	Unit
I_{SB4}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = 0, inputs static	7.5 ns cycle, 133 MHz	–	165	mA

Capacitance

Parameter [18]	Description	Test Conditions	100-pin TQFP Package	165-ball FBGA Package	Unit
$C_{ADDRESS}$	Address input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	6	6	pF
C_{DATA}	Data input capacitance		5	5	pF
C_{CTRL}	Control input capacitance		8	8	pF
C_{CLK}	Clock input capacitance		6	6	pF
$C_{I/O}$	I/O capacitance		5	5	pF

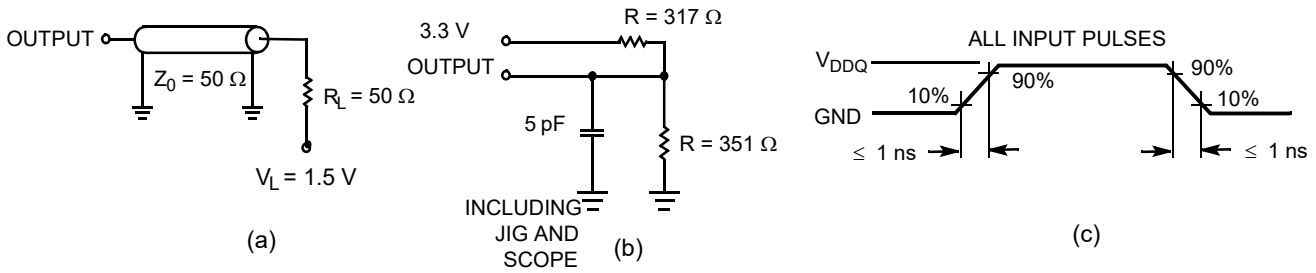
Thermal Resistance

Parameter [18]	Description	Test Conditions	100-pin TQFP Max	165-ball FBGA Max	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	24.63	16.3	°C/W
θ_{JC}	Thermal resistance (junction to case)		2.28	2.1	°C/W

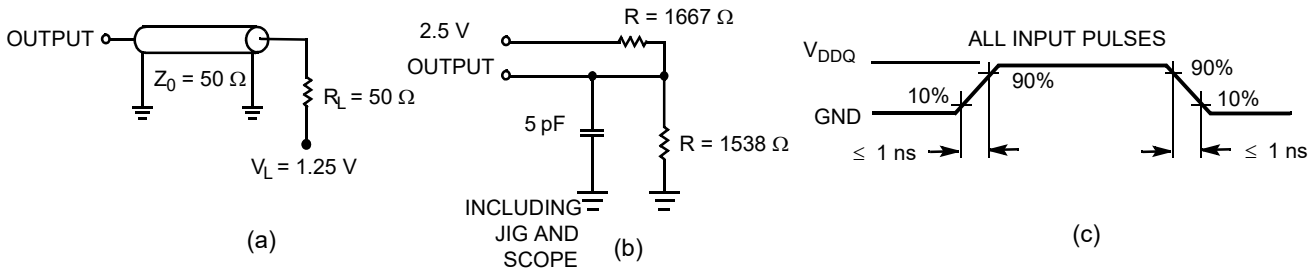
AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms

3.3 V I/O Test Load



2.5 V I/O Test Load



Note
18. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

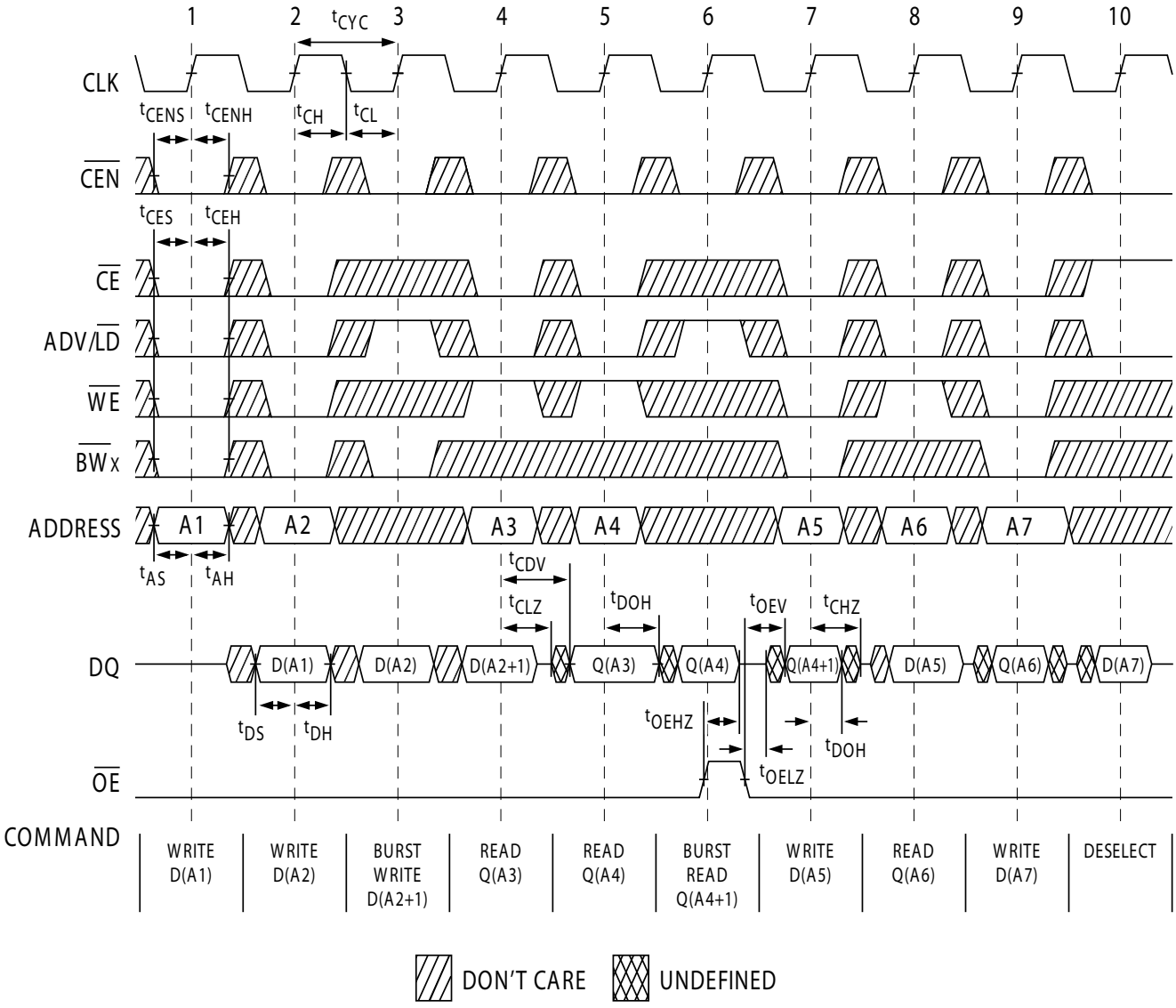
Parameter [19]	Description	133 MHz		Unit
		Min	Max	
t_{POWER} [20]		1	–	ms
Clock				
t_{CYC}	Clock cycle time	7.5	–	ns
t_{CH}	Clock HIGH	2.5	–	ns
t_{CL}	Clock LOW	2.5	–	ns
Output Times				
t_{CDV}	Data output valid after CLK rise	–	6.5	ns
t_{DOH}	Data output hold after CLK rise	2.5	–	ns
t_{CLZ}	Clock to low Z [21, 22, 23]	3.0	–	ns
t_{CHZ}	Clock to high Z [21, 22, 23]	–	3.8	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.0	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [21, 22, 23]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [21, 22, 23]	–	3.0	ns
Setup Times				
t_{AS}	Address setup before CLK rise	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ setup before CLK rise	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ setup before CLK rise	1.5	–	ns
t_{CENS}	$\overline{CEN}$ setup before CLK rise	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	ns
t_{CES}	Chip enable setup before CLK rise	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ hold after CLK rise	0.5	–	ns
t_{CENH}	$\overline{CEN}$ hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	ns

Notes

19. Unless otherwise noted in the following table, timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V. Test conditions shown in part (a) of Figure 5 on page 21 unless otherwise noted.
20. This part has an internal voltage regulator; t_{POWER} is the time that the power must be supplied above $V_{DD(minimum)}$ initially, before a read or write operation is initiated.
21. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 5 on page 21. Transition is measured ±200 mV from steady-state voltage.
22. At any supplied voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z before Low Z under the same system conditions.
23. This parameter is sampled and not 100% tested.

Switching Waveforms

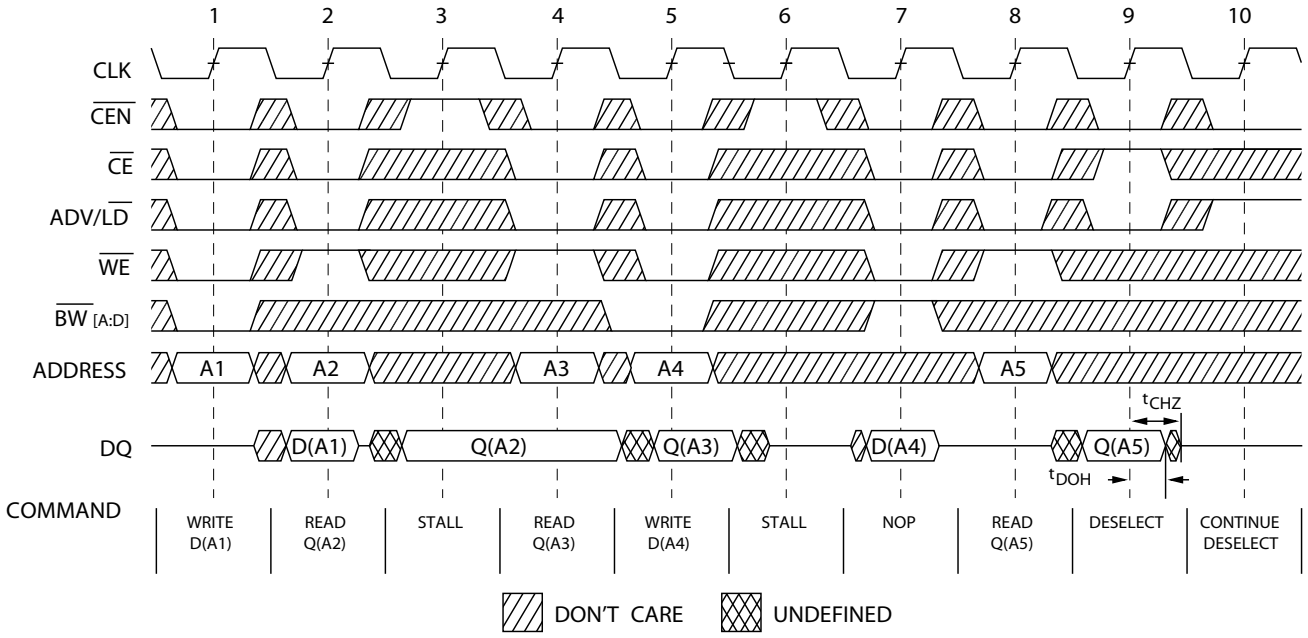
Figure 5. Read/Write Timing [24, 25, 26]



Notes
24. For this waveform ZZ is tied LOW.
25. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH, CE_2 is LOW or $\overline{CE_3}$ is HIGH.
26. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

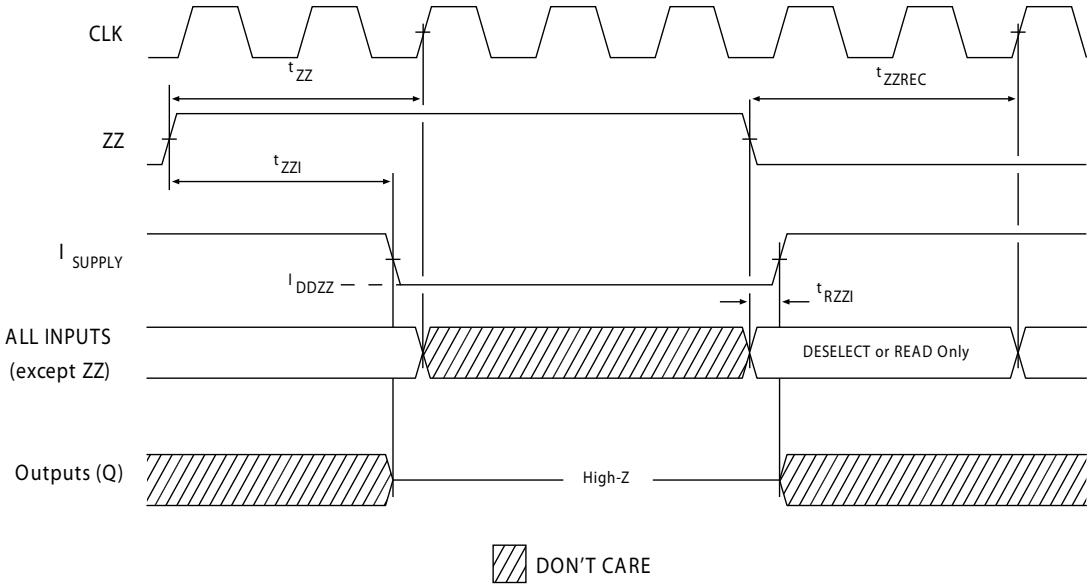
Figure 6. NOP, STALL, and DESELECT Cycles [27, 28, 29]



Notes
27. For this waveform ZZ is tied LOW.
28. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW or $\overline{CE}_3$ is HIGH.
29. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

Figure 7. ZZ Mode Timing [30, 31]



Notes
30. Device must be deselected when entering ZZ mode. See the Truth Table on page 10 for all possible signal conditions to deselect the device.
31. DQs are in high Z when exiting ZZ sleep mode.

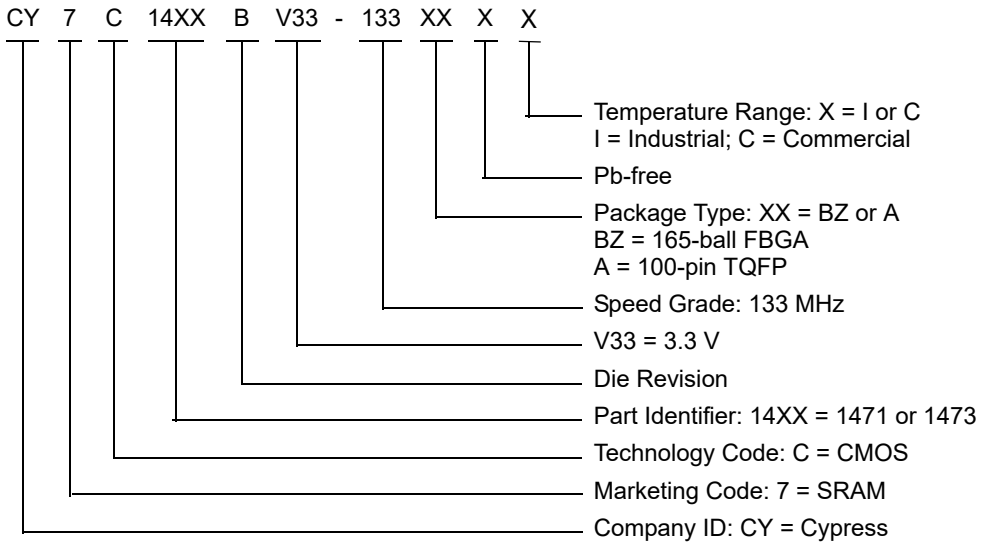
Ordering Information

Table 1 lists the CY7C1471BV33, CY7C1473BV33 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. CY7C1471BV33, CY7C1473BV33 Key Features and Ordering Information

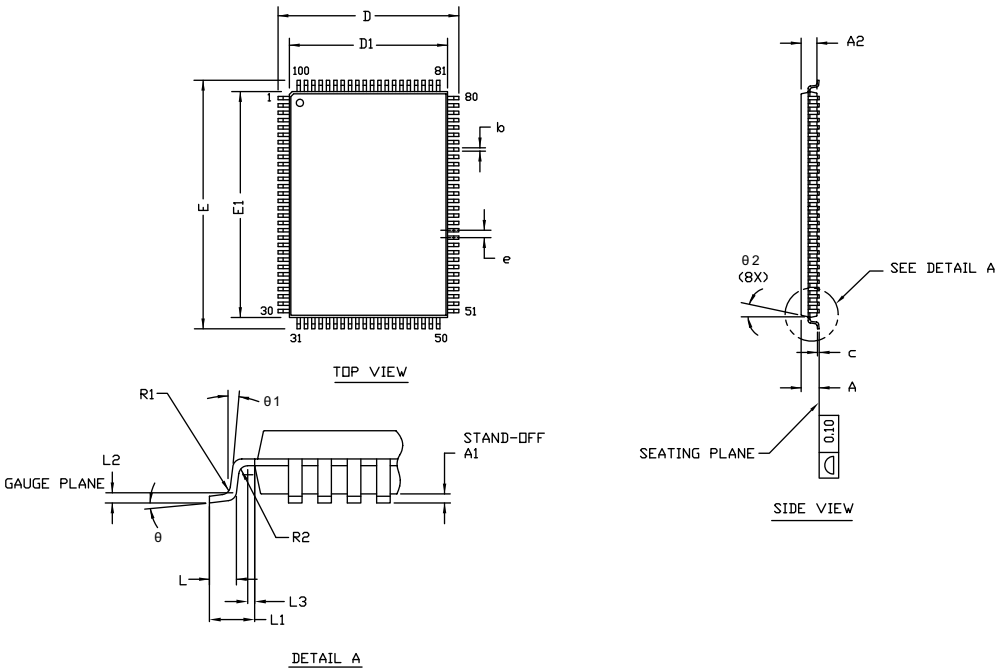
Speed (MHz)	Ordering Code	Package Diagram	Package	Operating Ranges
133	CY7C1471BV33-133BZI	51-85165	165-ball FBGA (15 × 17 × 1.4 mm)	Industrial
	CY7C1471BV33-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1473BV33-133AXC			

Ordering Code Definitions



Package Diagrams

Figure 8. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



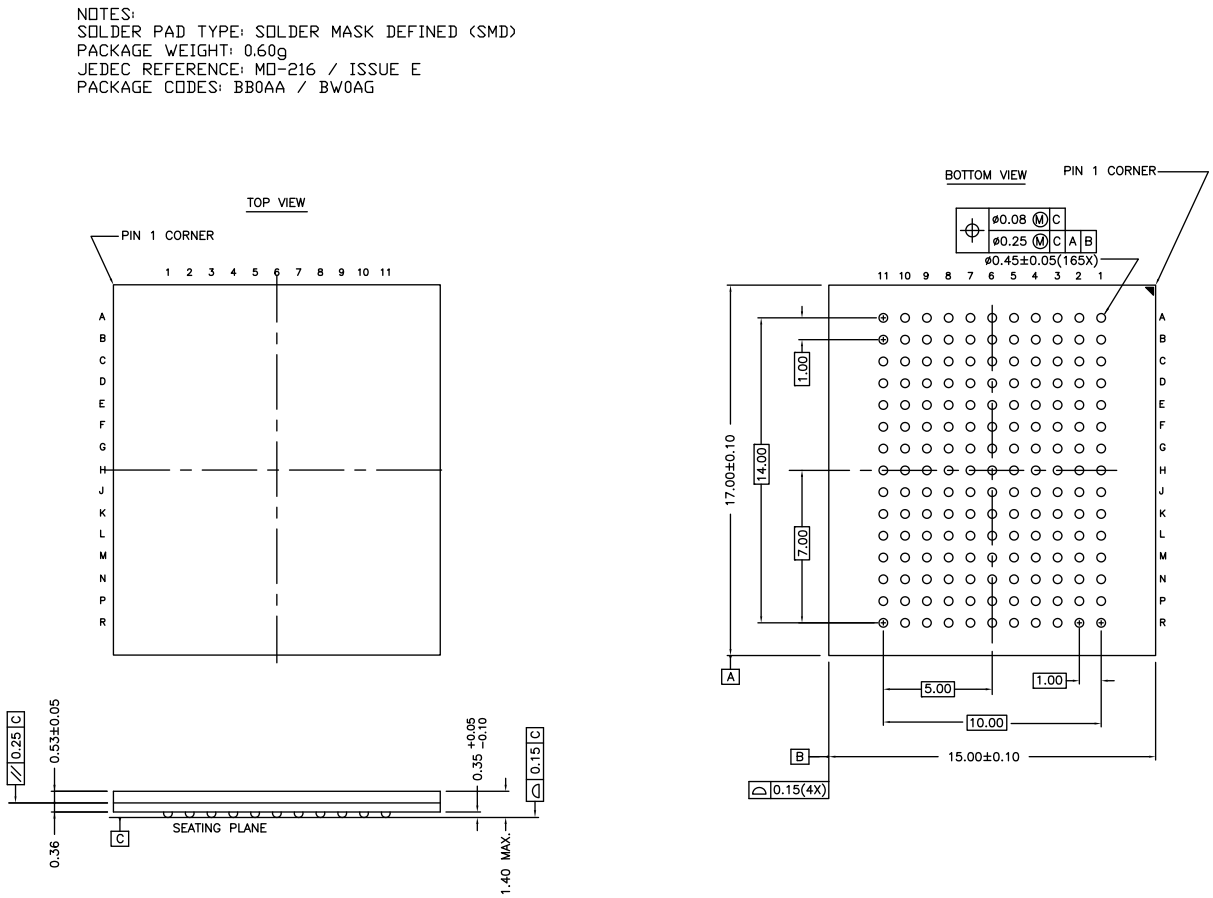
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.22	0.30	0.38
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.65 TYP		

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 *G

Package Diagrams (continued)

Figure 9. 165-ball FBGA (15 × 17 × 1.40 mm) (0.45 Ball Diameter) Package Outline, 51-85165



51-85165 *E

Acronyms

Acronym	Description
$\overline{CEN}$	Clock Enable
CMOS	Complementary Metal-Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JTAG	Joint Test Action Group
LSB	Least Significant Bit
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data-In
TDO	Test Data-Out
TMS	Test Mode Select
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1471BV33/CY7C1473BV33, 72-Mbit (2M × 36/4M × 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 001-15029				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1024500	VKN / KKVTMP	05/01/2007	New data sheet.
*A	1274731	VKN / AESA	07/18/2007	Updated Switching Waveforms (Updated Figure 6 (Corrected typo)).
*B	2183566	VKN / PYRS	03/06/2008	Changed status from Preliminary to Final. Updated Electrical Characteristics (Added Note 17 and referred the same note in I_{DD} parameter).
*C	2898663	NJY	03/24/2010	Updated Ordering Information (Updated part numbers). Updated Package Diagrams: spec 51-85050 – Changed revision from *B to *C. spec 51-85165 – Changed revision from *A to *B. spec 51-85167 – Changed revision from ** to *A.
*D	2905600	VKN	04/06/2010	Updated Ordering Information (Updated part numbers).
*E	3298193	OSN	06/30/2011	Updated Package Diagrams: spec 51-85050 – Changed revision from *C to *D. spec 51-85165 – Changed revision from *B to *C. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*F	3436299	PRIT	11/15/2011	Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85165 – Changed revision from *C to *D. spec 51-85167 – Changed revision from *A to *B. Updated to new template.
*G	3628180	PRIT	05/25/2012	Updated Features (Removed CY7C1475BV33 related information, removed 209-ball FBGA package related information, removed 165-ball FBGA package related information (Corresponding to CY7C1473BV33)). Updated Functional Description (Removed CY7C1475BV33 related information). Updated Selection Guide (Removed 117 MHz frequency related information). Removed Logic Block Diagram – CY7C1475BV33. Updated Pin Configurations (Updated Figure 3 (Removed CY7C1475BV33 related information), removed 209-ball FBGA package related information). Updated Pin Definitions. Updated Functional Overview (Removed CY7C1475BV33 related information). Updated Truth Table (Removed CY7C1475BV33 related information). Updated Truth Table for Read/Write (Removed CY7C1475BV33 related information). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed CY7C1473BV33, CY7C1475BV33 related information). Updated Identification Register Definitions (Removed CY7C1473BV33, CY7C1475BV33 related information). Updated Scan Register Sizes (Removed Bit Size (× 18), and Bit Size (× 72) columns). Removed Boundary Scan Exit Order (Corresponding to CY7C1473BV33).

Document History Page (continued)

Document Title: CY7C1471BV33/CY7C1473BV33, 72-Mbit (2M × 36/4M × 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 001-15029				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*G (cont.)	3628180	PRIT	05/25/2012	Updated Electrical Characteristics (Removed 117 MHz frequency related information). Updated Capacitance (Removed 209-ball FBGA package related information). Updated Thermal Resistance (Removed 209-ball FBGA package related information). Updated Switching Characteristics (Removed 117 MHz frequency related information). Updated Package Diagrams (Removed 209-ball FBGA package related information (spec 51-85167 Rev. *B)). Completing Sunset Review.
*H	4489161	PRIT	08/31/2014	Updated Ordering Information (Updated part numbers). Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E. Updated to new template.
*I	4569232	PRIT	11/14/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*J	4812510	PRIT	06/26/2015	Updated Package Diagrams: spec 51-85165 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*K	6029208	CNX	01/12/2018	Updated Package Diagrams: spec 51-85050 – Changed revision from *E to *G. Updated to new template.

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