CY62146EV30 MoBL®

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62146DV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in a Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin TSOP II Packages

Functional Description

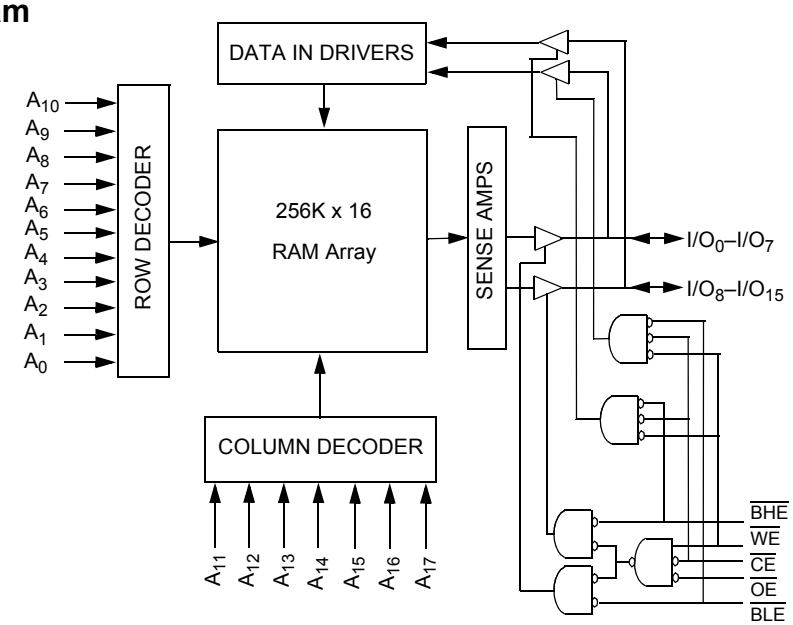
The CY62146EV30 is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features an advanced circuit design designed to provide an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 80 percent when addresses are not toggling.The device can also be put into standby mode reducing power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is in progress ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout [1, 2]

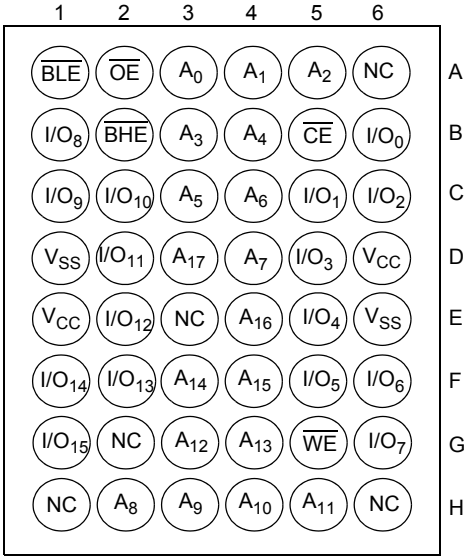
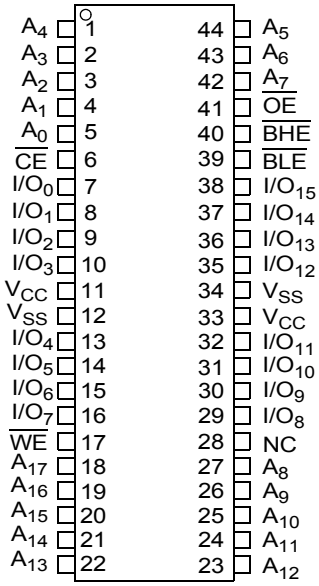


Figure 2. 44-pin TSOP II pinout [1]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [3]	Max		Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62146EV30LL	Industrial / Automotive-A	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Notes
1. NC pins are not connected on the die.
2. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8Mb, 16Mb and 32Mb respectively.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential .....–0.3 V to + 3.9 V (V_{CCmax} + 0.3 V)

DC voltage applied to outputs in High-Z state [4, 5] .....–0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

DC input voltage [4, 5] ..... –0.3 V to 3.9 V ($V_{CC\ max}$ + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up Current .....>200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [6]
CY62146EV30	Industrial / Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Ind'l/Auto-A)			Unit
				Min	Typ [7]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	V
V_{IH}	Input high voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ $V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ $V_O \leq V_{CC}$, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	15	20	mA
		f = 1 MHz		–	2	2.5	
I_{SB1}	Automatic CE power down current – CMOS inputs	$\overline{CE}$ > V_{CC} – 0.2 V, V_{IN} > V_{CC} – 0.2 V or V_{IN} < 0.2 V, f = f_{max} (Address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	1	7	µA
I_{SB2} [8]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	1	7	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{cc} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

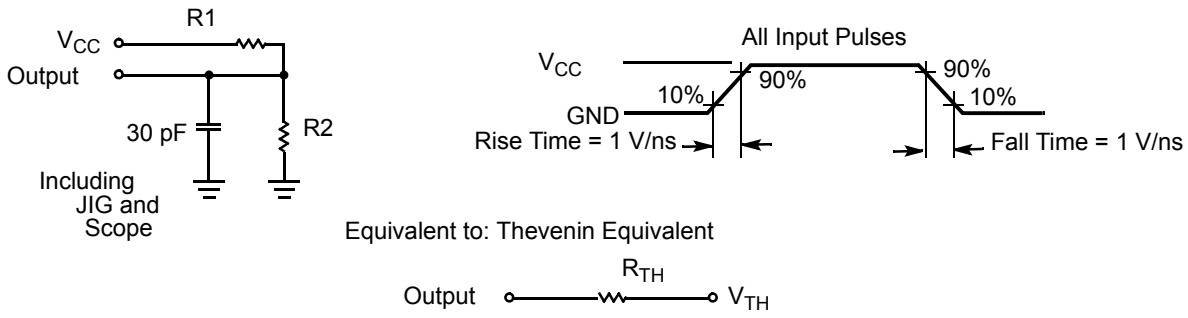
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	VFBGA	TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	42.10	55.52	°C/W
Θ_{JC}	Thermal resistance (junction to case)		23.45	16.03	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
9. Tested initially and after any design or process changes that may affect these parameters.

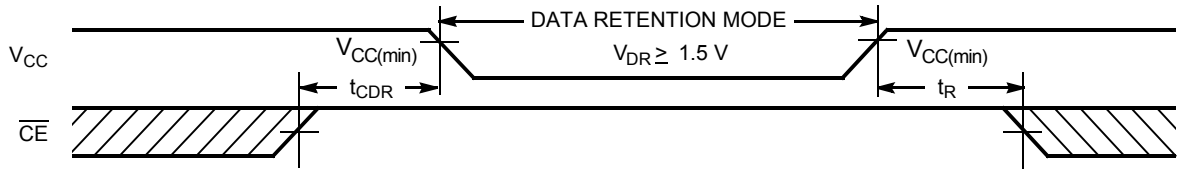
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [11]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial / Automotive-A	–	0.8	7	µA
t_{CDR} [12]	Chip deselect to data retention time	–		0	–	–	ns
t_R [13]	Operation recovery time	–		45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1}/ I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	45	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z [16]	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z [16, 17]	–	18	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [16]	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 3 on page 5.
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write
19. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled) [20, 21]

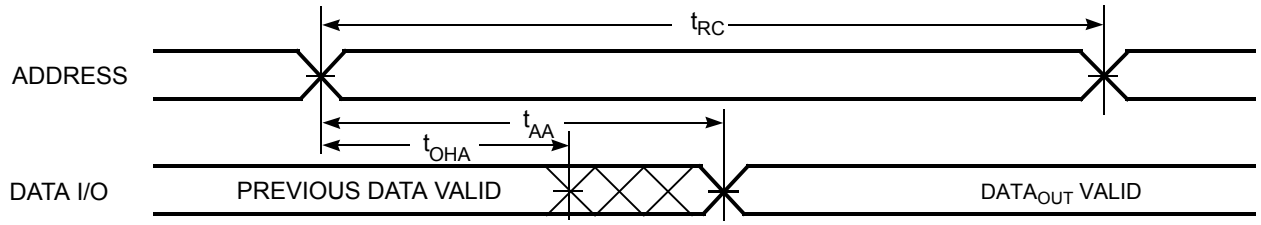
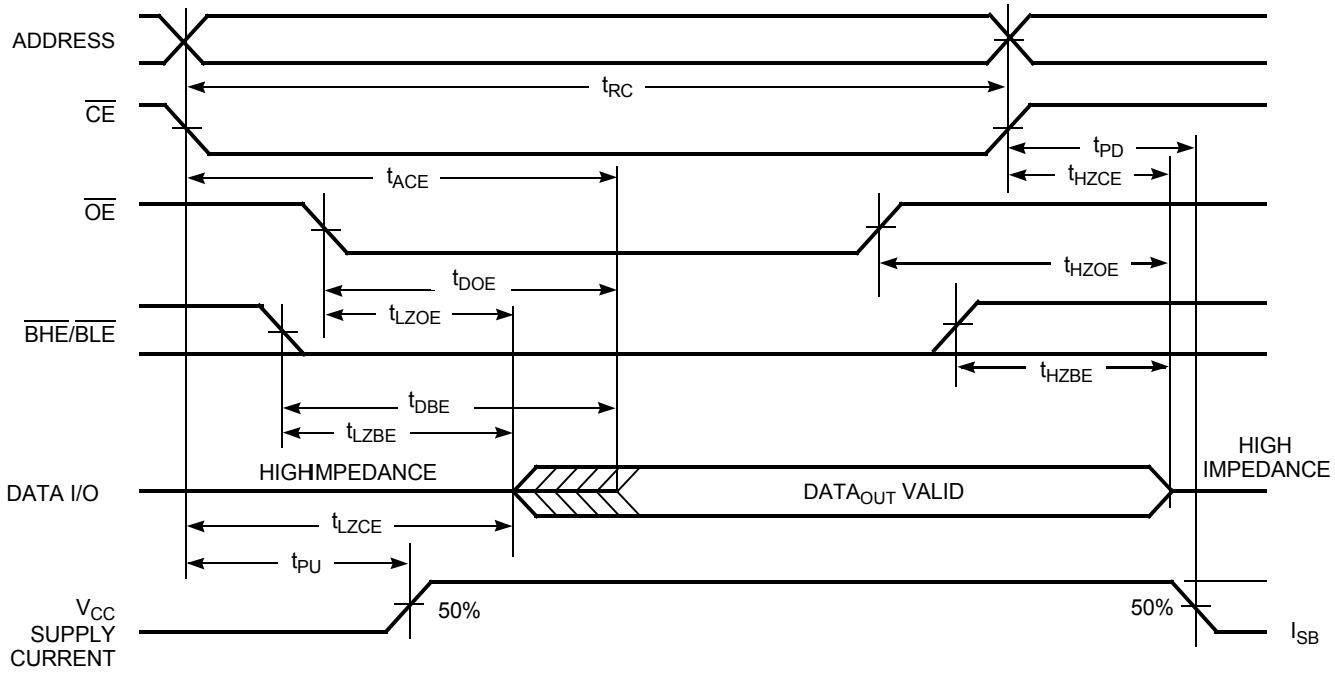


Figure 6. Read Cycle No. 2 (OE Controlled) [21, 22]



Notes
20. The device is continuously selected. OE, CE = V_{IL}, BHE and/or BLE = V_{IL}.
21. WE is HIGH for read cycle.
22. Address valid before or similar to CE and BHE, BLE transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (WE Controlled) [23, 24, 25]

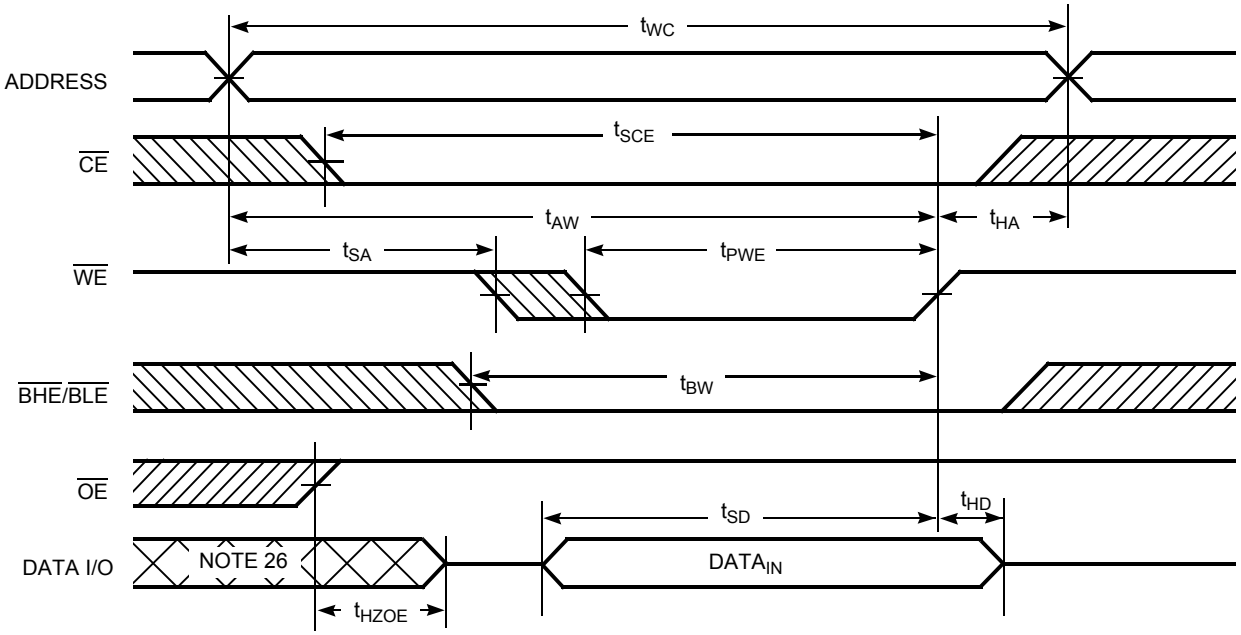
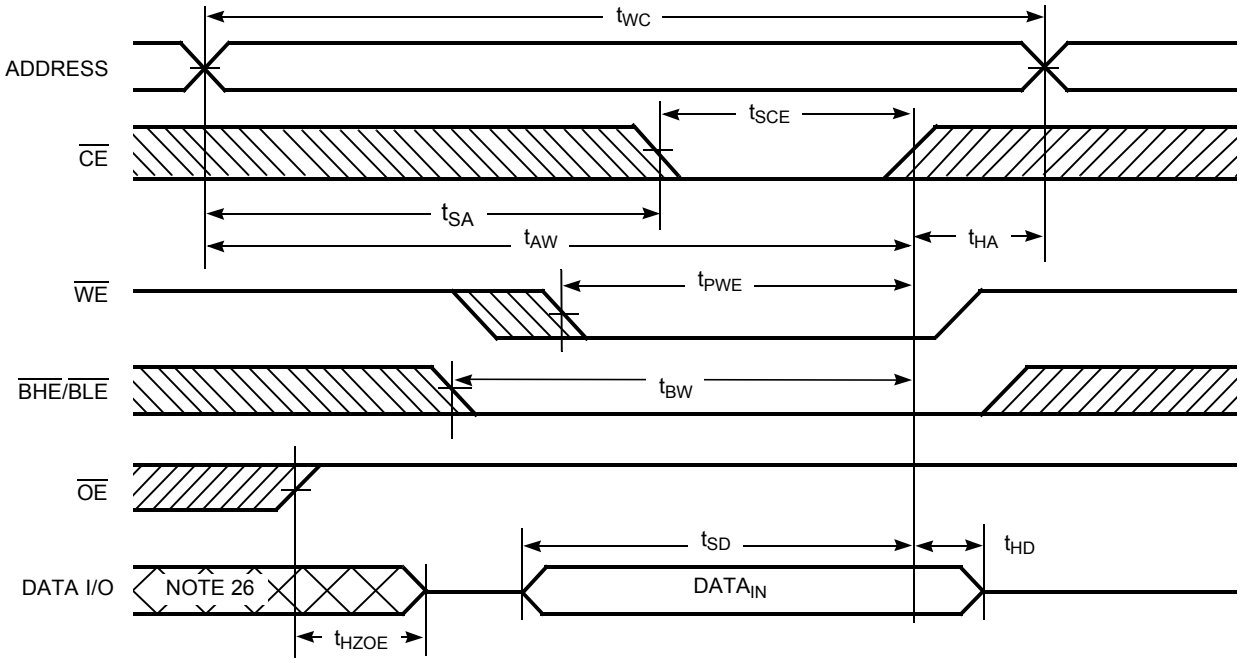


Figure 8. Write Cycle No. 2 (CE Controlled) [23, 24, 25]



Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
25. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
26. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (WE Controlled, OE LOW) [27, 28]

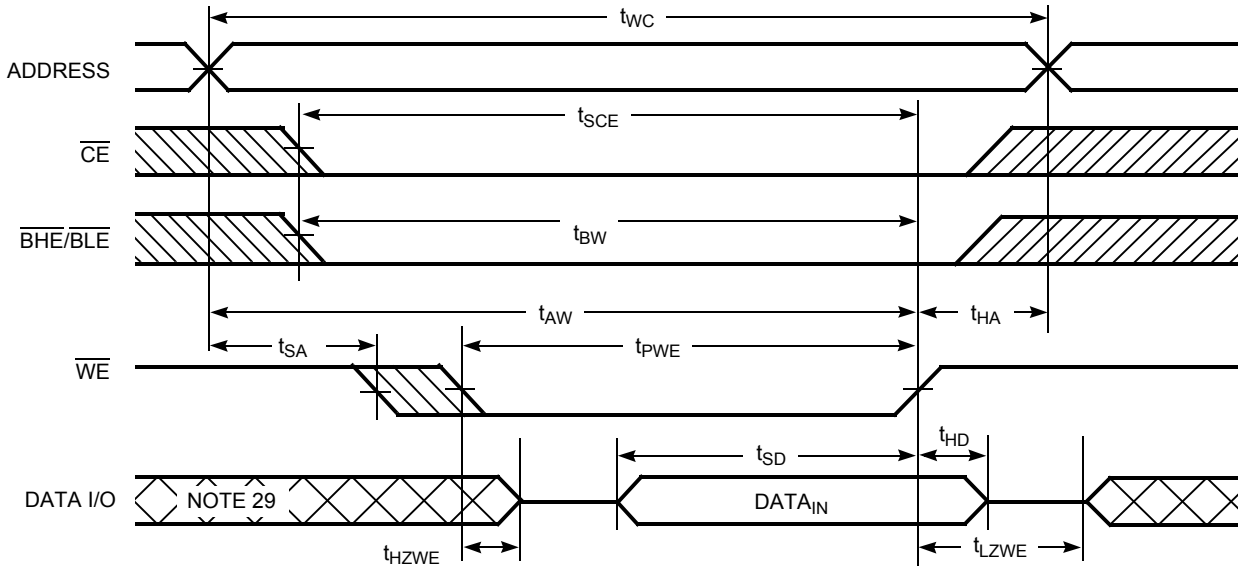
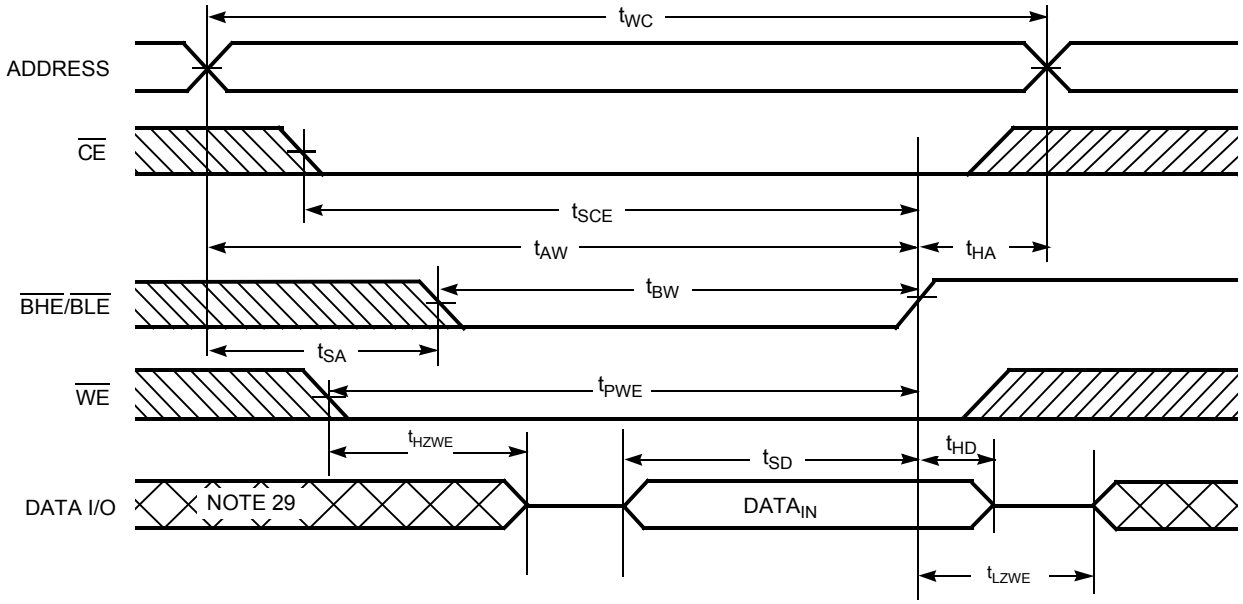


Figure 10. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [27]



Notes
27. If CE goes HIGH simultaneously with WE = V_{IH}, the output remains in a high impedance state.
28. The minimum write pulse width for Write Cycle No. 3 (WE Controlled, OE LOW) should be sum of t_{HZWE} and t_{SD}.
29. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{CE}$ [30]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/power-down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Write	Active (I_{CC})

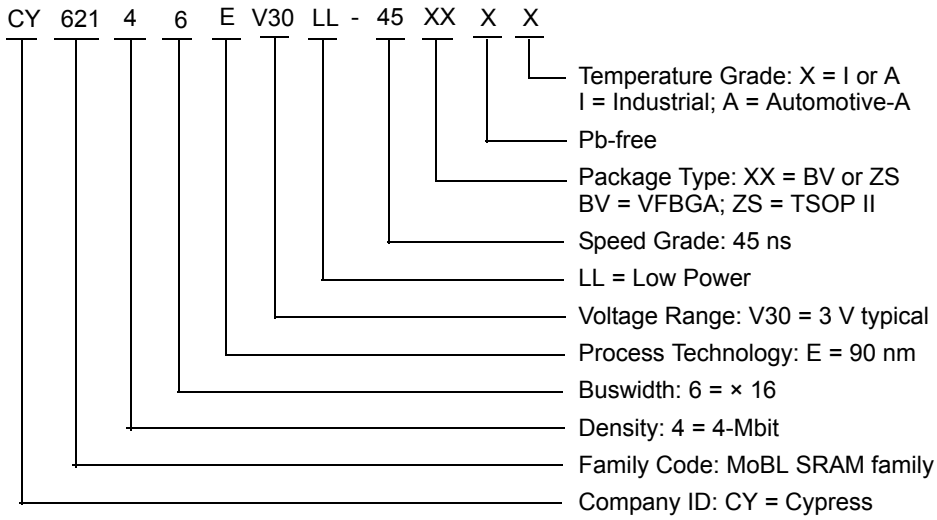
Note
30. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62146EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	
	CY62146EV30LL-45ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A

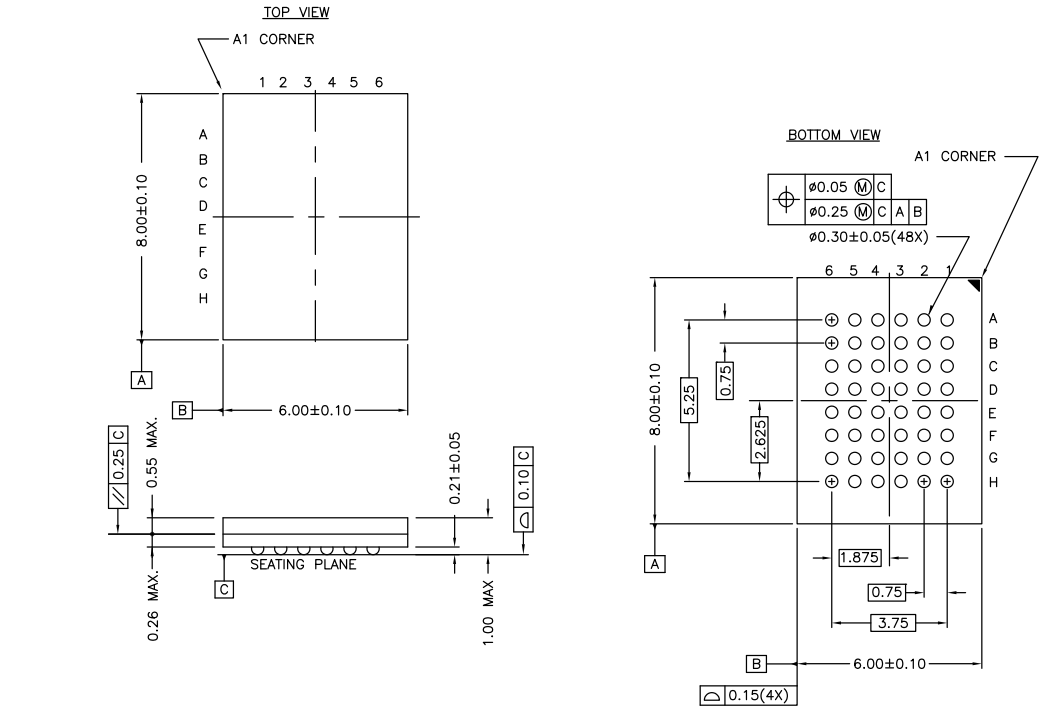
Please contact your local Cypress sales representative for availability of other parts

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

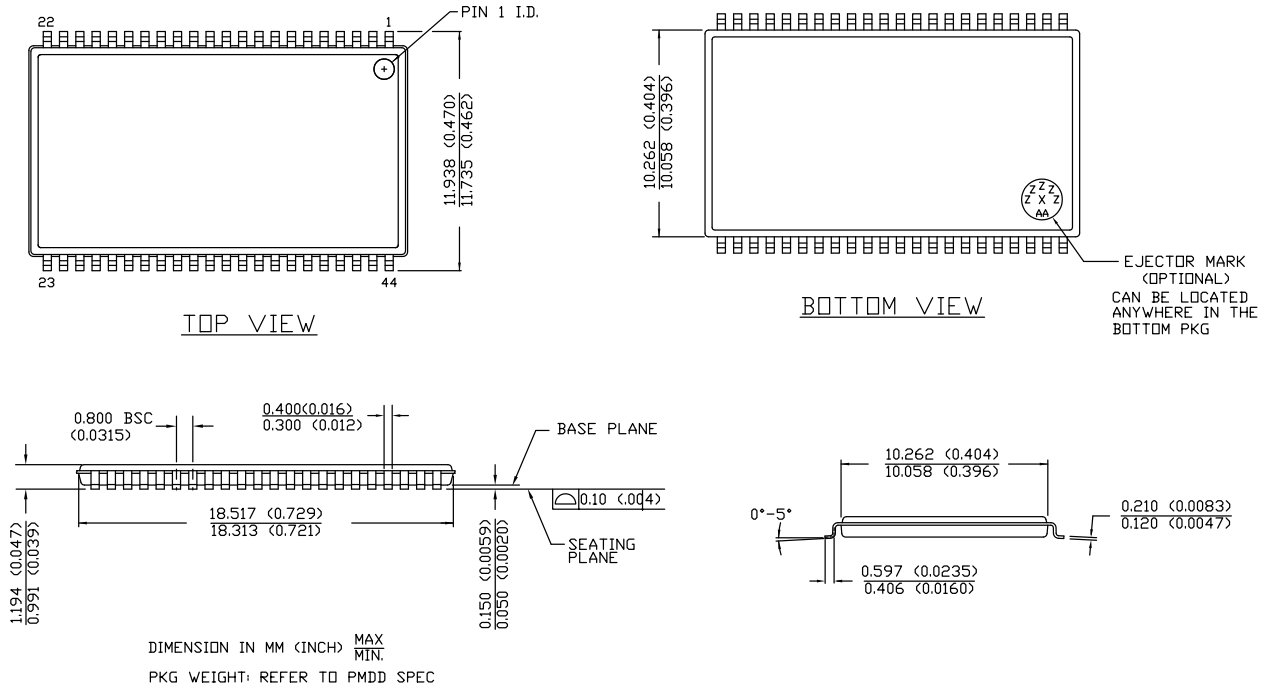


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Gird Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62146EV30 MoBL®, 4-Mbit (256K × 16) Static RAM Document Number: 38-05567				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	223225	AJU	See ECN	New data sheet.
*A	247373	SYT	See ECN	Changed status from Advance Information to Preliminary. Moved Product Portfolio to Page 2 Changed V_{CC} stabilization time in footnote #8 from 100 µs to 200 µs Removed Footnote #14(t_{LZBE}) from Previous revision Changed I_{CCDR} from 2.0 µA to 2.5 µA Changed typo in Data Retention Characteristics (t_R) from 100 µs to t_{RC} ns Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed t_{SCE} and t_{BW} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed t_{HZCE} from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Changed t_{DBE} from 15 to 18 ns for 35 ns Speed Bin Changed Ordering Information to include Pb-Free Packages
*B	414807	ZSD	See ECN	Changed status from Preliminary to Final. Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Removed 35ns Speed Bin Removed “L” version of CY62146EV30 Changed ball E3 from DNU to NC Removed the redundant foot note on DNU. Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max} Changed I_{SB1} and I_{SB2} Typ values from 0.7 µA to 1 µA and Max values from 2.5 µA to 7 µA. Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed I_{CCDR} from 2.5 µA to 7 µA. Added I_{CCDR} typical value. Changed t_{LZOE} from 3 ns to 5 ns Changed t_{LZCE} and t_{LZWE} from 6 ns to 10 ns Changed t_{LZBE} from 6 ns to 5 ns Changed t_{HZCE} from 22 ns to 18 ns Changed t_{PWE} from 30 ns to 35 ns. Changed t_{SD} from 22 ns to 25 ns. Updated the package diagram 48-ball VFBGA from *B to *D Updated the ordering information table and replaced the Package Name column with Package Diagram.
*C	925501	VKN	See ECN	Added footnote #8 related to I_{SB2} and I_{CCDR} Added footnote #12 related AC timing parameters
*D	2678796	VKN / PYRS	03/25/2009	Added Automotive-A information in all instances across the document.
*E	2944332	VKN	06/04/2010	Added Contents Removed byte enable from footnote #2 in Electrical Characteristics Added footnote related to chip enable in Truth Table Updated Package Diagrams. Updated links in Sales, Solutions, and Legal Information.

Document History Page (continued)

Document Title: CY62146EV30 MoBL®, 4-Mbit (256K × 16) Static RAM Document Number: 38-05567				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	3109050	PRAS	12/13/2010	Changed Table Footnotes to Footnotes. Added Ordering Code Definitions.
*G	3302915	RAME	07/14/2011	Removed the references of AN1064 SRAM system guidelines from the datasheet. Updated all the notes. Updated Ordering Code Definitions. Added Units of Measure. Updated to new template.
*H	3961126	TAVA	04/10/2013	Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *H. spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.
*I	4101995	VINI	08/22/2013	Updated Switching Characteristics: Updated Note 15. Updated to new template.
*J	4348752	MEMJ	04/16/2014	Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle” (for t_{PWE} parameter in WE controlled, OE LOW Write cycle). Updated Switching Waveforms: Added Note 28 and referred the same note in Figure 9 (for t_{PWE} parameter in WE controlled, OE LOW Write cycle). Completing Sunset Review.
*K	4576526	MEMJ	11/21/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*L	5233278	VINI	04/21/2016	Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated all values in “VFBGA” and “TSOP II” columns. Updated to new template. Completing Sunset Review.

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