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# 3-Mbit (128K × 24) Static RAM

#### **Features**

- High speed

  □ t<sub>AA</sub> = 10 ns
- Low active power
  □ I<sub>CC</sub> = 175 mA at f = 100 MHz
- Low CMOS standby power
  □ I<sub>SB2</sub> = 25 mA
- Operating voltages of 3.3 ± 0.3 V
- 2.0 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3$  features
- Available in Pb-free standard 119-ball PBGA

## **Functional Description**

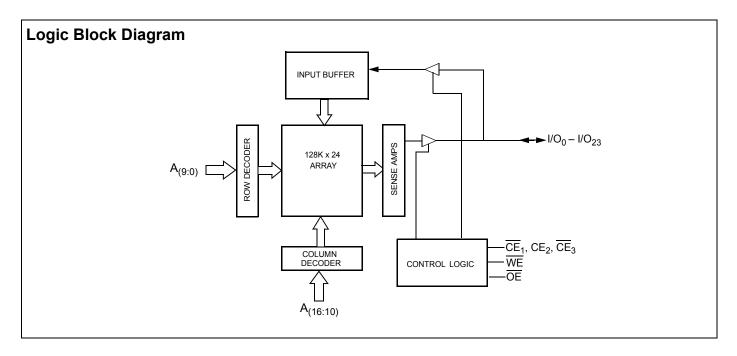
The CY7C1024DV33 is a high performance CMOS static RAM organized as 128 K words by 24 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

To write to the device, enable the chip ( $\overline{\text{CE}}_1$  LOW,  $\text{CE}_2$  HIGH, and  $\overline{\text{CE}}_3$  LOW), while forcing the Write Enable ( $\overline{\text{WE}}$ ) input LOW.

To read from the device, enable the chip by taking  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{CE}_3$  LOW while forcing the Output Enable ( $\overline{OE}$ ) LOW and the Write Enable ( $\overline{WE}$ ) HIGH. See the Truth Table on page 7 for a complete description of Read and Write modes.

The 24 I/O pins (I/O $_0$  to I/O $_2$ 3) are placed in a high impedance state when the device is deselected (CE $_1$  HIGH, CE $_2$  LOW, or CE $_3$  HIGH) or when the output enable (OE) is HIGH during a write operation. (CE $_1$  LOW, CE $_2$  HIGH, CE $_3$  LOW, and WE LOW).

For a complete list of related documentation, click here.





# **Selection Guide**

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	175	mA
Maximum CMOS standby current	25	mA

# **Pin Configuration**

Figure 1. 119-Ball PBGA Top View [1]

	1	2	3	4	5	6	7
Α	NC	Α	Α	Α	Α	Α	NC
В	NC	Α	Α	CE <sub>1</sub>	Α	Α	NC
С	I/O <sub>12</sub>	NC	CE <sub>2</sub>	NC	CE <sub>3</sub>	NC	I/O <sub>0</sub>
D	I/O <sub>13</sub>	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	I/O <sub>1</sub>
E	I/O <sub>14</sub>	$V_{SS}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{SS}$	I/O <sub>2</sub>
F	I/O <sub>15</sub>	$V_{DD}$	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	$V_{DD}$	I/O <sub>3</sub>
G	I/O <sub>16</sub>	$V_{SS}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{SS}$	I/O <sub>4</sub>
Н	I/O <sub>17</sub>	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	I/O <sub>5</sub>
J	NC	$V_{SS}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{SS}$	NC
K	I/O <sub>18</sub>	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	I/O <sub>6</sub>
L	I/O <sub>19</sub>	$V_{SS}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{SS}$	I/O <sub>7</sub>
M	I/O <sub>20</sub>	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	I/O <sub>8</sub>
N	I/O <sub>21</sub>	$V_{SS}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{SS}$	I/O <sub>9</sub>
Р	I/O <sub>22</sub>	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	I/O <sub>10</sub>
R	I/O <sub>23</sub>	NC	NC	NC	NC	NC	I/O <sub>11</sub>
T	NC	Α	Α	WE	Α	Α	NC
U	NC	Α	Α	ŌĒ	Α	Α	NC

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Note
1. NC pins are not connected on the die.



### **Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested. Ambient temperature with power applied .......55 °C to +125 °C Supply Voltage on  $V_{CC}$  Relative to GND  $^{[2]}$ ..-0.5 V to +4.6 V

DC Voltage Applied to Outputs in high Z state  $^{[2]}$ ......-0.5 V to  $V_{CC}$  + 0.5 V

DC input voltage [2]	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Current into outputs (LOW)	20 mA
Static discharge voltage	>2001 V
(MIL-STD-883, method 3015)	
Latch-up current	>200 mA

# **Operating Range**

Range	Ambient Temperature	V <sub>cc</sub>	
Industrial	–40 °C to +85 °C	$3.3~V\pm0.3~V$	

#### **DC Electrical Characteristics**

Over the Operating Range

Dovernator	Description	Test Conditions [3]	_	11:4	
Parameter	Description	rest Conditions (2)	Min	Max	Unit
V <sub>OH</sub>	Output HIGH voltage	Min $V_{CC}$ , $I_{OH} = -4.0 \text{ mA}$	2.4		V
V <sub>OL</sub>	Output LOW voltage	$Min V_{CC}, I_{OL} = 8.0 mA$		0.4	V
V <sub>IH</sub>	Input HIGH voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub> [2]	Input LOW voltage		-0.3	0.8	V
I <sub>IX</sub>	Input leakage current	$GND \le V_{IN} \le V_{CC}$	-1	+1	μΑ
I <sub>OZ</sub>	Output leakage current	$GND \le V_{OUT} \le V_{CC}$ , output disabled	-1	+1	μΑ
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	$\begin{aligned} &\text{Max V}_{\text{CC}},  \text{f = f}_{\text{MAX}} = 1/\text{t}_{\text{RC}} \\ &\text{I}_{\text{OUT}} = 0   \text{mA CMOS levels} \end{aligned}$		175	mA
I <sub>SB1</sub>	Automatic CE power-down current —TTL inputs	Max $V_{CC}$ , $\overline{CE} \ge V_{IH}$ $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ , $f = f_{MAX}$		30	mA
I <sub>SB2</sub>	Automatic CE power-down current — CMOS inputs	Max $V_{CC}$ , $\overline{CE} \ge V_{CC} - 0.3 \text{ V}$ , $V_{IN} \ge V_{CC} - 0.3 \text{ V}$ , or $V_{IN} \le 0.3 \text{ V}$ , f = 0		25	mA

#### Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	ter Description Test Conditions		Max	Unit	
C <sub>IN</sub>	Input capacitance	$T_A = 25 ^{\circ}\text{C}$ , f = 1 MHz, $V_{CC} = 3.3 \text{V}$	8	pF	
C <sub>OUT</sub>	I/O capacitance		10	pF	

#### Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	119-Ball PBGA	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	20.31	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		8.35	°C/W

#### Notes

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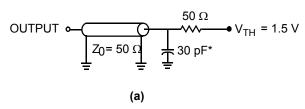
<sup>2.</sup>  $V_{IL}$  (min) = -2.0 V and  $V_{IH}$ (max) =  $V_{CC}$  + 2 V for pulse durations of less than 20 ns.
3.  $\overline{CE}$  refers to a combination of  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$ .  $\overline{CE}$  is LOW when  $\overline{CE}_1$  are LOW and  $\overline{CE}_2$  is HIGH.  $\overline{CE}$  is HIGH when  $\overline{CE}_1$  is HIGH, or  $\overline{CE}_2$  is LOW, or  $\overline{CE}_3$  is HIGH.



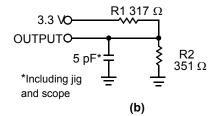
#### **AC Test Loads and Waveforms**

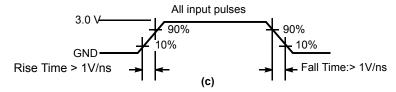
The AC test loads and waveform diagram follows.

Figure 2. AC Test Loads and Waveform<sup>[4]</sup>



\*Capacitive Load consists of all components of the test environment





### **AC Switching Characteristics**

Over the Operating Range [5]

Parameter	Description	-	10	Unit	
Parameter	Description	Min	Max	Unit	
Read Cycle		·			
t <sub>power</sub> <sup>[6]</sup>	V <sub>CC</sub> (Typical) to the first access	100	_	μS	
t <sub>RC</sub>	Read cycle time	10	-	ns	
t <sub>AA</sub>	Address to data valid	-	10	ns	
t <sub>OHA</sub>	Data hold from address change	3	_	ns	
t <sub>ACE</sub>	CE active LOW to data valid [3]	-	10	ns	
t <sub>DOE</sub>	OE LOW to data valid	_	5	ns	
t <sub>LZOE</sub>	OE LOW to low Z [7]	1	_	ns	
t <sub>HZOE</sub>	OE HIGH to high Z [7]	_	5	ns	
t <sub>LZCE</sub>	CE active LOW to low Z [3, 7]	3	_	ns	
t <sub>HZCE</sub>	CE deselect HIGH to high Z [3, 7]	_	5	ns	
t <sub>PU</sub>	CE active LOW to power-up [3, 8]	0	-	ns	
t <sub>PD</sub>	CE deselect HIGH to power-down [3, 8]	_	10	ns	

#### Notes

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V<sub>DD</sub> (3.0 V). 100  $\mu$ s (t<sub>power</sub>) after reaching the minimum operating V<sub>DD</sub>, normal SRAM operation can begin including reduction in V<sub>DD</sub> to the data retention (V<sub>CCDR</sub>, 2.0 V) voltage.

  Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading as shown in part a) of Figure 2, unless specified otherwise.
- $t_{POWER}$  gives the minimum amount of time that the power supply is at typical  $V_{CC}$  values until the first memory access is performed.
- thzoe, thzoe, thzwe, tzze, and tzze, and tzze are specified with a load capacitance of 5 pF as in part (b) of Figure 2. Transition is measured ±200 mV from steady state voltage.
- 8. These parameters are guaranteed by design and are not tested.



#### AC Switching Characteristics (continued)

Over the Operating Range [5]

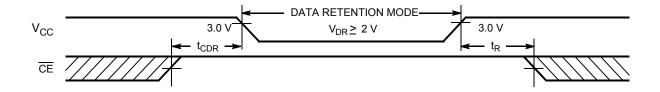
Parameter	Description	_	-10		
		Min	Max	Unit	
Write Cycle [9, 1	0]		•	•	
t <sub>WC</sub>	Write cycle time	10	_	ns	
t <sub>SCE</sub>	CE active LOW to write end [3]	7	_	ns	
t <sub>AW</sub>	Address setup to write end	7	-	ns	
t <sub>HA</sub>	Address hold from write end	0	-	ns	
t <sub>SA</sub>	Address setup to write start	0	-	ns	
t <sub>PWE</sub>	WE pulse width	7	_	ns	
t <sub>SD</sub>	Data setup to write end	5.5	-	ns	
t <sub>HD</sub>	Data hold from write end	0	_	ns	
t <sub>LZWE</sub>	WE HIGH to low Z [7]	3	-	ns	
t <sub>HZWE</sub>	WE LOW to high Z [7]	_	5	ns	

#### **Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions [3]	Min	Тур	Max	Unit
$V_{DR}$	V <sub>CC</sub> for data retention		2	_	_	V
I <sub>CCDR</sub>	Data retention current	$V_{CC} = 2 \text{ V}, \overline{CE} \ge V_{CC} - 0.2 \text{ V}, \\ V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$	_	_	25	mA
t <sub>CDR</sub> [11]	Chip deselect to data retention time		0	_	_	ns
t <sub>R</sub> <sup>[12]</sup>	Operation recovery time		t <sub>RC</sub>	_	_	ns

#### **Data Retention Waveform**



#### Notes

- 9. The internal write time of the memory is defined by the overlap of \(\overline{CE}\_1\) and \(\overline{CE}\_2\) and \(\overline{CE}\_3\) LOW and \(\overline{WE}\) LOW. Chip enables must be active and \(\overline{WE}\) must be LOW to initiate a write. The transition of any of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
- 10. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .
- 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \ge 50 \, \mu s$  or stable at  $V_{CC(min)} \ge 50 \, \mu s$ .

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#### **Switching Waveforms**

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [13, 14]

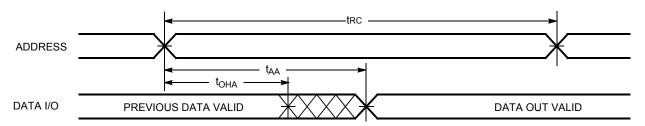


Figure 4. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled) [3, 14, 15]

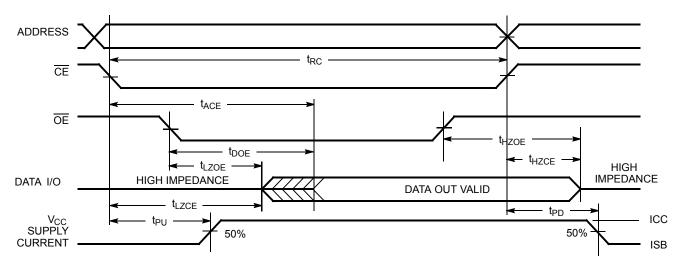
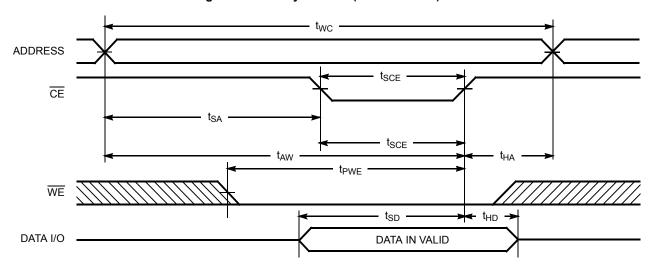


Figure 5. Write Cycle No. 1 (CE Controlled) [3, 16, 17]



- 13. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- 14. WE is HIGH for read cycle.
- 15. Address valid before or similar to  $\overline{\text{CE}}$  transition LOW.
- 16. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

  17. If  $\overline{CE}$  goes HIGH simultaneously with WE going HIGH, the output remains in a high impedance state.

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#### Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 (WE Controlled, OE HIGH During Write) [3, 16, 17]

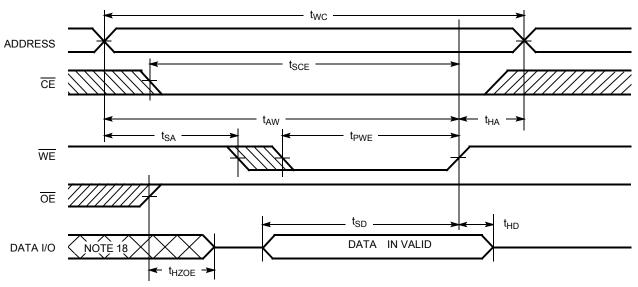
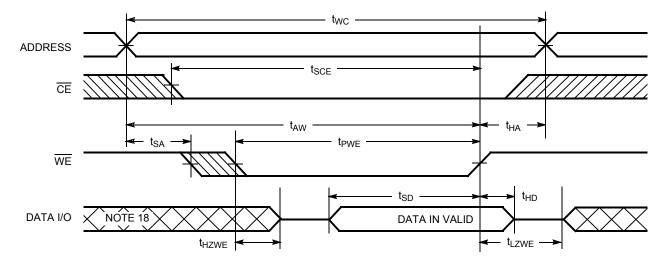


Figure 7. Write Cycle No. 3 (WE Controlled,  $\overline{\text{OE}}$  LOW) [3, 17, 19]



#### **Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	CE <sub>3</sub>	OE	WE	I/O <sub>0</sub> -I/O <sub>23</sub>	Mode	Power
Н	Х	Х	Χ	Х	High Z	Power-down	Standby (I <sub>SB</sub> )
Х	L	Х	Х	Х	High Z	Power-down	Standby (I <sub>SB</sub> )
Х	Х	Н	Х	Х	High Z	Power-down	Standby (I <sub>SB</sub> )
L	Н	L	L	Н	Full Data Out	Read	Active (I <sub>CC</sub> )
L	Н	L	Χ	L	Full Data In	Write	Active (I <sub>CC</sub> )
L	Н	L	Н	Н	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

#### Note

<sup>18.</sup> During this period, the I/Os are in the output state and input signals are not applied.

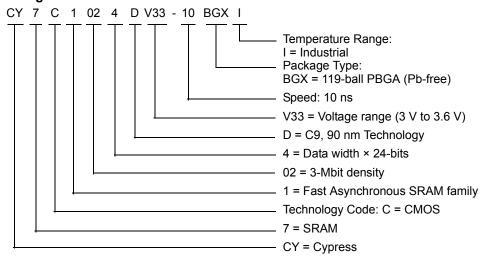
<sup>19.</sup> The minimum write cycle pulse width should be equal to the sum of tsD and tHZWE.



# **Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1024DV33-10BGXI	51-85115	119-ball Plastic Ball Grid Array (14 x 22 x 2.4 mm) (Pb-free)	Industrial

#### **Ordering Code Definitions**

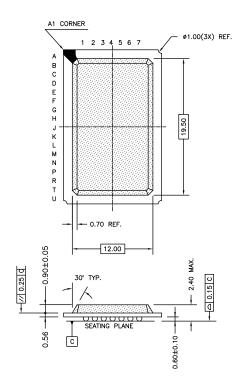


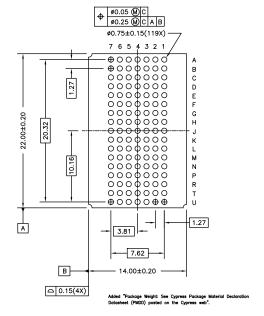
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# **Package Diagram**

Figure 8. 119-ball PBGA (14 x 22 x 2.4 mm)





51-85115 Rev. \*D



# **Acronyms**

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
TSOP	thin small outline package
TTL	Transistor-transistor logic

# **Document Conventions**

#### **Units of Measure**

Symbol	Unit of Measure			
°C	degrees Celsius			
μΑ	microamperes			
mA	milliamperes			
MHz	megahertz			
ns	nanoseconds			
pF	picofarads			
V	volts			
Ω	ohms			
W	watts			



# **Document History Page**

Document Title: CY7C1024DV33, 3-Mbit (128K × 24) Static RAM Document Number: 001-08353							
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change			
**	469517	NXR	See ECN	New data sheet			
*A	499604	NXR	See ECN	Added note 1 for NC pins Changed I <sub>CC</sub> specification from 150 mA to 185 mA Updated Test Condition for I <sub>CC</sub> in DC Electrical Characteristics table Added note for t <sub>ACE</sub> , t <sub>LZCE</sub> , t <sub>HZCE</sub> , t <sub>PU</sub> , t <sub>PD</sub> , t <sub>SCE</sub> in AC Switching Characteristics Table on page 4			
*B	1462586	VKN/SFV	See ECN	Converted from preliminary to final Updated block diagram Changed I <sub>CC</sub> specification from 185 mA to 225 mA Updated thermal specs			
*C	2604677	VKN/PYRS	11/12/08	Removed Commercial operating range, Added Industrial operating range Removed 8 ns speed bin, Added 10 ns speed bin			
*D	3109199	PRAS	12/13/2010	Added Ordering Code Definitions. Updated Package Diagram.			
*E	3388080	TAVA	09/29/2011	Minor technical edits. Added Acronyms and Document Conventions. Updated template.			
*F	4548836	MEMJ	10/22/2014	Updated Package Diagram spec 51-85115 – Changed revision from *C to *D Completing Sunset Review.			
*G	4576478	MEMJ	11/21/2014	Added related documentation hyperlink in page 1. Added Note 19 in Switching Waveforms. Added note reference 19 in Figure 7.			

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