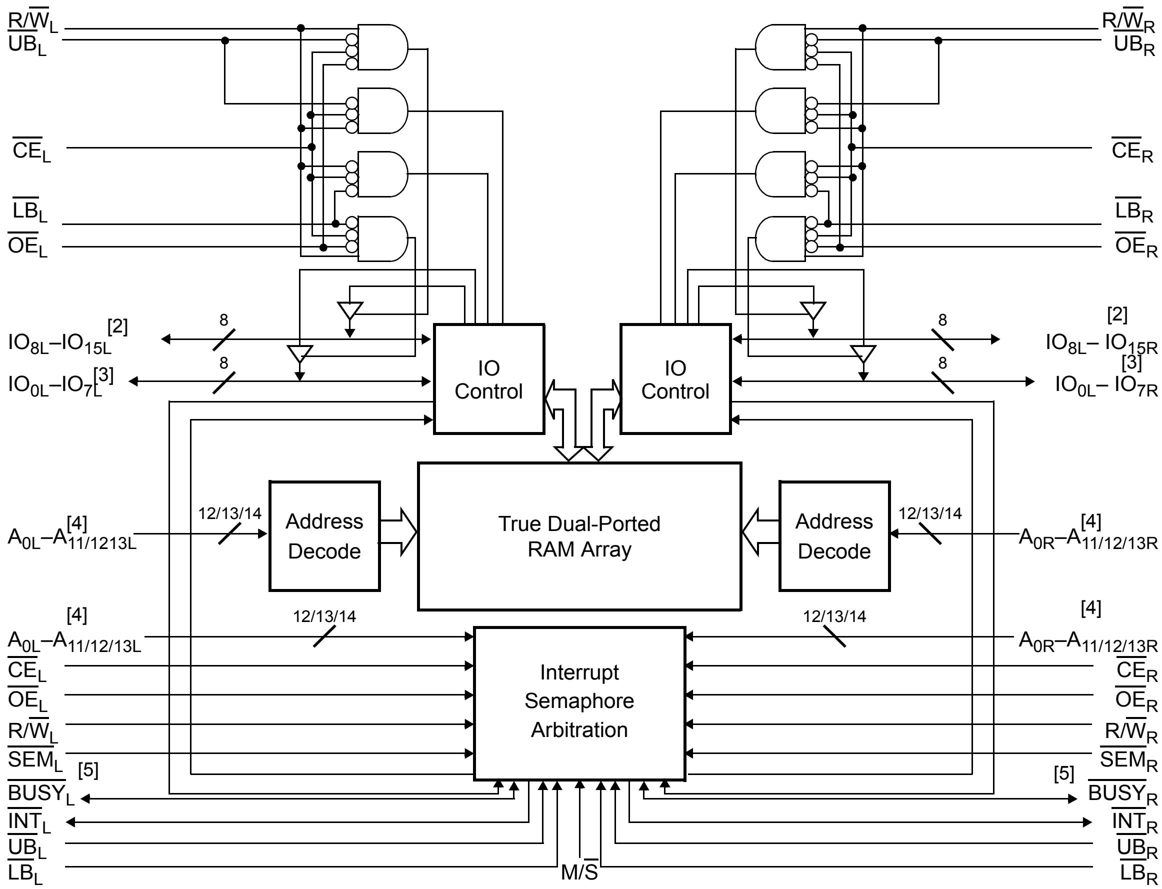
CY7C024AV/024BV/025AV/026AV

3.3 V 4 K / 8 K / 16 K × 16 Dual-Port Static RAM

Features

- True dual-ported memory cells which enable simultaneous access of the same memory location
- 4, 8 or 16 K × 16 organization (CY7C024AV/024BV [1] /025AV/026AV)
- 0.35 micron CMOS for optimum speed and power
- High speed access: 15 ns, 20 ns and 25 ns
- Low operating power
  - Active: I_{CC} = 115 mA (typical)
  - Standby: I_{SB3} = 10 µA (typical)
- Fully asynchronous operation
- Automatic power down
- Expandable data bus to 32 bits or more using Master and Slave chip select when using more than one device
- On chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{\text{INT}}$ flag for port-to-port communication
- Separate upper byte and lower byte control
- Pin select for Master or Slave (M/S)
- Commercial and industrial temperature ranges
- Available in 100-pin Pb-free TQFP and 100-pin TQFP

Logic Block Diagram

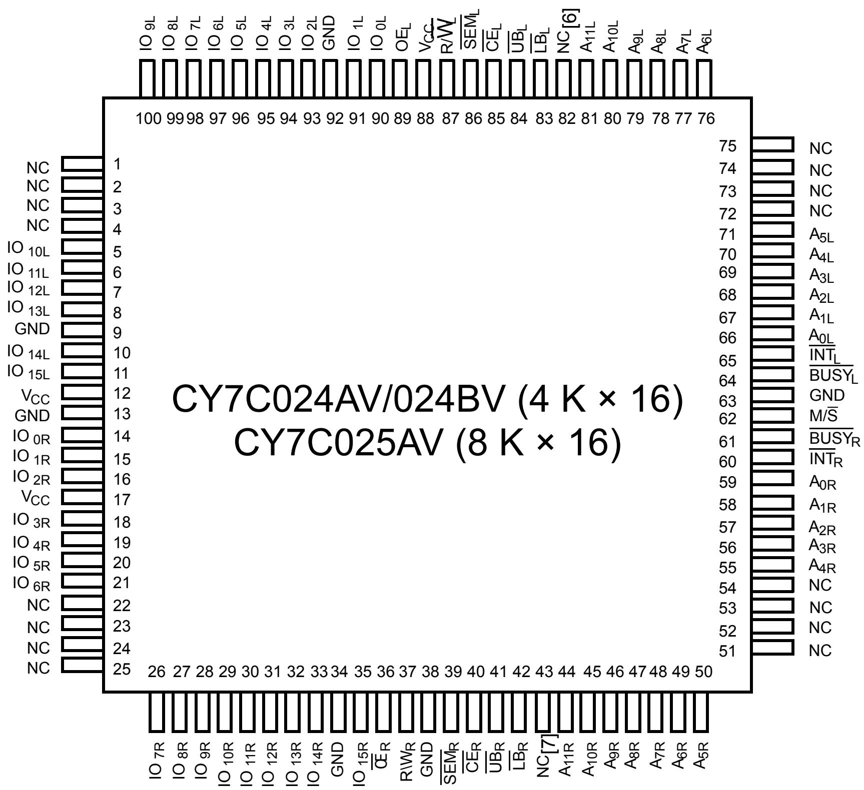


Notes
1. CY7C024AV and CY7C024BV are functionally identical.
2. IO_8–IO_{15} for × 16 devices
3. IO_0–IO_7 for × 16 devices
4. A_0–A_{11} for 4K devices; A_0–A_{12} for 8K devices; A_0–A_{13} for 16K devices.
5. $\overline{\text{BUSY}}$ is an output in master mode and an input in slave mode.

Contents

Pin Configurations

Figure 1. 100-pin TQFP (Top View)

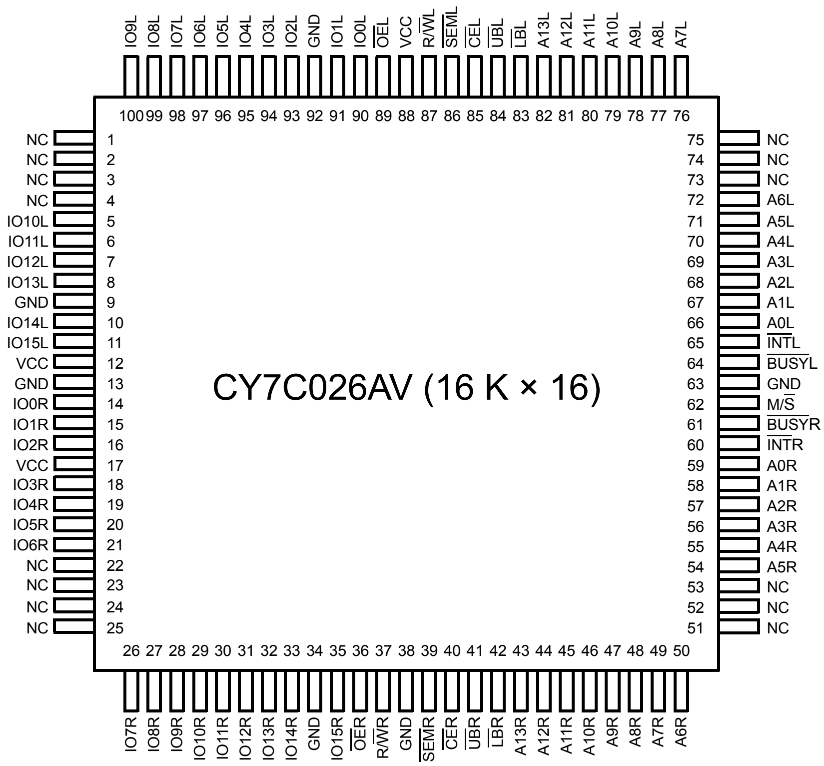


Notes

6. A_{12L} on the CY7C025AV.
7. A_{12R} on the CY7C025AV.

Pin Configurations (continued)

Figure 2. 100-pin TQFP (Top View)



Selection Guide

Parameter	CY7C024AV/024BV/025AV/026AV -20	CY7C024AV/024BV/025AV/026AV -25	Unit
Maximum Access Time	20	25	ns
Typical Operating Current	120	115	mA
Typical Standby Current for I_{SB1} (Both ports TTL Level)	35	30	mA
Typical Standby Current for I_{SB3} (Both ports CMOS Level)	10	10	µA

Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read and Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L}–A_{13L}	A_{0R}–A_{13R}	Address (A_0–A_{11} for 4K devices; A_0–A_{12} for 8K devices; A_0–A_{13} for 16K)
IO_{0L}–IO_{15L}	IO_{0R}–IO_{15R}	Data Bus Input and Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select (IO_8–IO_{15} for × 16 devices)
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select (IO_0–IO_7 for × 16 devices)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground
NC		No Connect

Architecture

The CY7C024AV/024BV/025AV/026AV consist of an array of 4 K, 8 K, and 16 K words of 16 bits each of dual-port RAM cells, IO and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, $R\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes and reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two Interrupt ($\overline{INT}$) pins can be used for port to port communication. Two Semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the $M/\overline{S}$ pin, the devices can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). They also have an automatic power down feature controlled by $\overline{CE}$. Each port has its own output enable control ($\overline{OE}$), which enables data to be read from the device.

Functional Description

The CY7C024AV/024BV/025AV/026AV are low power CMOS 4 K, 8 K, and 16 K × 16 dual port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. There are two ports permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be used as standalone 16-bit dual port static RAMs or multiple devices can be combined to function as a 32-bit or wider master and slave dual port static RAM. An $M/\overline{S}$ pin is provided for implementing 32-bit or wider memory applications. It does not need separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual port video and graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$), Read or Write Enable ($R/\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic has eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power down feature is controlled independently on each port by a Chip Select ($\overline{CE}$) pin.

The CY7C024AV/024BV/025AV/026AV are available in 100-pin Pb-free Thin Quad Flat Pack (TQFP) and 100-pin TQFP.

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of $R\overline{W}$ to guarantee a valid write. A write operation is controlled by either the $R\overline{W}$ pin (see Figure 7 on page 14) or the $\overline{CE}$ pin (see Figure 8 on page 14). Required inputs for non-contention operations are summarized in Table 1 on page 7.

If a location is being written to by one port and the opposite port tries to read that location, there must be a port to port flowthrough delay before the data is read on the output; otherwise the data read is not deterministic. Data is valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data is available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user wants to access a semaphore flag, then the $\overline{SEM}$ pin and $\overline{OE}$ must be asserted.

Interrupts

The upper two memory locations are for message passing. The highest memory location (FFF for the CY7C024AV/024BV, 1FFF for the CY7C025AV, 3FFF for the CY7C026AV) is the mailbox for the right port and the second highest memory location (FFE for the CY7C024AV/024BV, 1FFE for the CY7C025AV, 3FFE for the CY7C026AV) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in Table 2 on page 7*.*

Busy

The CY7C024AV/024BV/025AV/026AV provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{\text{CE}}$s are asserted and an address match occurs within t_{PS} of each other, the busy logic determines which port has access. If t_{PS} is violated, one port definitely gains permission to the location, but it is not predictable which port gets that permission. $\overline{\text{BUSY}}$ is asserted t_{BLA} after an address match or t_{BLC} after $\overline{\text{CE}}$ is taken LOW.

Master/Slave

A M/$\overline{\text{S}}$ pin helps to expand the word width by configuring the device as a master or a slave. The $\overline{\text{BUSY}}$ output of the master is connected to the $\overline{\text{BUSY}}$ input of the slave. This enables the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{\text{BUSY}}$ input has settled (t_{BLC} or t_{BLA}). Otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{\text{S}}$ pin enables the device to be used as a master and, therefore, the $\overline{\text{BUSY}}$ line is an output. $\overline{\text{BUSY}}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C024AV/024BV/025AV/026AV provide eight semaphore latches, which are separate from the dual port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{\text{SEM}}$ or $\overline{\text{OE}}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource. Otherwise (reads a one), it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{\text{SEM}}$ LOW. The $\overline{\text{SEM}}$ pin functions as a chip select for the semaphore latches ($\overline{\text{CE}}$ must remain HIGH during $\overline{\text{SEM}}$ LOW). A_{0-2} represents the semaphore address. $\overline{\text{OE}}$ and R/$\overline{\text{W}}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only IO_0 is used. If a zero is written to the left port of an available semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Table 3 on page 8 shows sample semaphore operations.

When reading a semaphore, all 16 data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one of them. But there is no guarantee which side controls the semaphore.

Table 1. Non-Contending Read/Write

Inputs						Outputs		Operation
$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	IO_8–IO_{15}	IO_0–IO_7	
H	X	X	X	X	H	High Z	High Z	Deselected: Power Down
X	X	X	H	H	H	High Z	High Z	Deselected: Power Down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H	_/¯	X	X	X	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
X	_/¯	X	H	H	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = HIGH) [8]

	Left Port					Right Port				
Function	$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L-13L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R-13R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	X	FFF [9]	X	X	X	X	X	L[10]
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	FFF (or 1/3FFF)	H[11]
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L[11]	L	L	X	FFE (or 1/3FFE)	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	FFE [9]	H[10]	X	X	X	X	X

Notes

8. See Functional Description on page 5 for specific highest memory locations by device.
9. See Functional Description on page 5 for specific addresses by device.
10. If $\overline{BUSY}_L$=L, then no change.
11. If $\overline{BUSY}_R$=L, then no change.

Table 3. Semaphore Operation Example

Function	$IO_0–IO_{15}$ Left	$IO_0–IO_{15}$ Right	Status
No action	1	1	Semaphore-free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free

Maximum Ratings

Exceeding maximum ratings [12] may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with
Power Applied .... –55 °C to +125 °C

Supply Voltage to Ground Potential ....–0.5 V to +4.6 V

DC Voltage Applied to
Outputs in High Z State ....–0.5 V to V_{CC} + 0.5 V

DC Input Voltage [13] .... –0.5 V to V_{CC} + 0.5 V

Output Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... > 2001 V

Latch-up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 300 mV
Industrial [14]	–40 °C to +85 °C	3.3 V ± 300 mV

Electrical Characteristics

Over the Operating Range

Parameter	Description		CY7C024AV/024BV/025AV/026AV						Unit
			-20			-25			
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (V_{CC} = Min, I_{OH} = –4.0 mA)		2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW Voltage (V_{CC} = Min, I_{OH} = +4.0 mA)		–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH Voltage		2.0	–	–	2.0	–	–	V
V_{IL}	Input LOW Voltage		–0.3 [15]	–	0.8		–	0.8	V
I_{OZ}	Output Leakage Current		–10	–	10	–10	–	10	µA
I_{IX}	Input Leakage Current		–10	–	10	–10	–	10	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA) Outputs Disabled	Commercial	–	120	175	–	115	165	mA
		Industrial [14]		–	–		135	185	mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE_L}$ & $\overline{CE_R}$ ≥ V_{IH}, f = f_{MAX}	Commercial		35	45		30	40	mA
		Industrial [14]		–	–		40	50	mA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE_L}$ | $\overline{CE_R}$ ≥ V_{IH}, f = f_{MAX}	Commercial		75	110		65	95	mA
		Industrial [14]		–	–		75	105	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE_L}$ & $\overline{CE_R}$ ≥ V_{CC} − 0.2 V, f = 0	Commercial		10	500		10	500	µA
		Industrial [14]		–	–		10	500	µA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE_L}$ | $\overline{CE_R}$ ≥ V_{IH}, f = f_{MAX} [16]	Commercial		70	95		60	80	mA
		Industrial [14]		–	–		70	90	mA

Notes

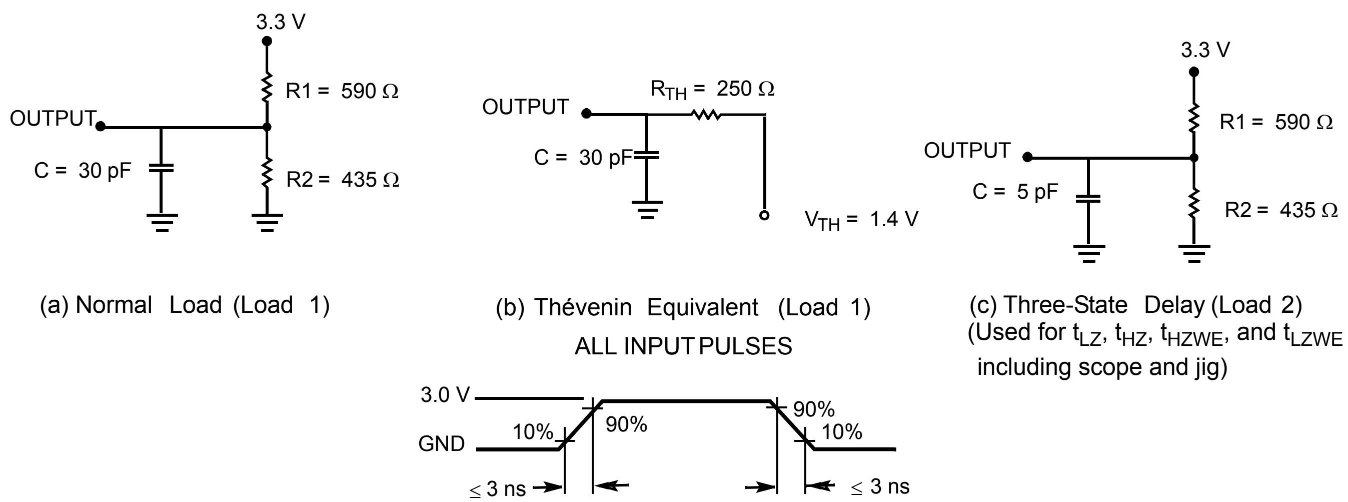
12. The voltage on any input or IO pin cannot exceed the power pin during power up.
13. Pulse width < 20 ns.
14. Industrial parts are available in CY7C024AV/024BV, CY7C025AV & CY7C026AV.
15. VIL ≥ –1.5V for pulse width less than 10ns.
16. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance

Parameter [17]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25\ °C$, f = 1 MHz, $V_{CC} = 3.3$ V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Note

17. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics

Over the Operating Range

Parameter [18]	Description	CY7C024AV/024BV/025AV/026AV				Unit
		-20		-25		
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read Cycle Time	20	–	25	–	ns
t_{AA}	Address to Data Valid	–	20	–	25	ns
t_{OHA}	Output Hold From Address Change	3	–	3	–	ns
t_{ACE}[19]	$\overline{CE}$ LOW to Data Valid	–	20	–	25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	12	–	13	ns
t_{LZOE}[20, 21, 22]	$\overline{OE}$ Low to Low Z	3	–	3	–	ns
t_{HZOE}[20, 21, 22]	$\overline{OE}$ HIGH to High Z	–	12	–	15	ns
t_{LZCE}[20, 21, 22]	$\overline{CE}$ LOW to Low Z	3	–	3	–	ns
t_{HZCE}[20, 21, 22]	$\overline{CE}$ HIGH to High Z	–	12	–	15	ns
t_{PU}[22]	$\overline{CE}$ LOW to Power Up	0	–	0	–	ns
t_{PD}[22]	$\overline{CE}$ HIGH to Power Down	–	20	–	25	ns
t_{ABE}[19]	Byte Enable Access Time	–	20	–	25	ns
Write Cycle						
t_{WC}	Write Cycle Time	20	–	25	–	ns
t_{SCE}[19]	$\overline{CE}$ LOW to Write End	15	–	20	–	ns
t_{AW}	Address Valid to Write End	15	–	20	–	ns
t_{HA}	Address Hold From Write End	0	–	0	–	ns
t_{SA}[19]	Address Setup to Write Start	0	–	0	–	ns
t_{PWE}	Write Pulse Width	15	–	20	–	ns
t_{SD}	Data Setup to Write End	15	–	15	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	ns
t_{HZWE}[21, 22]	R/$\overline{W}$ LOW to High Z	–	12	–	15	ns
t_{LZWE}[21, 22]	R/$\overline{W}$ HIGH to Low Z	3	–	0	–	ns
t_{WDD}[23]	Write Pulse to Data Delay	–	45	–	50	ns
t_{DDD}[23]	Write Data Valid to Read Data Valid	–	30	–	35	ns

Notes

18. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OI}/I_{OH} and 30 pF load capacitance.
19. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{ACE}/t_{SCE} time.
20. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
21. Test conditions used are Load 3.
22. This parameter is guaranteed but not tested. For information on port to port delay through RAM cells from writing port to reading port, refer to Figure 11.
23. For information on port to port delay through RAM cells from writing port to reading port, refer to Figure 11.

Switching Characteristics (continued)

Over the Operating Range

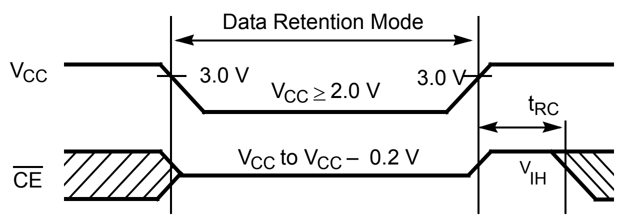
Parameter [18]	Description	CY7C024AV/024BV/025AV/026AV				Unit
		-20		-25		
		Min	Max	Min	Max	
Busy Timing [24]						
t_{BLA}	$\overline{\text{BUSY}}$ LOW from Address Match	–	20	–	20	ns
t_{BHA}	$\overline{\text{BUSY}}$ HIGH from Address Mismatch	–	20	–	20	ns
t_{BLC}	$\overline{\text{BUSY}}$ LOW from $\overline{\text{CE}}$ LOW	–	20	–	20	ns
t_{BHC}	$\overline{\text{BUSY}}$ HIGH from $\overline{\text{CE}}$ HIGH	–	17	–	17	ns
t_{PS}	Port Setup for Priority	5	–	5	–	ns
t_{WB}	R/$\overline{\text{W}}$ HIGH after $\overline{\text{BUSY}}$ (Slave)	0	–	0	–	ns
t_{WH}	R/$\overline{\text{W}}$ HIGH after $\overline{\text{BUSY}}$ HIGH (Slave)	15	–	17	–	ns
t_{BDD} [25]	$\overline{\text{BUSY}}$ HIGH to Data Valid	–	20	–	25	ns
Interrupt Timing [24]						
t_{INS}	$\overline{\text{INT}}$ Set Time	–	20	–	20	ns
t_{INR}	$\overline{\text{INT}}$ Reset Time	–	20	–	20	ns
Semaphore Timing						
t_{SOP}	SEM Flag Update Pulse ($\overline{\text{OE}}$ or $\overline{\text{SEM}}$)	10	–	12	–	ns
t_{SWRD}	SEM Flag Write to Read Time	5	–	5	–	ns
t_{SPS}	SEM Flag Contention Window	5	–	5	–	ns
t_{SAA}	SEM Address Access Time	–	20	–	25	ns

Data Retention Mode

The CY7C024AV/024BV/025AV/026AV are designed for battery backup. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{\text{CE}}$) must be held HIGH during data retention, within V_{CC} to $V_{CC} - 0.2$ V.
2. $\overline{\text{CE}}$ must be kept between $V_{CC} - 0.2$ V and 70 percent of V_{CC} during the power up and power down transitions.
3. The RAM can begin operation > t_{RC} after V_{CC} reaches the minimum operating voltage (3.0 V).

Timing



Parameter	Test Conditions [26]	Max	Unit
ICC_{DR1}	at $VCC_{DR} = 2$ V	50	μA

Notes

24. Test conditions used are Load 2.
25. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).
26. $\overline{\text{CE}} = V_{CC}$, V_{in} = GND to V_{CC}, $T_A = 25°C$. This parameter is guaranteed but not tested.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Either Port Address Access) [27, 28, 29]

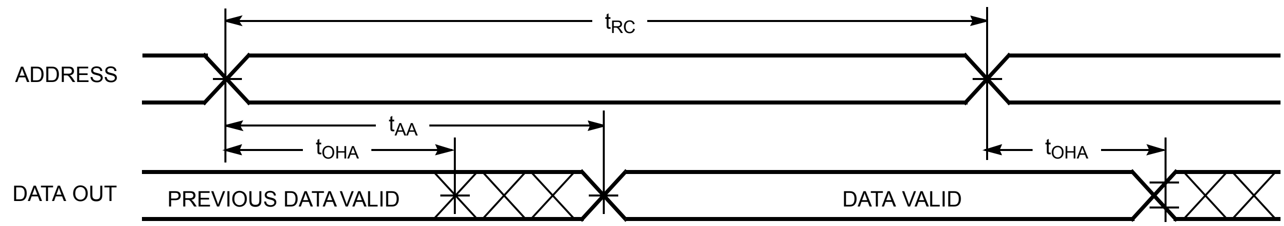


Figure 5. Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access) [27, 30, 31]

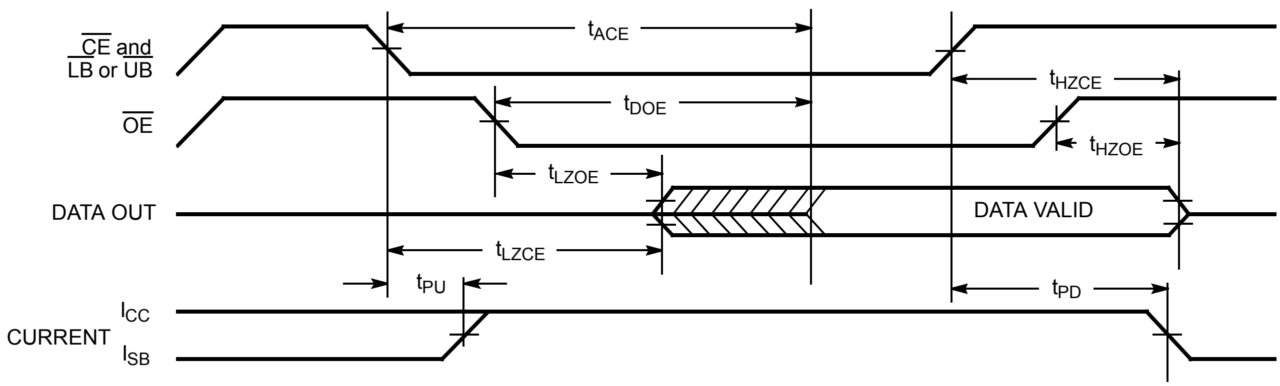
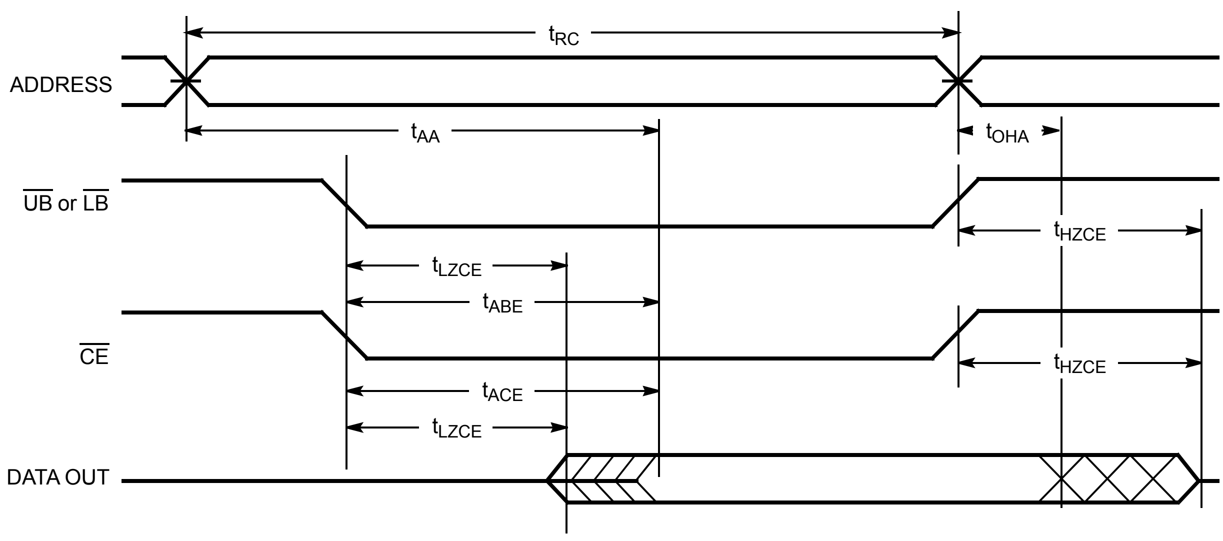


Figure 6. Read Cycle No. 3 (Either Port) [27, 29, 30, 31]



Notes
27. R/$\overline{W}$ is HIGH for read cycles.
28. Device is continuously selected $\overline{CE}$ = V_{IL} and $\overline{UB}$ or $\overline{LB}$ = V_{IL}. This waveform cannot be used for semaphore reads.
29. $\overline{OE}$ = V_{IL}.
30. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
31. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.

Switching Waveforms (continued)

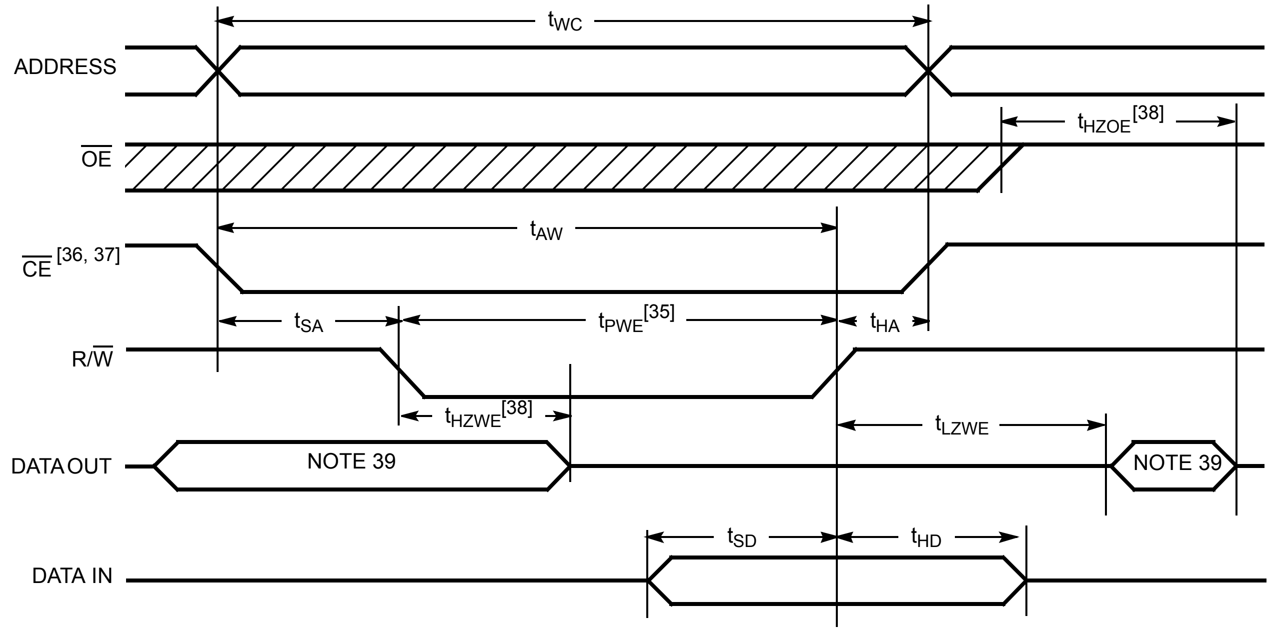


Figure 7. Write Cycle No. 1 (R/$\overline{W}$ Controlled Timing) [32, 33, 34, 35]

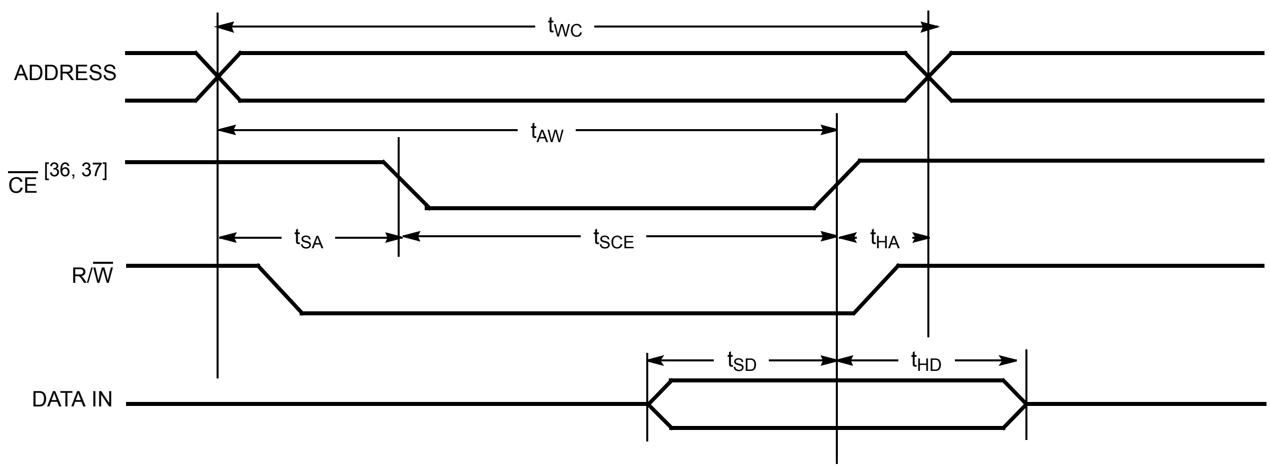


Figure 8. Write Cycle No. 2 ($\overline{CE}$ Controlled Timing) [32, 33, 34, 40]

Notes

32. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
33. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.
34. t_{HA} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
35. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to enable the IO drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
36. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
37. To access upper byte, $\overline{CE}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access lower byte, $\overline{CE}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
38. Transition is measured $\pm$500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100 percent tested.
39. During this period, the IO pins are in the output state, and input signals must not be applied.
40. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high impedance state.

Switching Waveforms (continued)

Figure 9. Semaphore Read after Write Timing, either side [41]

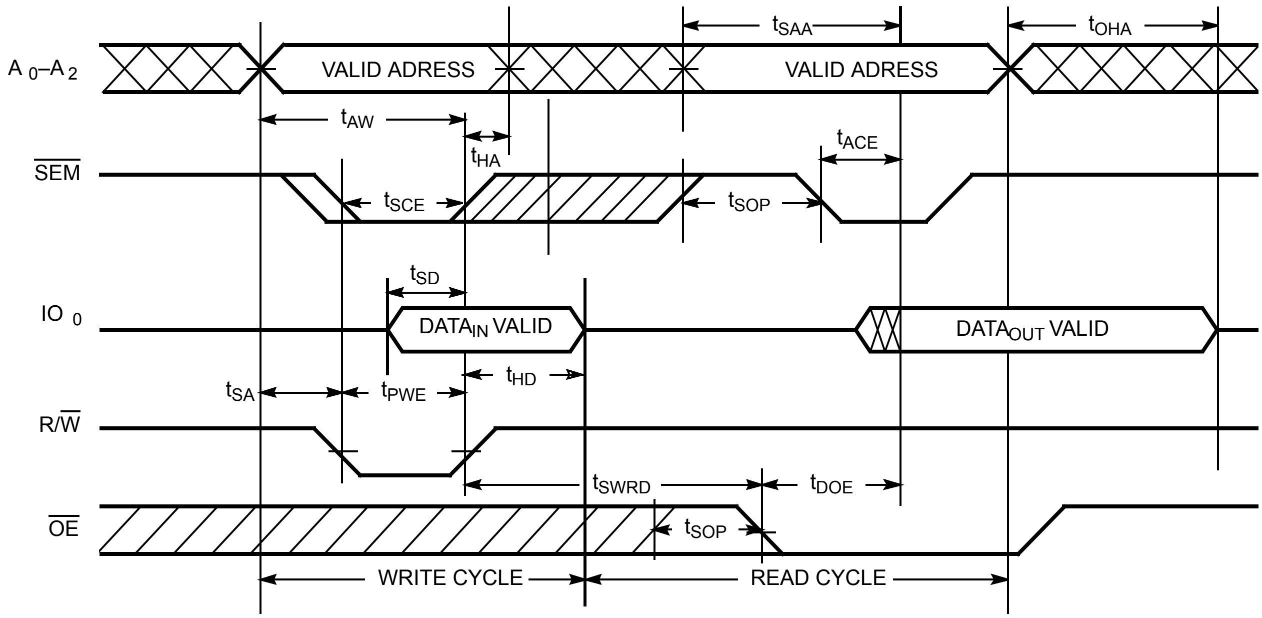
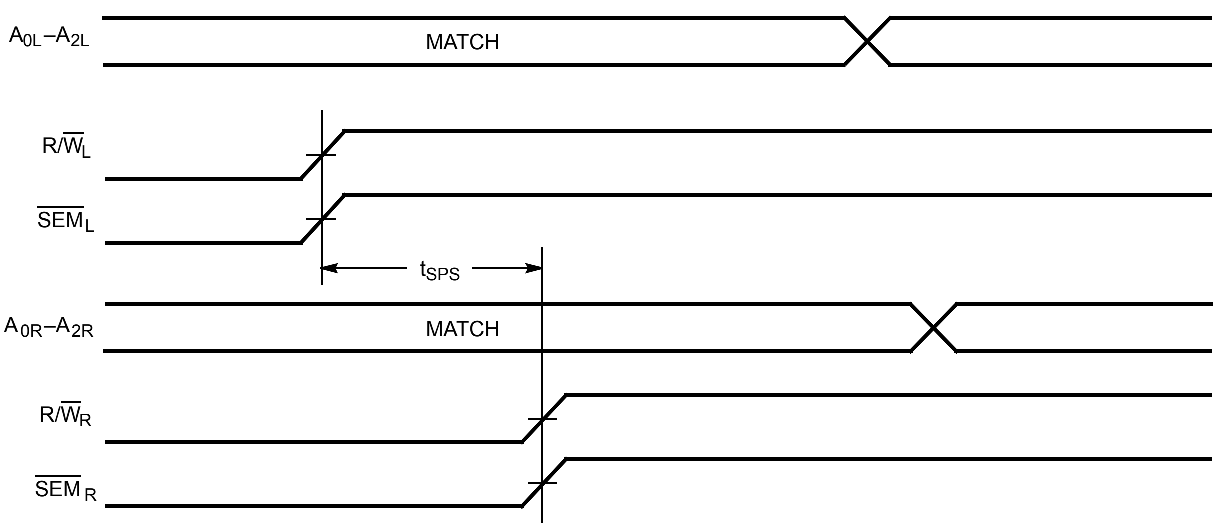


Figure 10. Timing Diagram of Semaphore Contention [42, 43, 44]



Notes

41. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
42. $IO_{0R} = IO_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
43. Semaphores are reset (available to both ports) at cycle start.
44. If t_{SPS} is violated, the semaphore is definitely obtained by one side or the other, but which side gets the semaphore is unpredictable.

Switching Waveforms (continued)

Figure 11. Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$ = HIGH) [45]

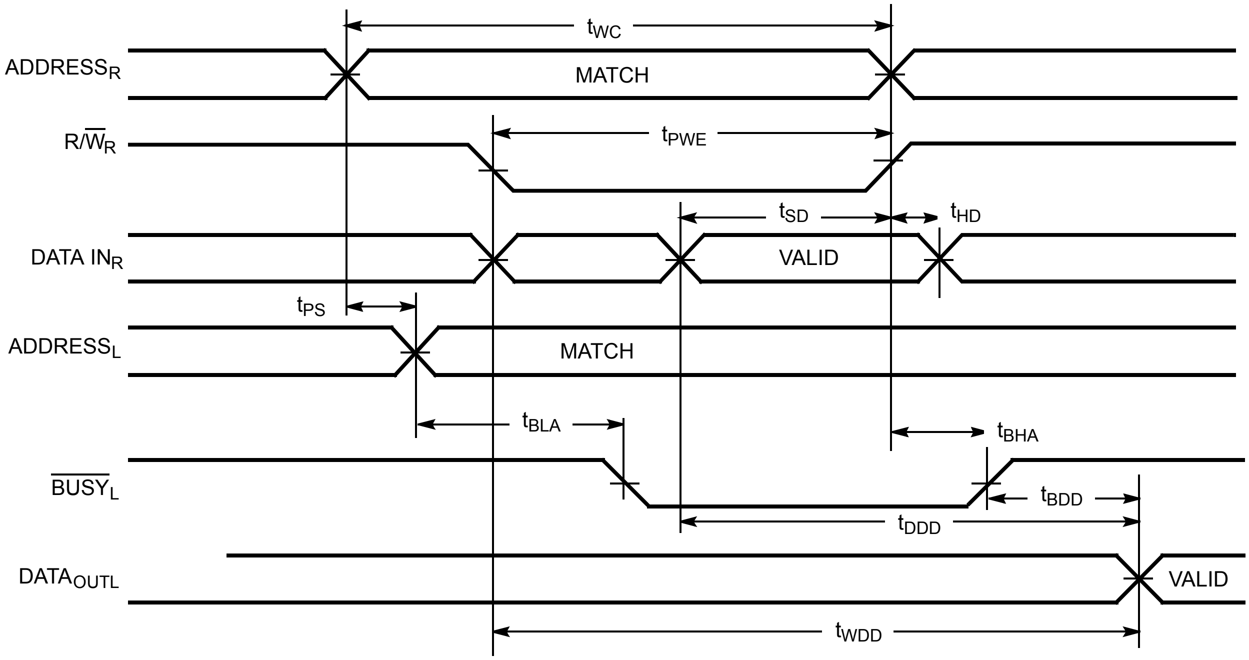
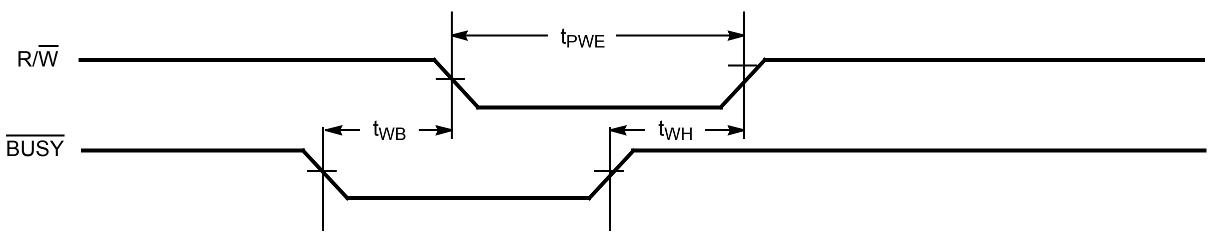


Figure 12. Write Timing with Busy Input (M/$\overline{S}$ = LOW)



Note
45. $\overline{CE}_L = \overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Figure 13. Busy Timing Diagram No.1 ($\overline{CE}$ Arbitration) [46]

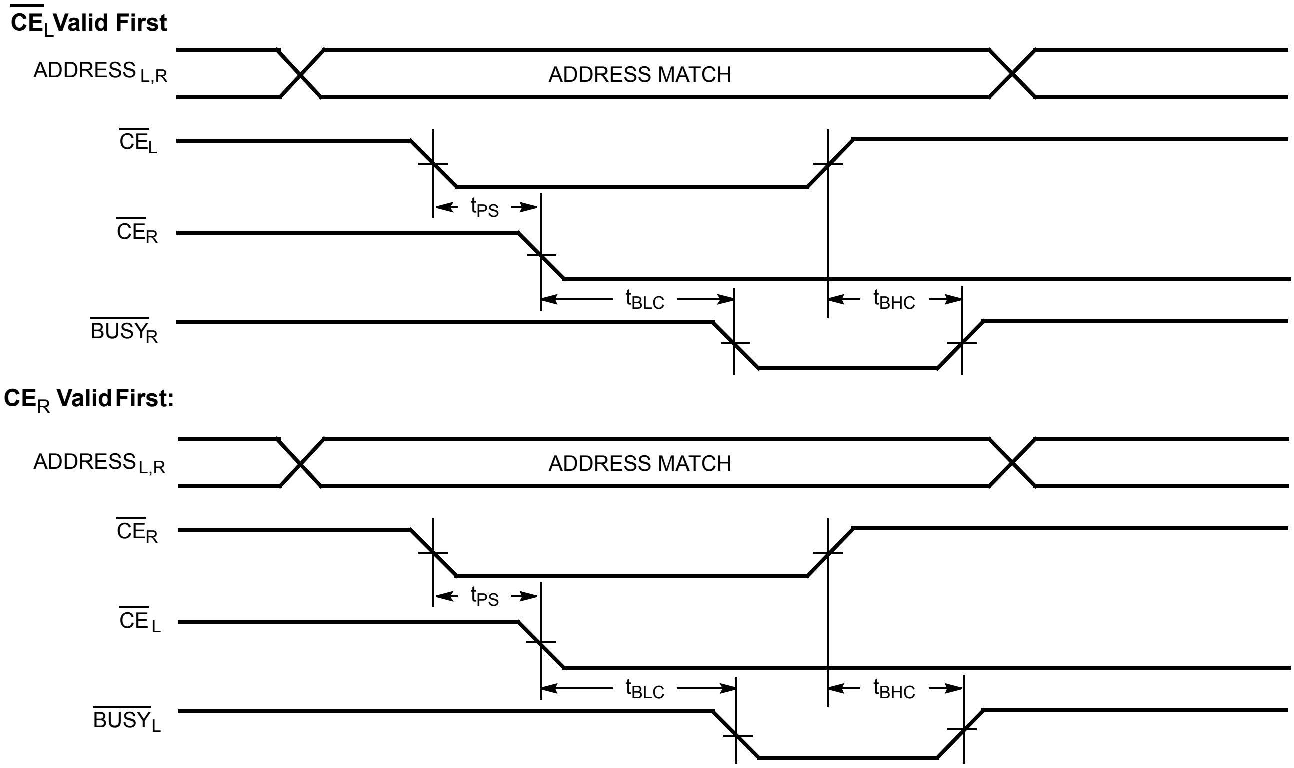
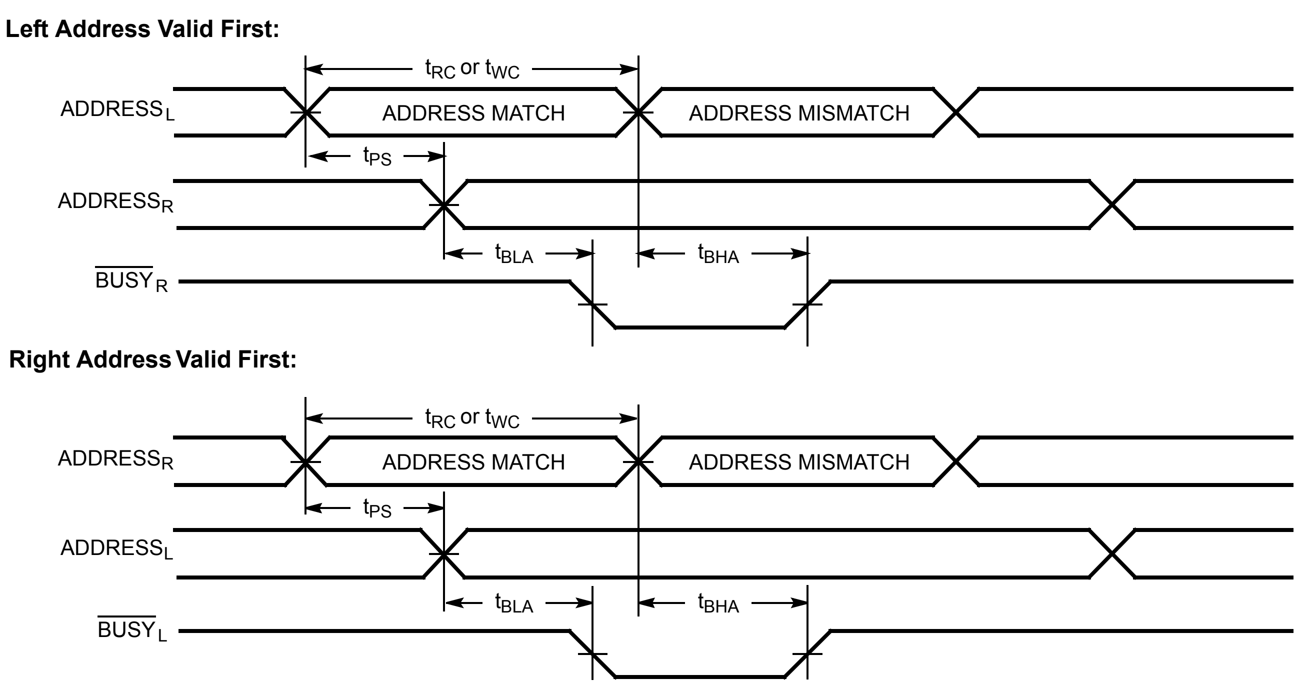


Figure 14. Busy Timing Diagram No.2 (Address Arbitration) [46]

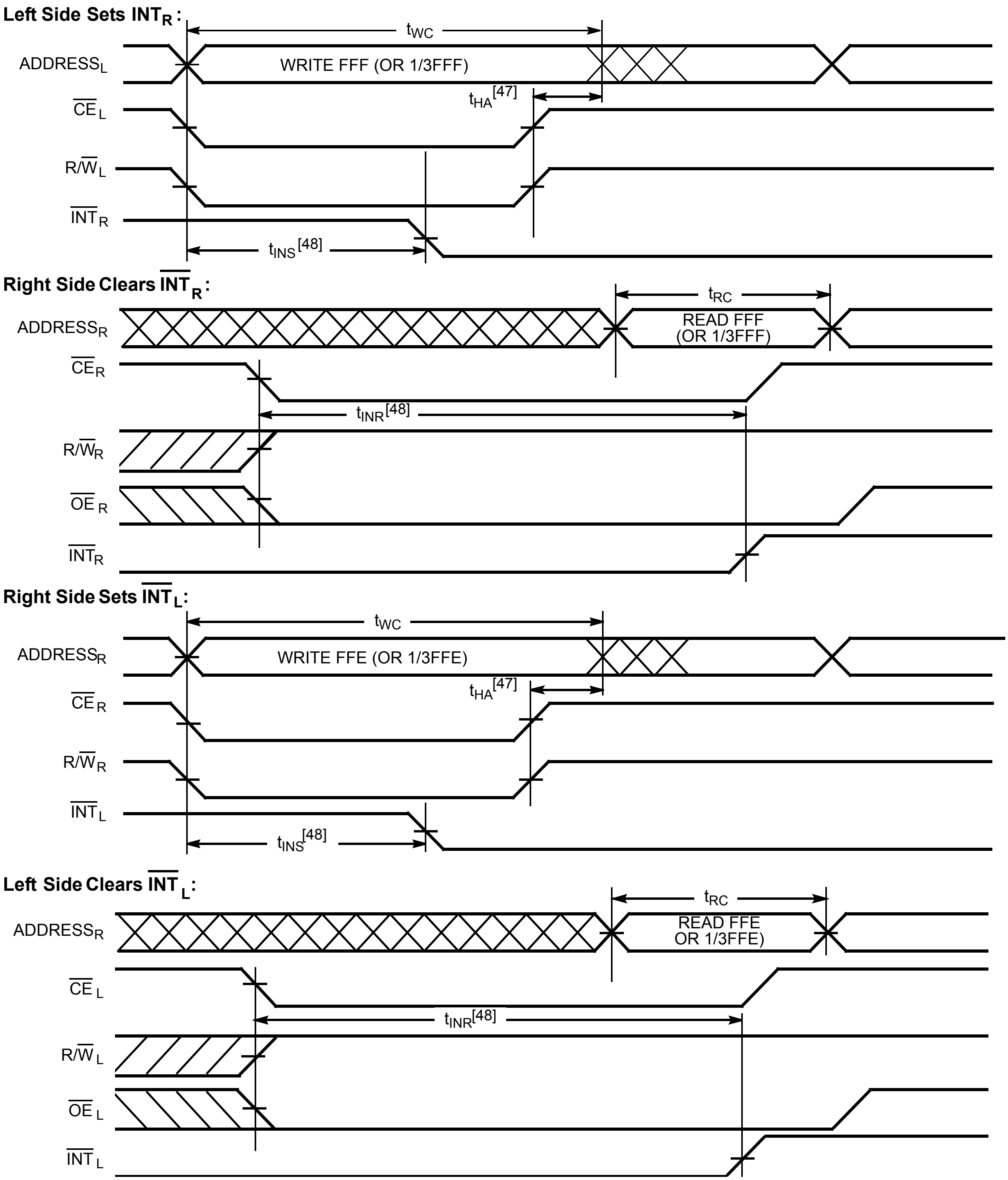


Note

46. If t_{PS} is violated, the busy signal is asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ is asserted.

Switching Waveforms (continued)

Figure 15. Interrupt Timing Diagram



Notes

47. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
48. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Ordering Information

4 K × 16 3.3 V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C024BV-15AXI	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Industrial
20	CY7C024AV-20AXC	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Commercial
	CY7C024AV-20AXI	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Industrial
25	CY7C024AV-25AXC	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Commercial
	CY7C024AV-25AXI	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Industrial

8 K × 16 3.3 V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY7C025AV-20AXC	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Commercial
25	CY7C025AV-25AXC	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Commercial
	CY7C025AV-25AXI	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Industrial

16 K × 16 3.3 V Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY7C026AV-20AXC	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	Commercial
25	CY7C026AV-25AC	51-85048	100-pin Thin Quad Flat Pack	Commercial
	CY7C026AV-25AXC	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	
	CY7C026AV-25AI	51-85048	100-pin Thin Quad Flat Pack	Industrial
	CY7C026AV-25AXI	51-85048	100-pin Thin Quad Flat Pack (Pb-free)	

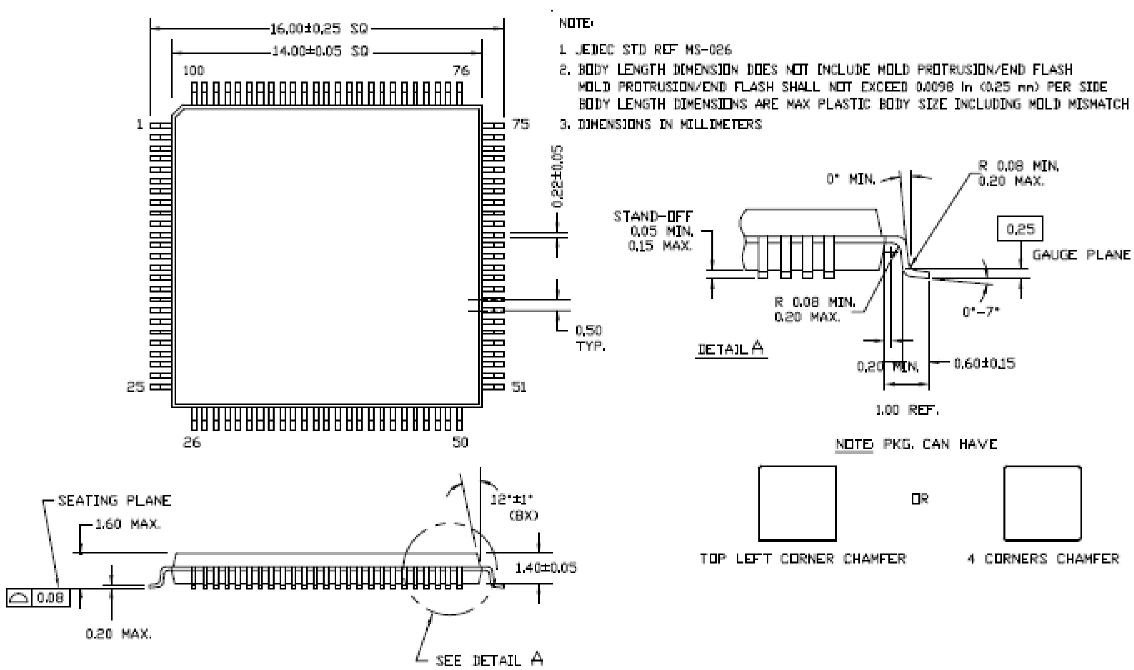
Ordering Code Definitions

CY 7 C 02 X XX - XX X X X

- Temperature Range: X = C or I
  C = Commercial; I = Industrial
- X = Pb-free (RoHS Compliant)
- Package Type:
  A = 100-pin TQFP
- Speed Grade: XX = 15 ns or 20 ns or 25 ns
- XX = AV/BV = 3.3 V
- Depth: X = 4 or 5 or 6
  4 = 4K; 5 = 8K; 6 = 16K
- 02 = Width: × 16
- Technology Code: C = CMOS
- Marketing Code: 7 = Dual Port SRAM
- Company ID: CY = Cypress

Package Diagram

Figure 16. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA



51-85048 *E

 [+] Feedback

Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
TTL	transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
µA	micro Amperes
mA	milli Amperes
mm	milli meter
mV	milli Volts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
V	Volts

Document History Page

Document Title: CY7C024AV/024BV/025AV/026AV, 3.3 V 4 K / 8 K / 16 K × 16 Dual-Port Static RAM Document Number: 38-06052				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110204	SZV	11/11/01	Change from Spec number: 38-00838 to 38-06052
*A	122302	RBI	12/27/02	Power up requirements added to Maximum Ratings Information
*B	128958	JFU	9/03/03	Added CY7C025AV-25AI to Ordering Information
*C	237622	YDT	See ECN	Removed cross information from features section
*D	241968	WWZ	See ECN	Added CY7C024AV-25AI to Ordering Information
*E	276451	SPN	See ECN	Corrected x18 for 026AV to x16
*F	279452	RUY	See ECN	Added Pb-free packaging information Corrected pin A113L to A13L on CY7C026AV pin list Added minimum V_{IL} of 0.3V and note 16
*G	373580	RUY	See ECN	Corrected CY7C024AC-25AXC to CY7C024AV-25AXC in Ordering Information
*H	380476	PCX	See ECN	Added to Part Ordering information: CY7C024AV-15AI, CY7C024AV-15AXI, CY7C024AV-20AI, CY7C024AV-20AXI, CY7C025AV-20AXI, CY7C026AV-20AXI
*I	2543577	NXR / AESA	07/25/08	Updated note number 33 on page 12 from “R/W must be HIGH during all address transitions” to “R/W or CE must be HIGH during all address transitions”
*J	2623540	VKN / PYRS	12/17/08	Added CY7C024BV part
*K	2896038	RAME	03/19/10	Removed inactive parts from ordering information table Updated package diagram
*L	3110406	ADMU	12/14/2010	Added Ordering Code Definitions.
*M	3210221	ADMU	03/30/2011	Updated Package Diagram from *D to *E Part CY7C025AV-25AC from Ordering Information table.
*N	3343888	ADMU	08/12/2011	Updated Document Title to read as “CY7C024AV/024BV/025AV/026AV, 3.3 V 4 K / 8 K / 16 K × 16 Dual-Port Static RAM”. Updated Features (Removed CY7C0241/251 and CY7C036 information). Updated Pin Configurations (Removed CY7C0241/251 and CY7C036 information). Updated Selection Guide (Removed CY7C0241/251 and CY7C036 information). Updated Pin Definitions. Updated Architecture (Removed CY7C0241/251 and CY7C036 information). Updated Functional Description (Removed CY7C0241/251 and CY7C036 information). Updated Electrical Characteristics (Removed CY7C0241/251 and CY7C036 information). Updated Switching Characteristics (Removed CY7C0241/251 and CY7C036 information). Added Acronyms and Units of Measure. Updated in new template.

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