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THIS SPEC IS OBSOLETE

Spec No: 38-05475

Spec Title: CY7C1049DV33, 4-MBIT (512K X 8) STATIC RAM

Replaced by: None

CY7C1049DV33

4-Mbit (512K × 8) Static RAM

Features

- Pin and function compatible with CY7C1049CV33
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 90 mA at 10 ns
- Low CMOS standby power
  - I_{SB2} = 10 mA
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 36-pin (400 Mil) molded SOJ and 44-pin TSOP II packages

Functional Description

The CY7C1049DV33 is a high performance CMOS Static RAM organized as 512K words by 8-bits. Easy memory expansion is provided by an Active LOW Chip Enable ($\overline{CE}$), an Active LOW Output Enable ($\overline{OE}$), and tristate drivers. You can write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (IO_0 through IO_7) is then written into the location specified on the address pins (A_0 through A_{18}).

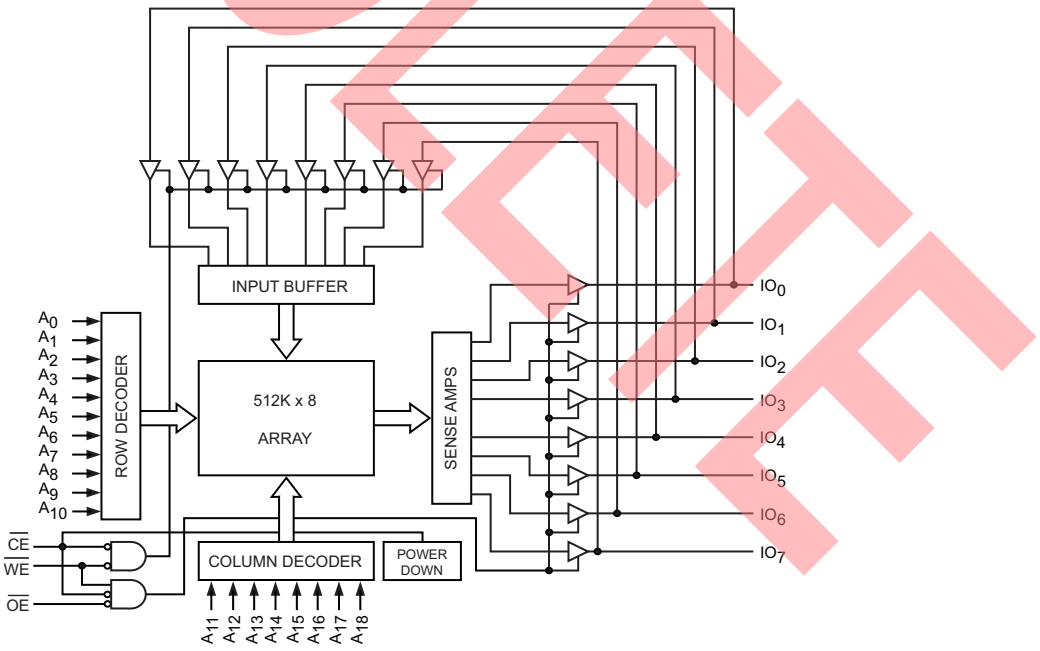
You can read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input or output pins (IO_0 through IO_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1049DV33 is available in standard 400 Mil wide 36 -pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

For a complete list of related documentation, click here.

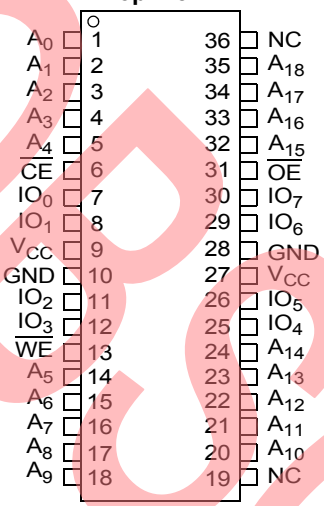
Logic Block Diagram



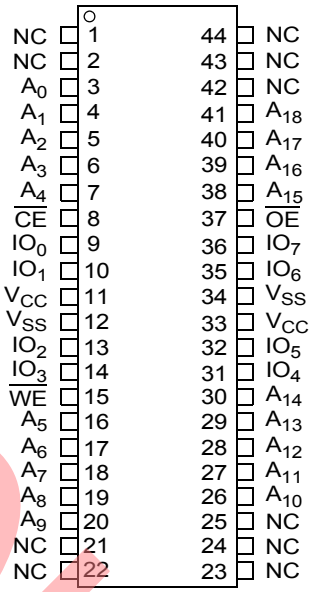
Contents

Pin Configuration

36-pin SOJ
Top View



44-pin TSOP II
Top View



Selection Guide

Description	-10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	90	mA
Maximum CMOS standby current	10	mA

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[1] .....–0.3 V to +4.6 V

DC voltage applied to outputs in High Z State[1] .....–0.3 V to V_{CC} + 0.3 V

DC input voltage[1] .....–0.3 V to V_{CC} + 0.3 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V (MIL-STD-883, Method 3015)

Latch up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V	10 ns

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10 (Industrial) Min	-10 (Industrial) Max	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		–	0.4	V
V_{IH}[1]	Input HIGH voltage			2.0	V_{CC} + 0.3	V
V_{IL}[1]	Input LOW voltage[1]			–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$	100 MHz	–	90	mA
			83 MHz	–	80	mA
			66 MHz	–	70	mA
			40 MHz	–	60	mA
I_{SB1}	Automatic CE Power down current —TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}; V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	20	mA
I_{SB2}	Automatic CE Power down current —CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0		–	10	mA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	I/O capacitance		8	pF

Note
1. V_{IL} (min.) = –2.0 V and V_{IH}(max) = V_{CC} + 2 V for pulse durations of less than 20 ns.

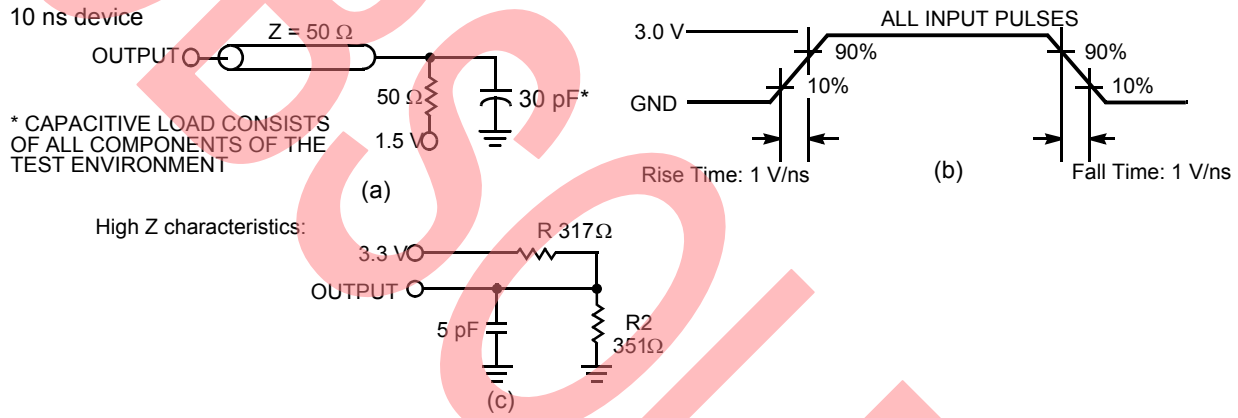
Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	36-pin SOJ Package	44-pin TSOP II Package	Unit
Θ_{JA}	Thermal resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two layer printed circuit board	57.91	50.66	°C/W
Θ_{JC}	Thermal resistance (Junction to Case)		36.73	17.17	°C/W

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms [4]

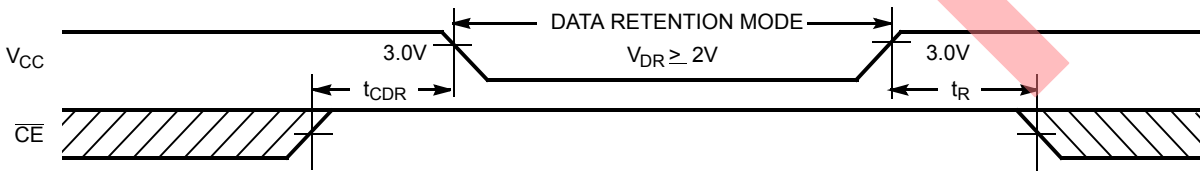


Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions [4]	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	10	mA
t_{CDR} [2]	Chip deselect to data retention time		0	–	ns
t_R [5]	Operation recovery time		t_{RC}	–	ns

Figure 2. Data Retention Waveform



Notes

2. Tested initially and after any design or process changes that may affect these parameters.
3. AC characteristics (except High Z) are tested using the load conditions shown in Figure 1 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 1 (c).
4. No input may exceed V_{CC} + 0.3 V.
5. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ µs or stable at $V_{CC(min.)} \geq 50$ µs.

AC Switching Characteristics

Over the Operating Range [6]

Parameter	Description	-10 (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{power}[7]	V_{CC} (typical) to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8, 9]	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]	–	5	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	10	ns
Write Cycle[10, 11]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7	–	ns
t_{AW}	Address setup to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data setup to write end	5	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]	–	5	ns

Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
7. t_{POWER} gives the minimum amount of time that the power supply must be at stable, typical V_{CC} values until the first memory access is performed.
8. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 1 on page 5. Transition is measured when the outputs enter a high impedance state.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set up and hold timing must be referred to the leading edge of the signal that terminates the write.
11. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 3. Read Cycle No. 1[12, 13]

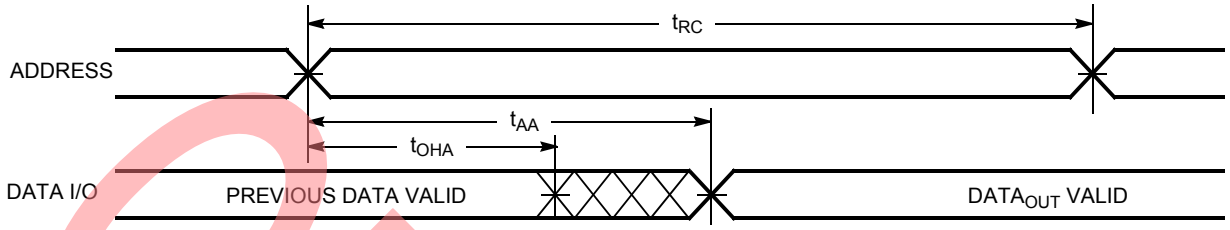


Figure 4. Read Cycle No. 2 (OE Controlled)[13, 14]

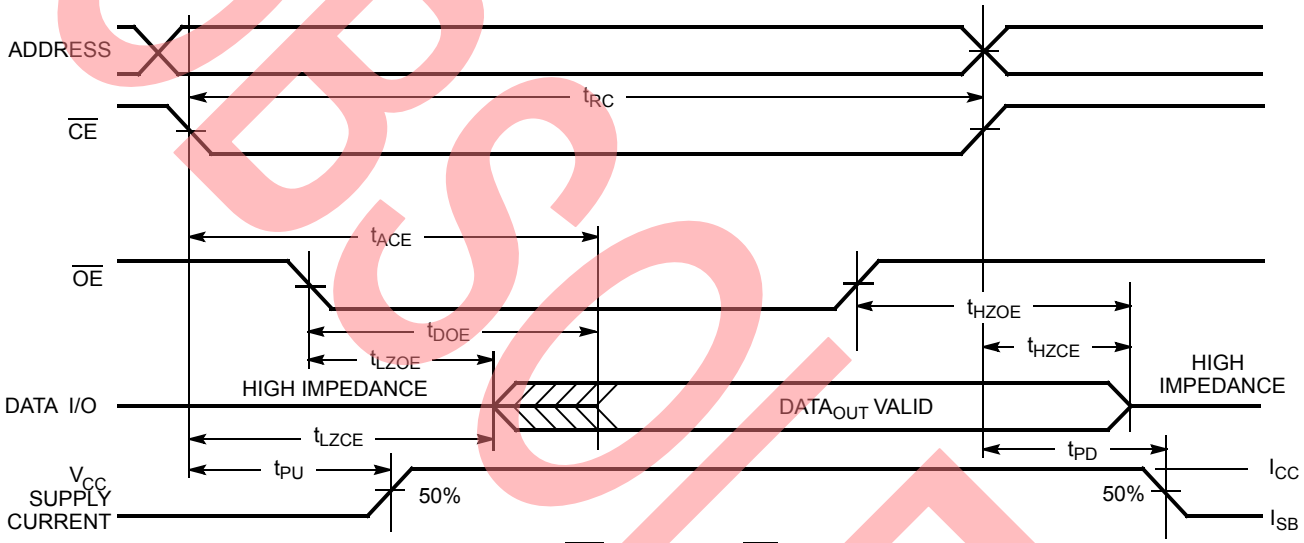
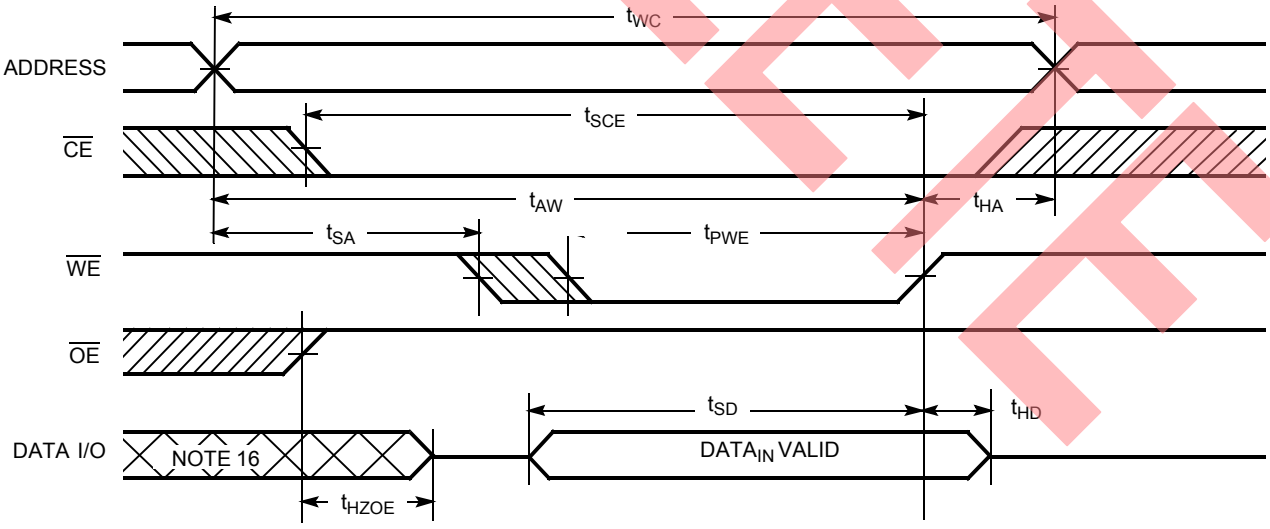


Figure 5. Write Cycle No. 1 (WE Controlled, OE HIGH During Write)[15, 16]



Notes
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[17]

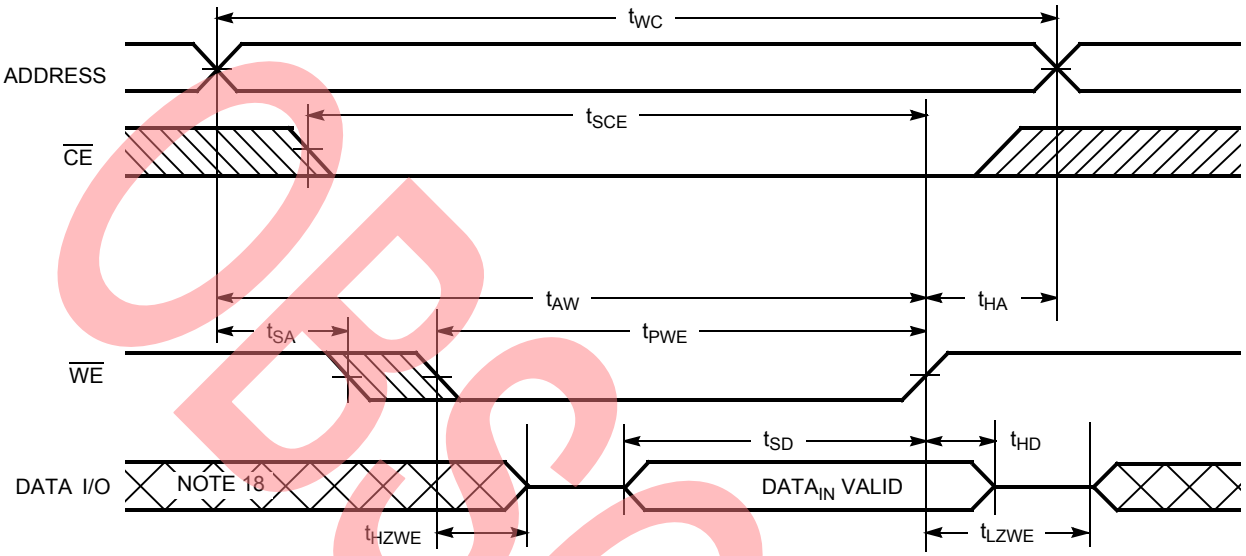
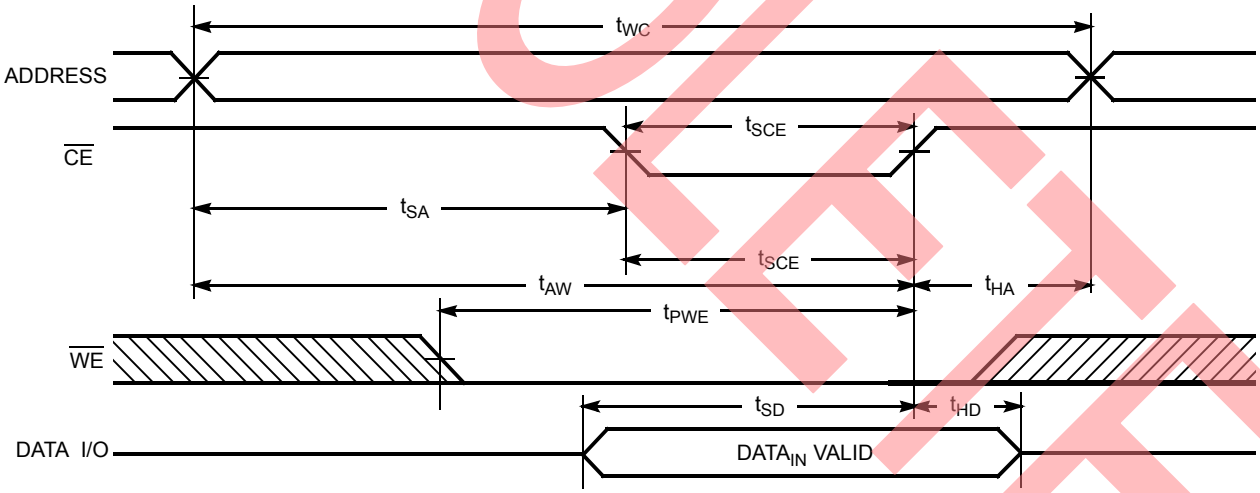


Figure 7. Write Cycle No. 3 ($\overline{CE}$ Controlled)[17, 19]



Notes
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
18. During this period the I/Os are in the output state and input signals must not be applied.
19. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	IO_0–IO_7	Mode	Power
H	X	X	High Z	Power down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1049DV33-10VXI	51-85090	36-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1049DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

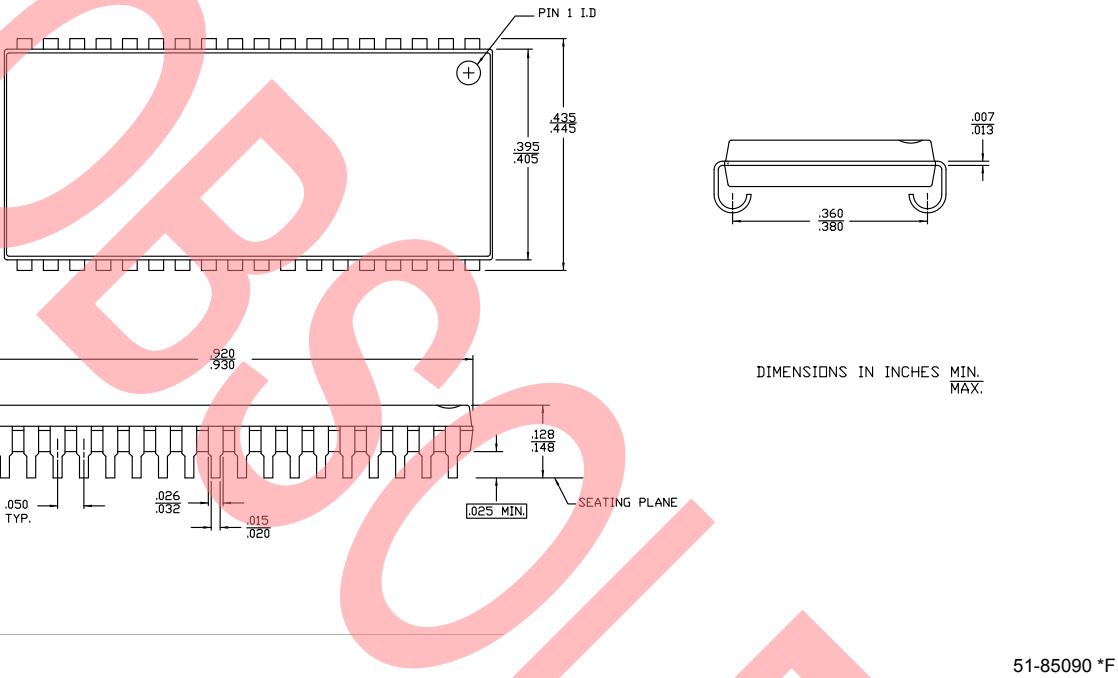
Ordering Code Definitions

CY 7 C 1 04 9 D V33 - XX XX X X

- Temperature Range: X = I
  I = Industrial
- Pb-free
- Package Type: XX = V or ZS
  V = 36-pin (400-Mil) Molded SOJ
  ZS = 44-pin TSOP II
- Speed: XX = 10 ns
- V33 = Voltage range (3 V to 3.6 V)
- D = C9, 90 nm Technology
- 9 = Data width × 8-bits
- 04 = 4-Mbit density
- 1 = Fast Asynchronous SRAM family
- Technology Code: C = CMOS
- 7 = SRAM
- CY = Cypress

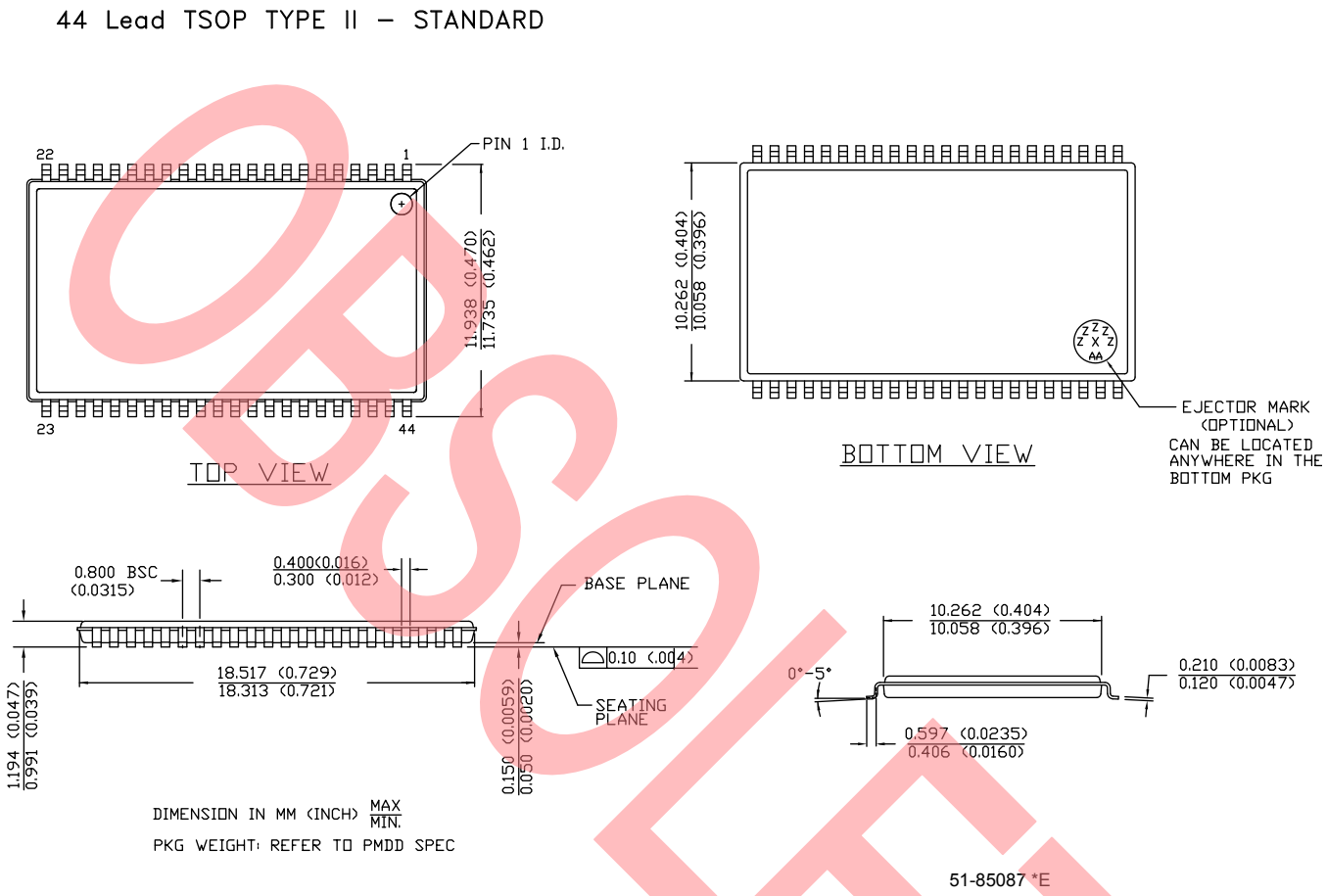
Package Diagrams

Figure 8. 36-pin (400-Mil) Molded SOJ V36.4, (51-85090)



Package Diagrams (continued)

Figure 9. 44-pin TSOP Z44-II, (51-85087)



Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celcius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeter
ms	milliseconds
ns	nanoseconds
Ω	ohms
%	percent
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY7C1049DV33, 4-Mbit (512K × 8) Static RAM Document Number: 38-05475				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Datasheet for C9 IPP
*A	233729	See ECN	SYT	1.AC, DC parameters are modified as per EROS (Specification # 01-2165) 2.Pb-free offering in the Ordering Information Table
*B	351096	See ECN	PCI	Changed status from Advance to Preliminary. Removed 20 ns Speed bin Corrected DC voltage (min) value in maximum ratings section from - 0.5 to - 0.3V Redefined I_{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 100, 80, and 67 mA to 90, 80 and, 75 mA for 8, 10, and 12ns speed bins respectively I_{CC} (Ind'l): Changed from 80 and 67 mA to 90 and 85 mA for 10 and 12ns speed bins respectively Added $V_{IH(max)}$ specification in Note# 2 Changed reference voltage level for measurement of High Z parameters from ±500 mV to ±200 mV Added Data Retention Characteristics, Waveform, and footnotes 11 and 12 Changed Package Diagram name from 44-pin TSOP II Z44 to 44-pin TSOP II ZS44 Changed part names from Z to ZS in the Ordering Information Table Added 8 ns parts in the Ordering Information Table Added Pb-free Ordering Information Shaded Ordering Information Table
*C	446328	See ECN	NXR	Changed status from Preliminary to Final. Removed -8 speed bin Removed Commercial Operating Range product information Added Automotive Operating Range product information Updated Thermal Resistance table Updated footnote #8 on High Z parameter measurement Replaced Package Name column with Package Diagram in the Ordering Information table
*D	1274726	See ECN	VKN/AESA	Updated Pin Configuration. Corrected typo in the 44-pin TSOP II pinout.
*E	2899972	03/29/2010	AJU	Updated Package Diagrams.
*F	3059162	10/14/2010	PRAS	Added Ordering Code Definitions. Updated Package Diagrams.
*G	3266084	05/28/2011	PRAS	Updated Functional Description (Removed "Refer to the Cypress application note AN1064, SRAM System Guidelines for best practice recommendations."). Added Acronyms and Units of Measure. Updated to new template.
*H	3440302	11/16/2011	TAVA	Removed Automotive Temperature Range related information in all instances across the document. Updated Switching Waveforms. Updated Ordering Information: Updated part numbers.
*I	4574311	11/19/2014	TAVA	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Package Diagrams: spec 51-85090 – Changed revision from *E to *F.
*J	5544150	12/06/2016	VINI	Obsolete document. Completing Sunset Review.

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