4-Mbit (256K words × 16 bit) Static RAM

Features

- High speed: 45 ns/55 ns
- Ultra-low standby power
  - Typical standby current: 3.5 µA
  - Maximum standby current: 8.7 µA
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

CY62147GN and CY621472GN are high-performance CMOS low-power (MoBL) SRAM devices organized as 256K Words by 16-bits. Both devices are offered in single and dual chip enable options and in multiple pin configurations.

Devices with a single chip enable input are accessed by asserting the chip enable ($\overline{CE}$) input LOW. Dual chip enable devices are accessed by asserting both chip enable inputs – $\overline{CE}_1$ as low and CE_2 as HIGH.

Data writes are performed by asserting the Write Enable ($\overline{WE}$) input LOW, while providing the data on I/O_0 through I/O_{15} and address on A_0 through A_{17} pins. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control write operations to the upper and lower bytes of the specified memory location. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_{15}). Byte accesses can be performed by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a HI-Z state when the device is deselected ($\overline{CE}$ HIGH for a single chip enable device and $\overline{CE}_1$ HIGH/CE_2 LOW for a dual chip enable device), or control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

The device also has a unique Byte Power down feature, where, if both the Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) are disabled, the devices seamlessly switch to standby mode irrespective of the state of the chip enables, thereby saving power.

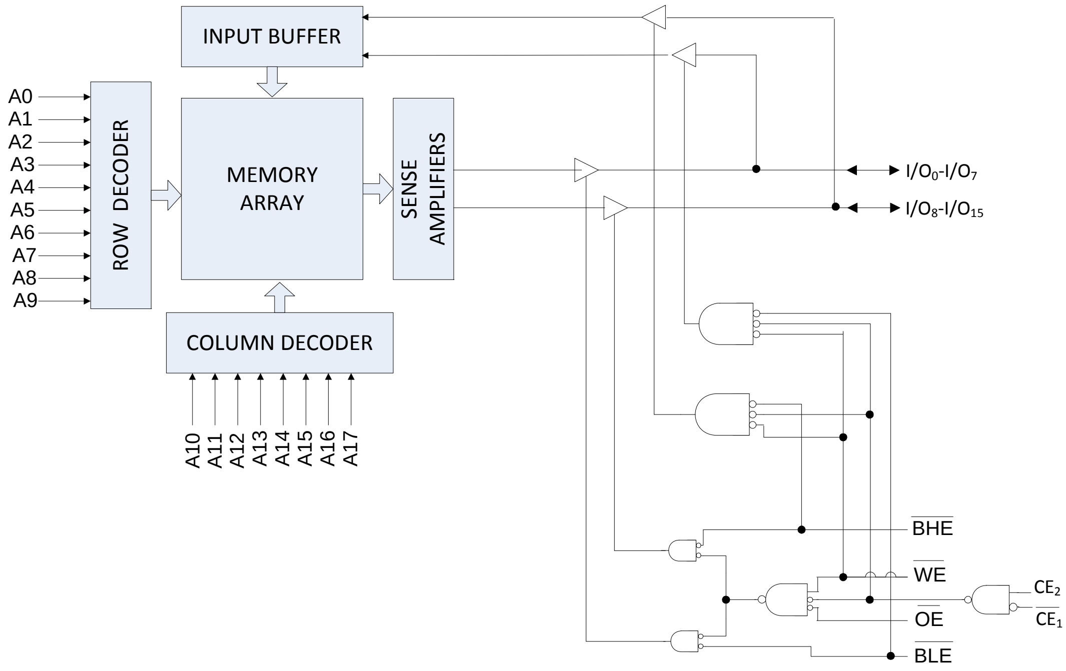
The logic block diagram is provided in page 2.

Product Portfolio

Product	Features and Options (see the Pin Configurations section)	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (µA)	
					Typ[1]	Max	Typ[1]	Max
CY62147GN18	Single or dual Chip Enables	Industrial	1.65 V–2.2 V	55	15	20	3.5	10
CY62147GN30 CY621472GN30			2.2 V–3.6 V	45	15	20	3.5	8.7
CY62147GN			4.5 V–5.5 V					

Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY62147GN



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Pin Configuration – CY62147GN

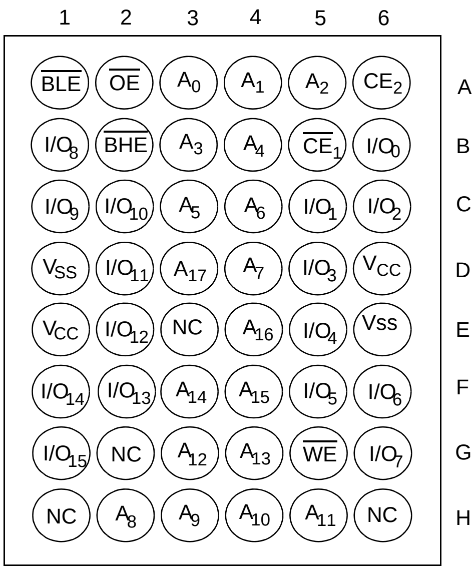


Figure 1. 48-ball VFBGA pinout (Dual Chip Enable), CY62147GN[2]

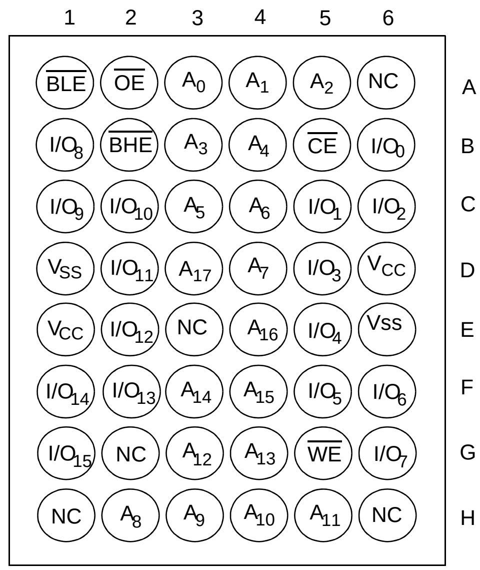
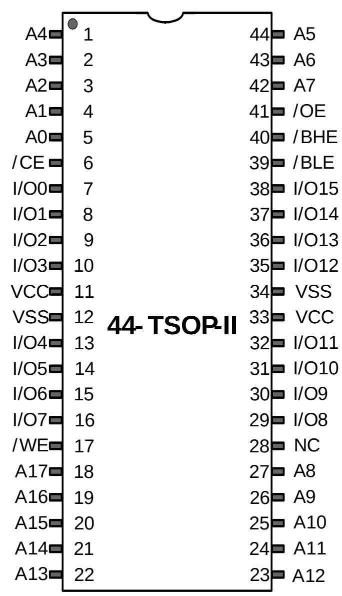


Figure 2. 48-ball VFBGA pinout (Single Chip Enable), CY62147GN[2]

Figure 3. 44-pin TSOP II Pinout (Single Chip Enable), CY62147GN[2]

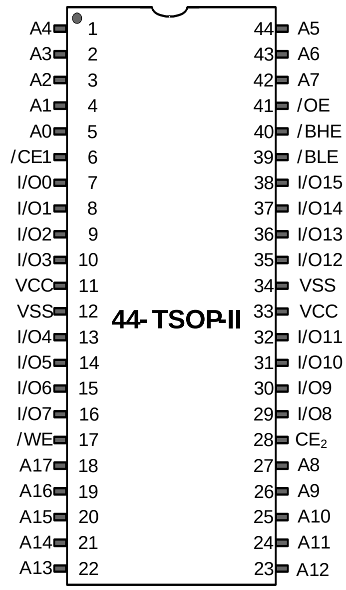


Notes

2. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configuration – CY621472GN

Figure 4. 44-pin TSOP II pinout (Dual Chip Enable), CY621472GN



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature with power applied .... –55 °C to + 125 °C

Supply voltage to ground potential[3] .... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs in HI-Z state[3] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage[3] .... –0.5 V to V_{CC} + 0.5 V

Output current into outputs (in low state) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... >2001 V

Latch-up current .... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions		45/55 ns Min	45/55 ns Typ	45/55 ns Max	Unit
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA		2	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA		V_{CC} – 0.5[4]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2[3]	V
		2.2 V to 2.7 V	–		1.8	–	V_{CC} + 0.3[3]	
		2.7 V to 3.6 V	–		2	–	V_{CC} + 0.3[3]	
		4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5[3]	
V_{IL}	Input LOW voltage	1.65 V to 2.2 V	–		–0.2[3]	–	0.4	V
		2.2 V to 2.7 V	–		–0.3[3]	–	0.6	
		2.7 V to 3.6 V	–		–0.3[3]	–	0.8	
		4.5 V to 5.5 V	–		–0.5[3]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current		Max V_{CC}, I_{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	–	15	20	mA
				f = 18.18 MHz (55 ns)	–	15	20	mA
				f = 1 MHz	–	3.5	6	mA

Notes

3. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
4. This parameter is guaranteed by design and not tested.

DC Electrical Characteristics (continued)

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions		45/55 ns			Unit
				Min	Typ	Max	
I_{SB1}[5]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), Max V_{CC}		–	3.5	8.7	µA
	Automatic power down current – CMOS inputs V_{CC} = 1.65 V to 2.2 V			–	–	10	
I_{SB2}[5]	Automatic power down current – CMOS inputs V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, Max V_{CC}	25 °C[6]	–	3.5	3.7	µA
			40 °C[6]	–	–	4.8	
			70 °C[6]	–	–	7	
			85 °C	–	–	8.7	
	Automatic power down current – CMOS inputs V_{CC} = 1.65 V to 2.2 V	$\overline{CE}_1 \geq V_{CC}$ – 0.2V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, Max V_{CC}	25 °C[6]	–	3.5	4.3	
			40 °C[6]	–	–	5	
			70 °C[6]	–	–	7.5	
			85 °C	–	–	10	

Notes
5. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
6. The I_{SB2} limits at 25 °C, 40 °C, 70 °C, and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

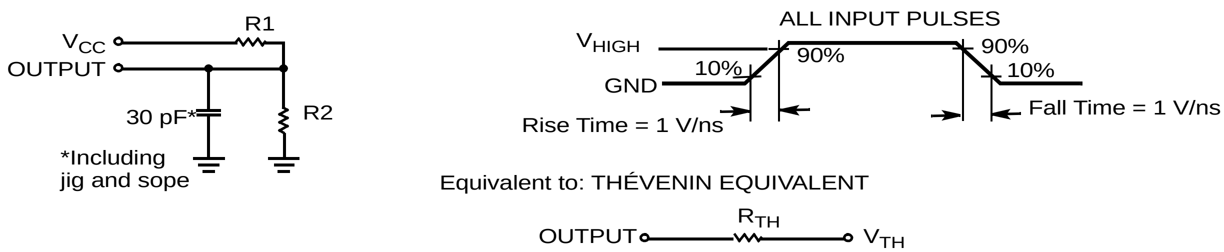
Parameter[7]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25$ °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter[7]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	31.35	68.85	°C/W
Θ_{JC}	Thermal resistance (junction to case)		14.74	15.97	°C/W

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms[8]



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V

Notes
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

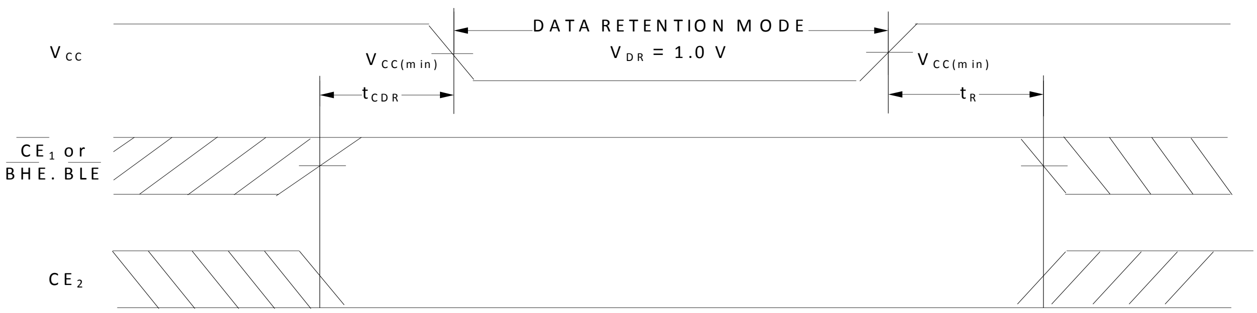
Data Retention Characteristics

Over the Operating range

Parameter	Description	Conditions	Min	Typ[9]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
I_{CCDR}[10, 11]	Data retention current	Vcc = 1.2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–		13	µA
t_{CDR}[12]	Chip deselect to data retention time		0	–	–	ns
t_R[13]	Operation recovery time		45/55	–	–	ns

Data Retention Waveform

Figure 6. Data Retention Waveform[14]



Notes

9. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
10. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR}.
12. These parameters are guaranteed by design.
13. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
14. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

AC Switching Characteristics

Parameter[15, 16]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
READ CYCLE						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low impedance[17]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to HI-Z[17, 18]	–	18	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low impedance[17]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to HI-Z[17, 18]	–	18	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	45	–	55	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	45	–	55	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low impedance[17]	5	–	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HI-Z[17, 18]	–	18	–	18	ns
WRITE CYCLE[19, 20]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	45	–	ns
t_{AW}	Address setup to write end	35	–	45	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	45	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to HI-Z[17, 18]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low impedance[17]	10	–	10	–	ns

Notes

15. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
16. These parameters are guaranteed by design.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$, or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
20. The minimum pulse width in Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 7. Read Cycle No. 1 of CY62147GN (Address Transition Controlled)[21, 22]

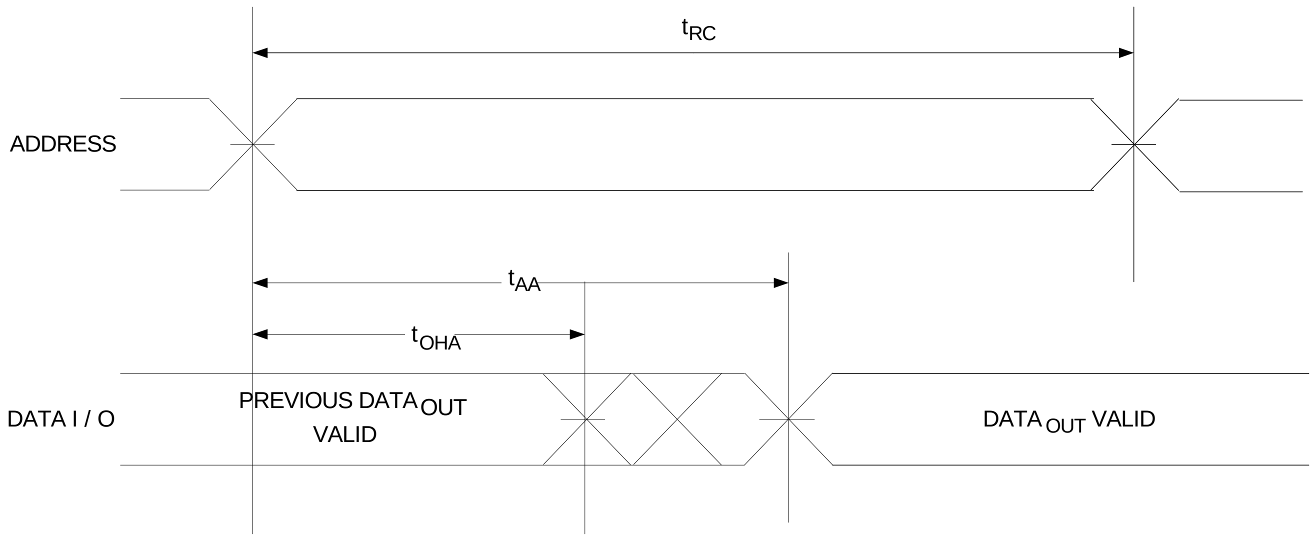
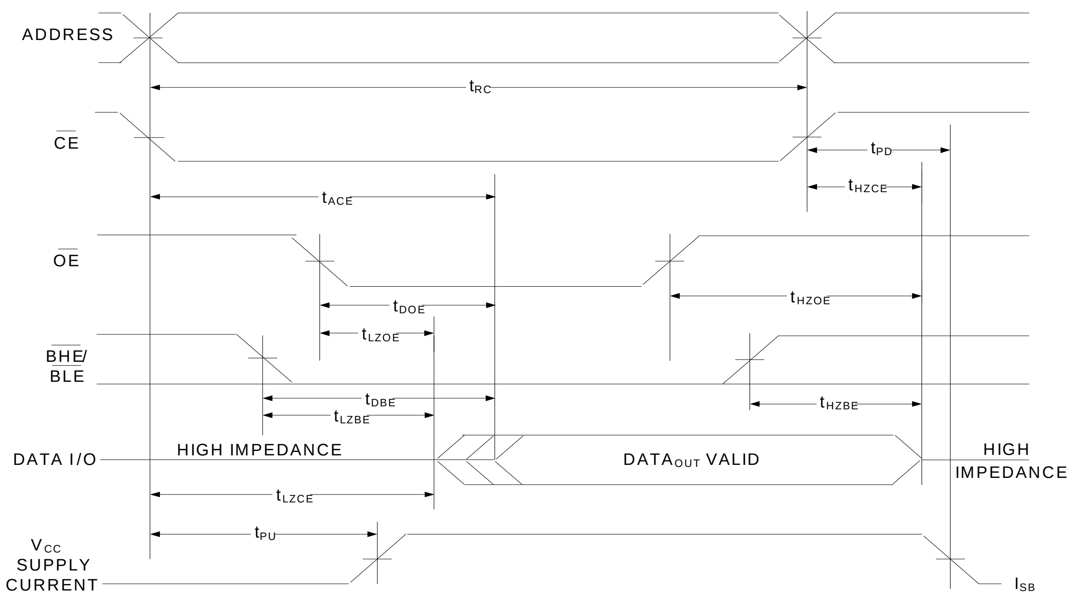


Figure 8. Read Cycle No. 2 ($\overline{OE}$ Controlled)[21, 22, 23, 24]

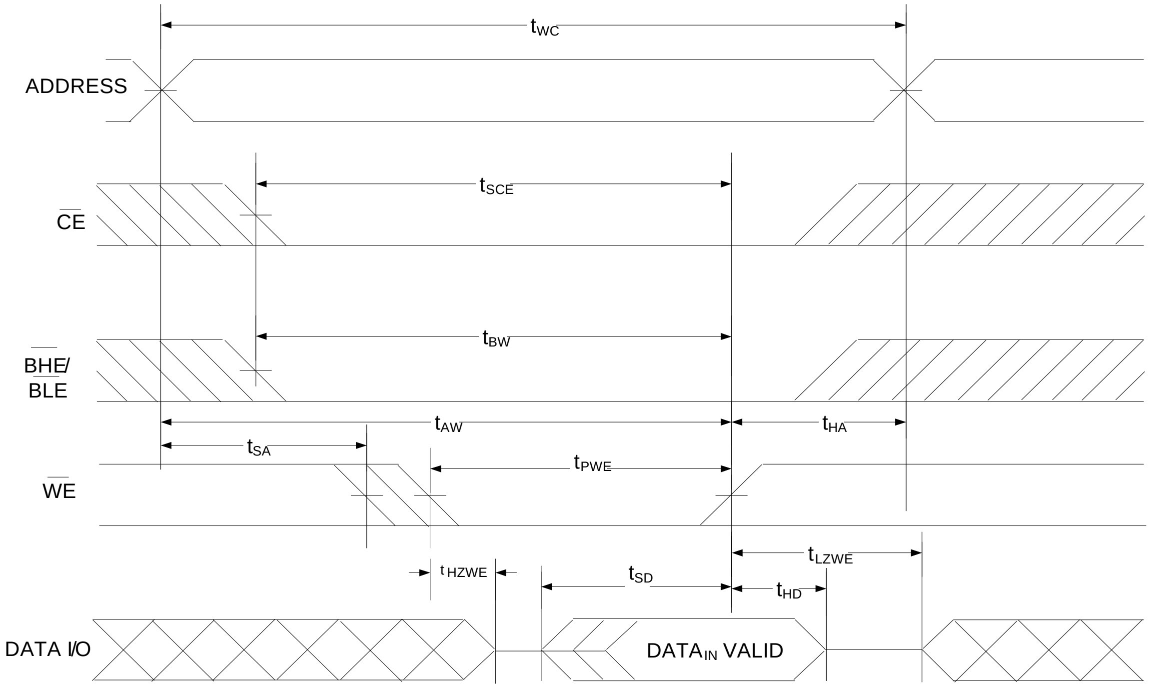


Notes

21. The device is continuously selected. $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
22. $\overline{WE}$ is HIGH for Read cycle.
23. Data I/O is in a HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
24. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 1 (WE Controlled)[25, 26, 27]



Notes

25. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
26. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
27. Data I/O is in a HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 2 ($\overline{CE}$ Controlled)[28, 29, 30]

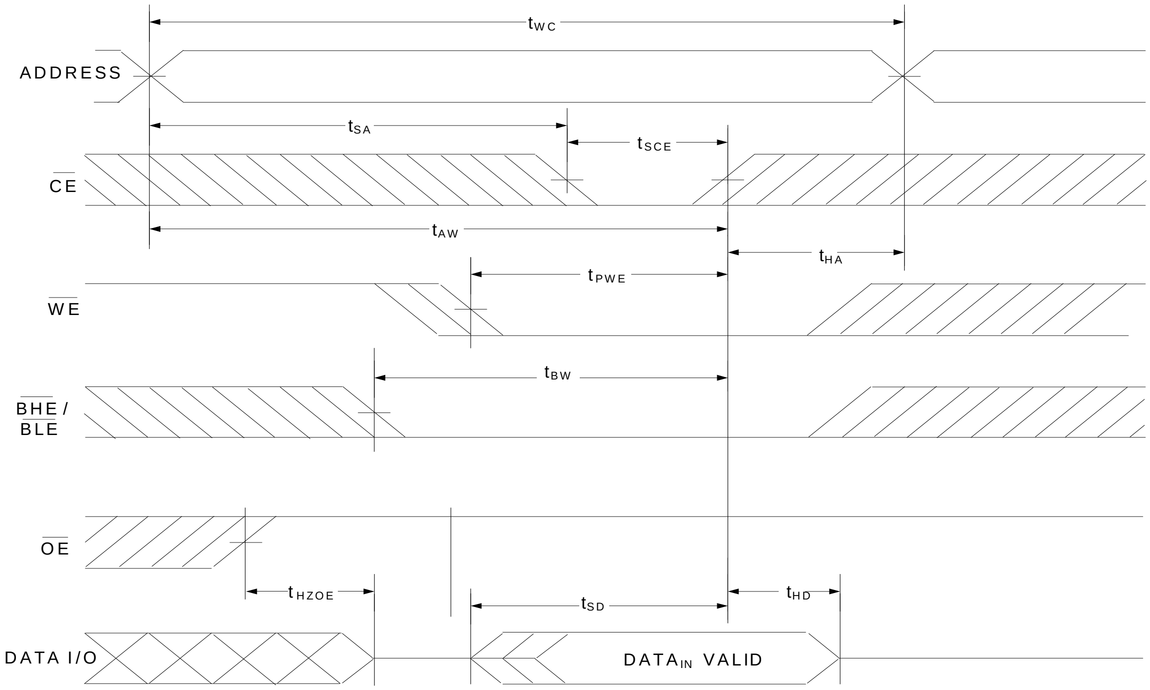
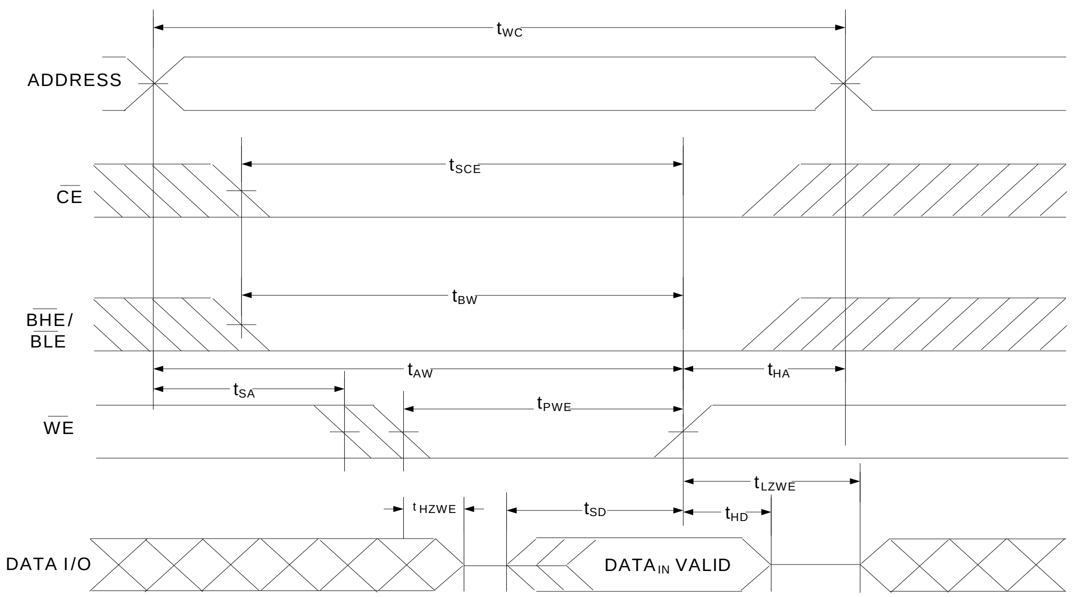


Figure 11. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[28, 29, 30, 31]



Notes

28. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
29. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
30. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
31. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

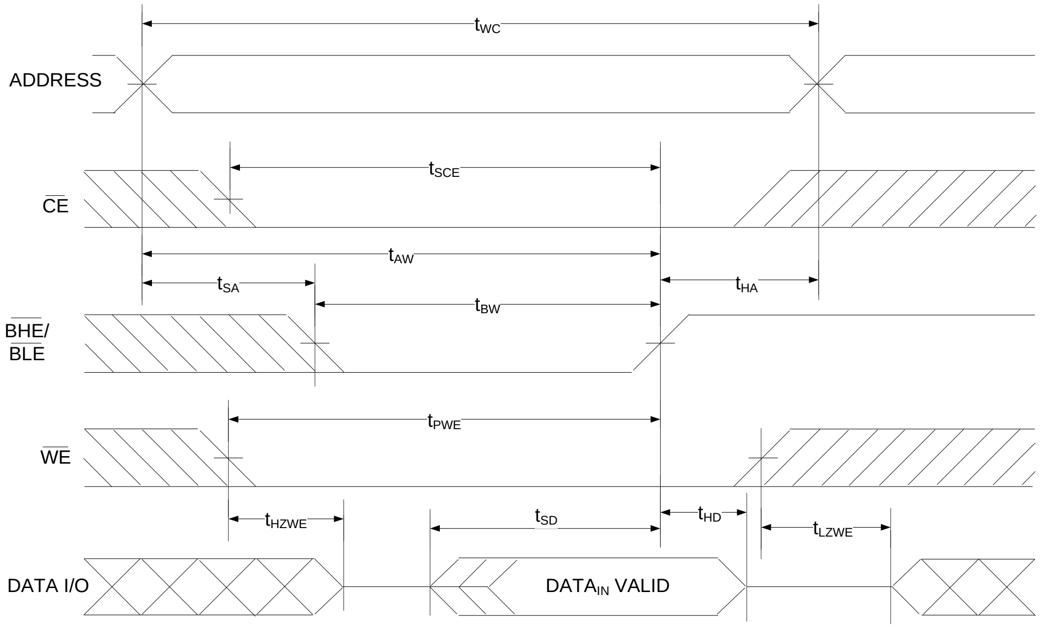


Figure 12. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled)[32, 33, 34]

Notes

32. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
33. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
34. Data I/O is in a HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

Truth Table – CY62147GN/CY621472GN

$\overline{CE_1}$/$\overline{CE}$[35]	CE_2[35]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[36]	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	X	H	H	HI-Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	HI-Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	HI-Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	HI-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	HI-Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	HI-Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Notes

35. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH
36. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62147GN30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Dual Chip Enable	Industrial
		CY62147GN30-45BVXIT	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Dual Chip Enable, Tape and Reel	
		CY62147GN30-45ZSXI	51-85087	44-pin TSOP II, Single Chip Enable	
		CY62147GN30-45ZSXIT	51-85087	44-pin TSOP II, Single Chip Enable, Tape and Reel	
		CY62147GN30-45B2XI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable	
		CY62147GN30-45B2XIT	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel	
		CY621472GN30-45ZSXI	51-85087	44-pin TSOP II, Dual Chip Enable	
		CY621472GN30-45ZSXIT	51-85087	44-pin TSOP II, Dual Chip Enable, Tape and Reel	
55	1.65 V–2.2 V	CY62147GN18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable	
		CY62147GN18-55BVXIT	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Single Chip Enable, Tape and Reel	

Ordering Code Definitions

CY 621 4 7 X GN XX - XX XX X X X

- X: T = Tape and Reel; Blank = Bulk
- Temperature Grade: X = I; I = Industrial
- Pb-free
- Package Type: XX = BV, B2 or ZS
  BV = 48-ball VFBGA (Dual Chip Enable);
  B2 = 48-ball VFBGA (Single Chip Enable)
  ZS = 44-pin TSOP II
- Speed Grade: XX = 45 ns or 55 ns
- Voltage Range: 30 = 3 V typ
- Process Technology: GN = 65 nm
- Chip Enable: X = blank or 2
  blank = Single Chip Enable; 2 = Dual Chip Enable
- Bus Width: 7 = × 16
- Density: 4 = 4-Mbit
- Family Code: 621 = MoBL SRAM family
- Company ID: CY = Cypress

Package Diagrams

Figure 13. 44-pin TSOP II (Z44) Package Outline, 51-85087

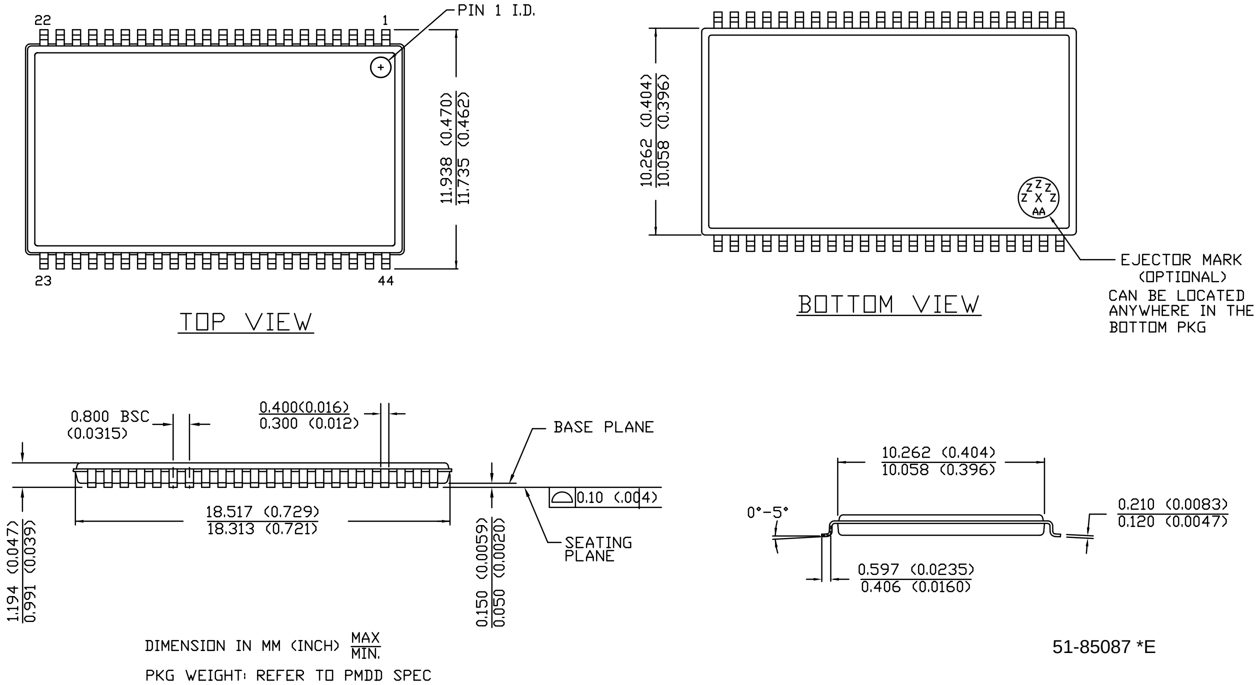
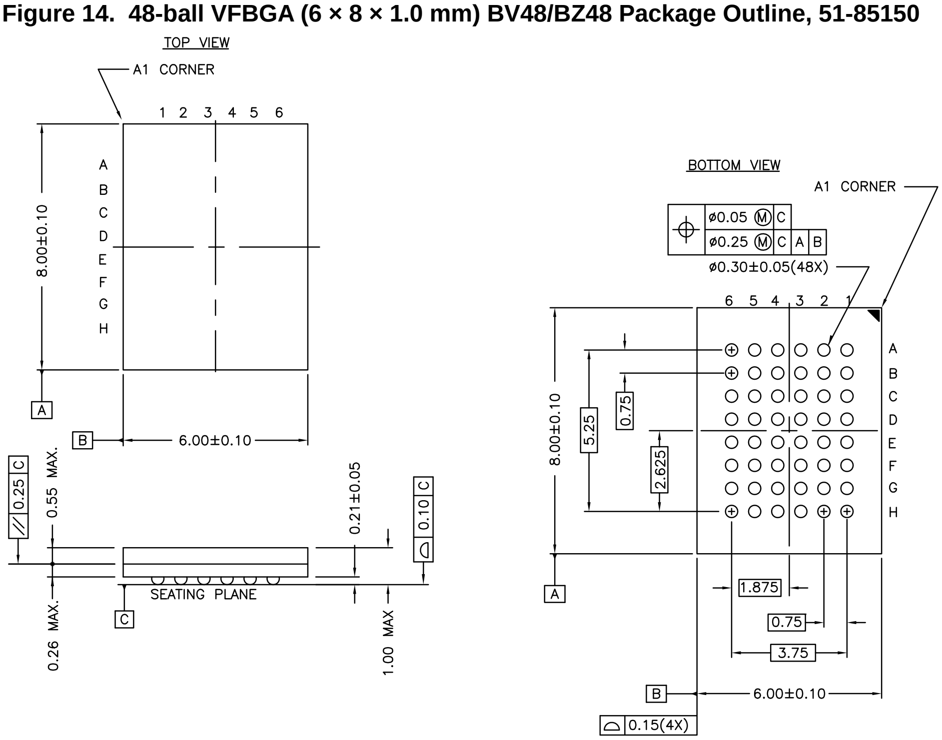


Figure 14. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY62147GN/CY621472GN MoBL®, 4-Mbit (256K words × 16 bit) Static RAM Document Number: 002-10624				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5076421	NILE	01/07/2016	New data sheet.
*A	5084145	NILE	01/13/2016	Updated Logic Block Diagram – CY62147GN.
*B	5329364	VINI	06/29/2016	Updated Ordering Information: Updated part numbers. Updated to new template.
*C	5429186	NILE	09/07/2016	Updated DC Electrical Characteristics: Enhanced VIH of 2.2V - 2.7V operating range from 2.0V to 1.8V. Enhanced VOH of 2.7V - 3.6V operating range from 2.2V to 2.4V. Updated Ordering Information: Updated part numbers. Updated Note 3. Updated Copyright and Disclaimer.
*D	6002285	AESATP12	12/21/2017	Updated logo and copyright.

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