Fixed-frequency 800 V / 950 V CoolSET™
in DIP-7 package

Features

- Integrated 800 V / 950 V avalanche rugged CoolMOS™
- Enhanced Active Burst mode with selectable entry and exit standby power
- Digital frequency reduction for better overall system efficiency
- Fast startup achieved with cascode configuration
- DCM and CCM operation with slope compensation
- Frequency jitter and soft gate driving for low EMI
- Built-in digital soft start
- Integrated error amplifier to support direct feedback in non-isolated flyback and buck topologies
- Comprehensive protection with input line overvoltage, V_{CC} overvoltage, V_{CC} undervoltage, overload, open loop and overtemperature
- All protections are in auto restart mode
- Limited charging current for V_{CC} short to GND
- Pb-free lead plating, halogen-free mold compound, RoHS-compliant

PG-DIP-7

Potential applications

- Auxiliary power supply for home appliances, white goods, TV, PC and server, smart metering
- Blu-ray players, set-top boxes, and LCD/LED monitors

Product validation

Fully qualified according to JEDEC for Industrial Applications.

Description

The ICE5xRxxxxxZ is the fifth-generation of fixed-frequency integrated power IC (CoolSET™) optimized for off-line switch-mode power supplies in cascode configuration. The CoolSET™ package contains two separate chips. One is the controller chip and the other is the 800 V / 950 V CoolMOS™ chip. The cascode configuration helps achieve fast startup. The frequency reduction with soft gate driving and frequency jitter operation offers lower EMI and better efficiency between a light load and 50% load. The selectable entry and exit standby power ABM enables flexibility and ultra-low power consumption in standby mode with small and controllable output voltage ripple. The product has a wide operating range (10.0 V to 25.5 V) of IC power supply and lower power consumption. The numerous protection functions support the power supply system in failure situations. All these make the fifth-generation CoolSET™ series an outstanding integrated power stage fixed frequency flyback and buck converter in the market.

Datasheet
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Figure 1 **Typical application in isolated flyback using TL431 and optocoupler**

Figure 2 **Typical application in non-isolated flyback utilizing integrated error amplifier**

*Rs is recommended to avoid saturation of inductor (L1) during output short circuit

Figure 3 **Typical application in non-isolated buck**

Output power of fifth-generation fixed-frequency CoolSET™ in flyback design

Table 1   Output power of fifth-generation fixed-frequency CoolSET™ in flyback design

Type	Package	Marking	V_{DS}	F_{sw}	R_{DSon}[1]	220 V AC ±20%[2] at DCM	85-300 V AC[2] at DCM	85-300 V AC[2] at CCM
ICE5BR4780BZ	PG-DIP-7	5BR4780BZ	800 V	65 kHz	4.13 Ω	27.5 W	15 W	16.5 W
ICE5BR3995BZ	PG-DIP-7	5BR3995BZ	950 V	65 kHz	3.46 Ω	30 W	16.5 W	18 W
ICE5BR3995CZ	PG-DIP-7	5BR3995CZ	950 V	65 kHz	3.46 Ω	30 W	16.5 W	18 W
ICE5AR3995BZ	PG-DIP-7	5AR3995BZ	950 V	100 kHz	3.46 Ω	30 W	16.5 W	18 W
ICE5BR2280BZ	PG-DIP-7	5BR2280BZ	800 V	65 kHz	2.13 Ω	40 W	22 W	24 W
ICE5AR2280CZ	PG-DIP-7	5AR2280CZ	800 V	100 kHz	2.13 Ω	40 W	22 W	24 W

Output current of fifth-generation fixed-frequency CoolSET™ in non-isolated buck design

Infineon® recommends the 65 kHz variant for a non-isolated Buck converter.

Table 2   Output current of fifth-generation generation fixed-frequency CoolSET™ in non-isolated buck design

Type	Package	Marking	V_{DS}	Fsw	R_{DSon}[1]	85-265 V AC[3] at DCM	Typical output voltage
ICE5BR4780BZ	PG-DIP-7	5BR4780BZ	800 V	65 kHz	4.13 Ω	450 mA	
ICE5BR3995BZ	PG-DIP-7	5BR3995BZ	950 V	65 kHz	3.46 Ω	550 mA	15 V
ICE5BR2280BZ	PG-DIP-7	5BR2280BZ	800 V	65 kHz	2.13 Ω	700 mA	

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[1] Typically at T_i = 25°C (inclusive of low side MOSFET).

[2] Calculated maximum output power rating in an open frame design at T_a = 50°C, T_j = 125°C (integrated high voltage MOSFET) and using minimum drain pin copper area in a 2 oz copper single-sided PCB. The output power figure is for selection purpose only. The actual power can vary depending on the designs. Contact a technical expert from Infineon® for more information.

[3] Calculated maximum output currrent rating in an open frame design at T_a = 50°C, T_j = 125°C (integrated high voltage MOSFET) and using minimum 100mm[2] drain pin copper area in a 2 oz copper single-sided PCB. The output current figure is for selection purpose only. The actual current can vary depending on the designs. Contact a technical expert from Infineon® for more information.
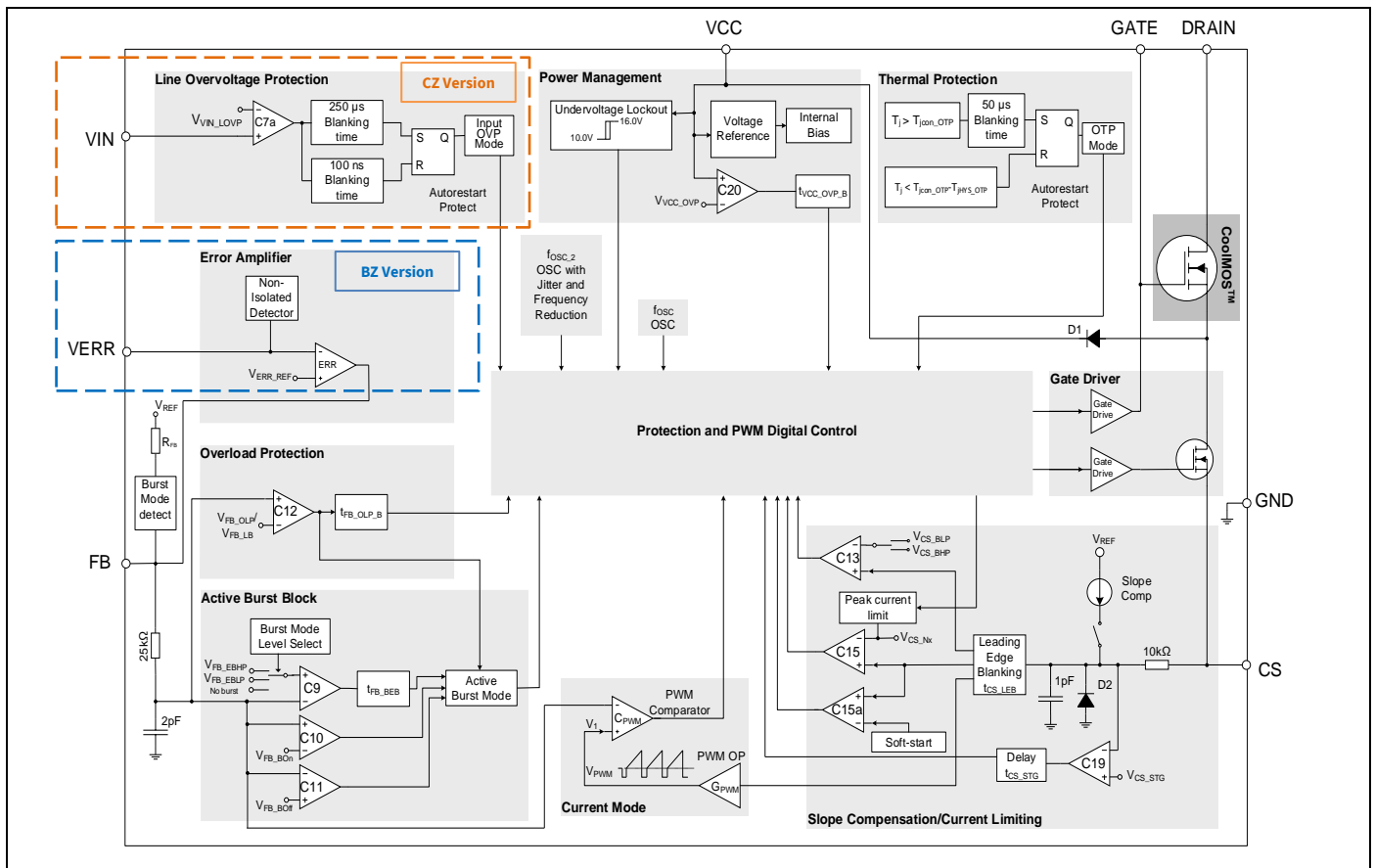
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1 Block diagram

Figure 4 **Block diagram**

Note: *Junction temperature of the controller chip is sensed for overtemperature protection. The CoolMOS™ is a separate chip from the controller chip in the same package. Refer to the design guide or consult a technical expert for the proper thermal design.*

2 Pin configuration

The pin configuration is shown in **Figure 5** and the functions are described in **Table 3**.
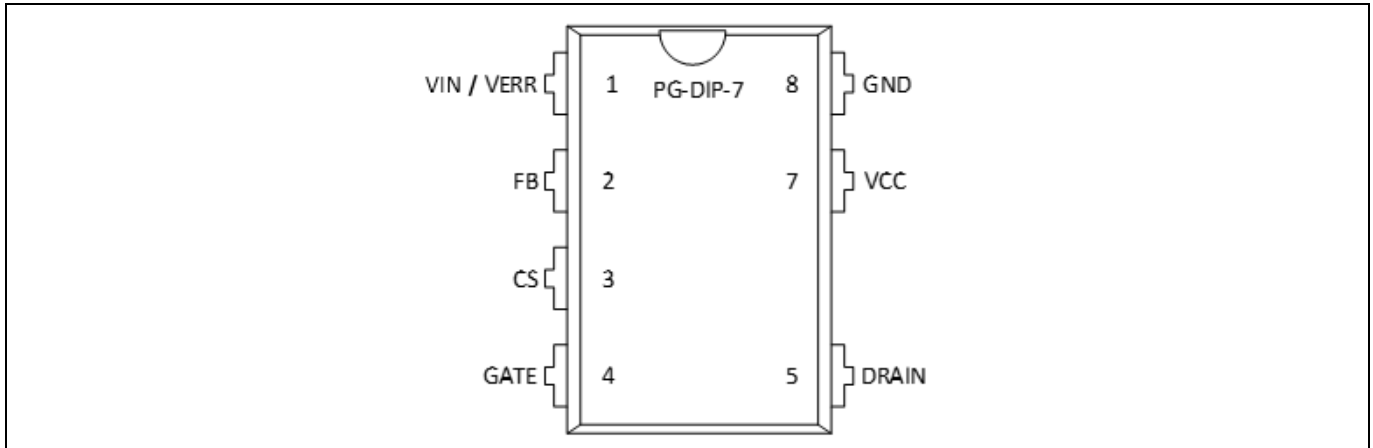

Figure 5 Pin configuration

Table 3 Pin definitions and functions

Pin	Symbol	Function
1	VERR (BZ version)	Error amplifier VERR pin is internally connected to the transconductance error amplifier for a non-isolated converter. Connect this pin to GND for an isolated converter.
	VIN (CZ version)	Input line overvoltage protection (LOVP) VIN pin is connected to the bus via a resistor divider (see **Figure 1**) to sense the line voltage. Internally, it is connected to the line overvoltage comparator which stops the switching when a LOVP condition occurs. To disable LOVP, connect this pin to GND.
2	FB	Feedback and ABM entry and exit control FB pin combines the functions of feedback control, selectable burst entry/exit control and overload/open loop protection.
3	CS	Current sense The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally.
4	GATE	Gate driver output The GATE pin is connected to the Gate of the internal CoolMOS™ and additionally, a pull-up resistor is connected from a bus voltage to turn on the internal CoolMOS™ for charging up the V_{CC} capacitor during startup.
5	DRAIN	DRAIN (Drain of integrated CoolMOS™) The DRAIN pin is connected to the drain of the integrated CoolMOS™.
7	VCC	VCC (Positive voltage supply) The VCC pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
8	GND	Ground The GND pin is the common ground of the controller.

3 Functional description

3.1 V_{CC} precharging and typical V_{CC} voltage during startup

As shown in **Figure 1**, once the line input voltage is applied, a rectified voltage appears across the capacitor C_{BUS}. The pull-up resistor $R_{STARTUP}$ provides a current to charge the C_{iss} (input capacitance) of CoolMOS™ and gradually generate one voltage level. If the voltage over C_{iss} is high enough, CoolMOS™ and the V_{CC} capacitor are charged through the primary inductance of a transformer L_P, CoolMOS™ and the internal diode D_1 with the two steps constant current source $I_{VCC\_Charge1}$[1] and $I_{VCC\_Charge3}$[1].

A very small constant current source ($I_{VCC\_Charge1}$) is charged to the V_{CC} capacitor until V_{CC} reaches V_{CC_SCP} to protect the controller from the V_{CC} pin short to ground during the startup. After this, the second step constant current source ($I_{VCC\_Charge3}$) is provided to charge the V_{CC} capacitor further, until the V_{CC} voltage exceeds the turned-on threshold V_{VCC_ON}. As shown in the time phase I in **Figure 6**, the V_{CC} voltage increases almost linearly with two steps.
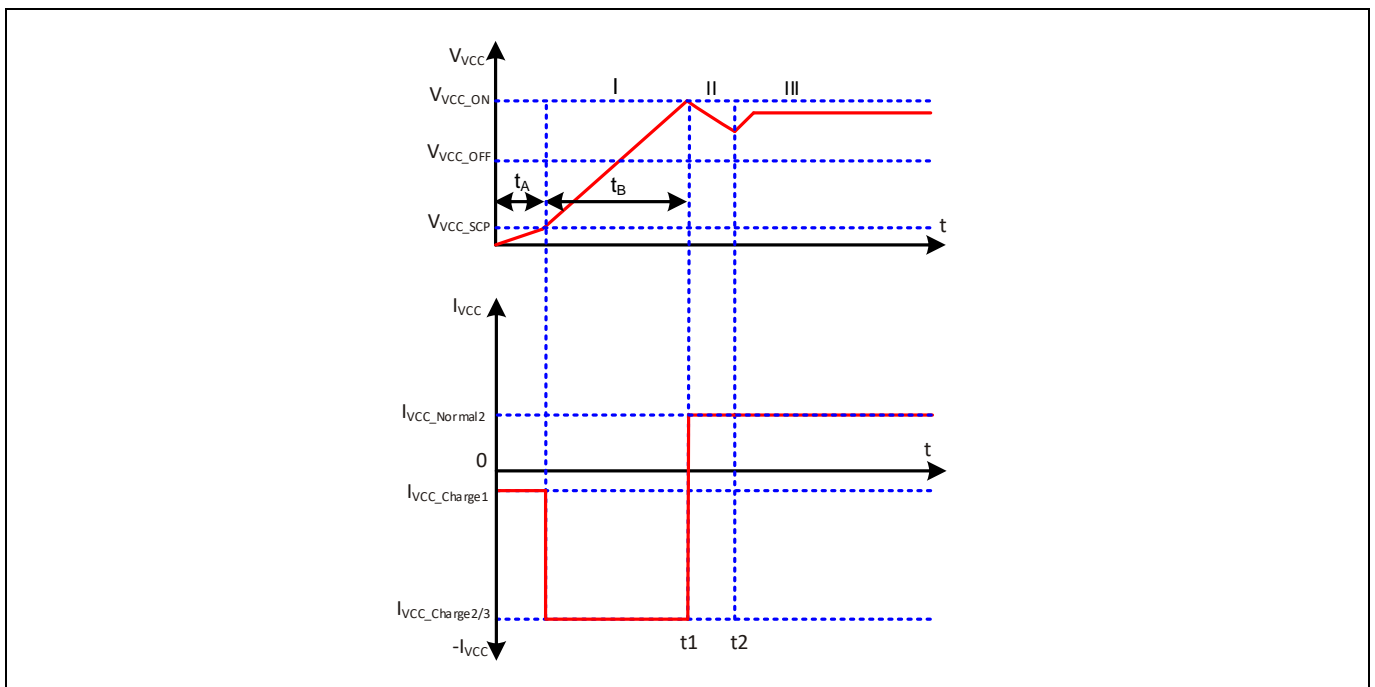

Figure 6 V_{CC} **voltage and current at startup**

The time for the V_{CC} precharging can then be calculated as:

$$t_1 = t_A + t_B = \frac{V_{VCC\_SCP} \times C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \times C_{VCC}}{I_{VCC\_Charge3}} \tag{1}$$

When the V_{CC} voltage exceeds the V_{CC} turn on threshold V_{VCC_ON} at time t_1, the IC starts to operate with soft start. Due to the power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V_{CC} capacitor before the output voltage is built up, the V_{CC} voltage drops (phase II). Once the output voltage rises close to regulation, the auxiliary winding starts to charge the V_{CC} capacitor from the time t_2 onward and delivering the $I_{VCC\_Normal2}$[2] to the CoolSET™. V_{CC} then reaches a constant value depending on the output load.

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[1] $I_{VCC\_Charge1/2/3}$ is charging current from the controller to VCC capacitor during startup.

[2] $I_{VCC\_Normal2}$ is supply current from VCC capacitor or auxiliary winding to the CoolSET™ during normal operation.

3.2 Soft start

As shown in **Figure 7**, the IC starts to operate with a soft start at time t_{on}. The switching stresses on the power MOSFET, diode, and transformer are minimized during soft start. The soft start implemented in ICE5xRxxxxxZ is a digital time-based function. The preset soft start time is t_{SS} (12 ms) with four steps. If not limited by other functions, the peak voltage on CS pin increases step by step from 0.3 V to finally V_{CS_N} (0.8 V). The normal feedback loop takes over the control when the output voltage reaches its regulated value.
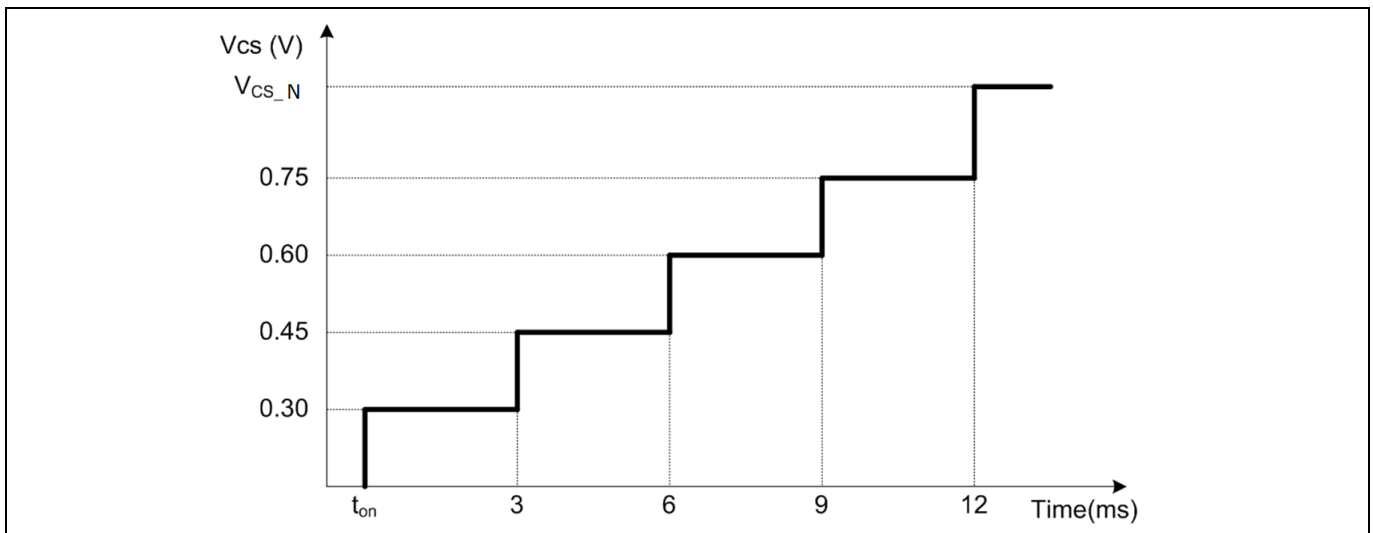

Figure 7   **Maximum current sense voltage during soft start**

3.3 Normal operation

The PWM controller during normal operation consists of a digital signal processing circuit including regulation control and an analog circuit including a current measurement unit and a comparator. Details about the full operation of the CoolSET™ in normal operation are illustrated in the following paragraphs.

3.3.1 PWM operation and peak current mode control

3.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with the internal oscillator with a switching frequency F_{SW} that corresponds to the voltage level V_{FB} (see **Figure 9**).

3.3.1.2 Switch-off determination

In peak current mode control, the PWM comparator monitors voltage V_1 (see **Figure 4**), which represents the instantaneous current of the power MOSFET. When V_1 exceeds V_{FB}, the PWM comparator sends a signal to switch off the GATE of the power MOSFET. Therefore, the peak current of the power MOSFET is controlled by the feedback voltage V_{FB} (see **Figure 8**).

At switch-on transient of the power MOSFET, a voltage spike across R_{CS} can cause V_1 to increase and exceed V_{FB}. To avoid a false switch off, the IC has a blanking time t_{CS_LEB} before detecting the voltage across R_{CS} to mask the voltage spike. Therefore, the minimum turn on time of the power MOSFET is t_{CS_LEB}.

If the voltage level at V_1 takes a long time to exceed V_{FB}, the IC has implemented a maximum duty cycle control to force the power MOSFET to switch off when $D_{MAX} = 0.75$ is reached.
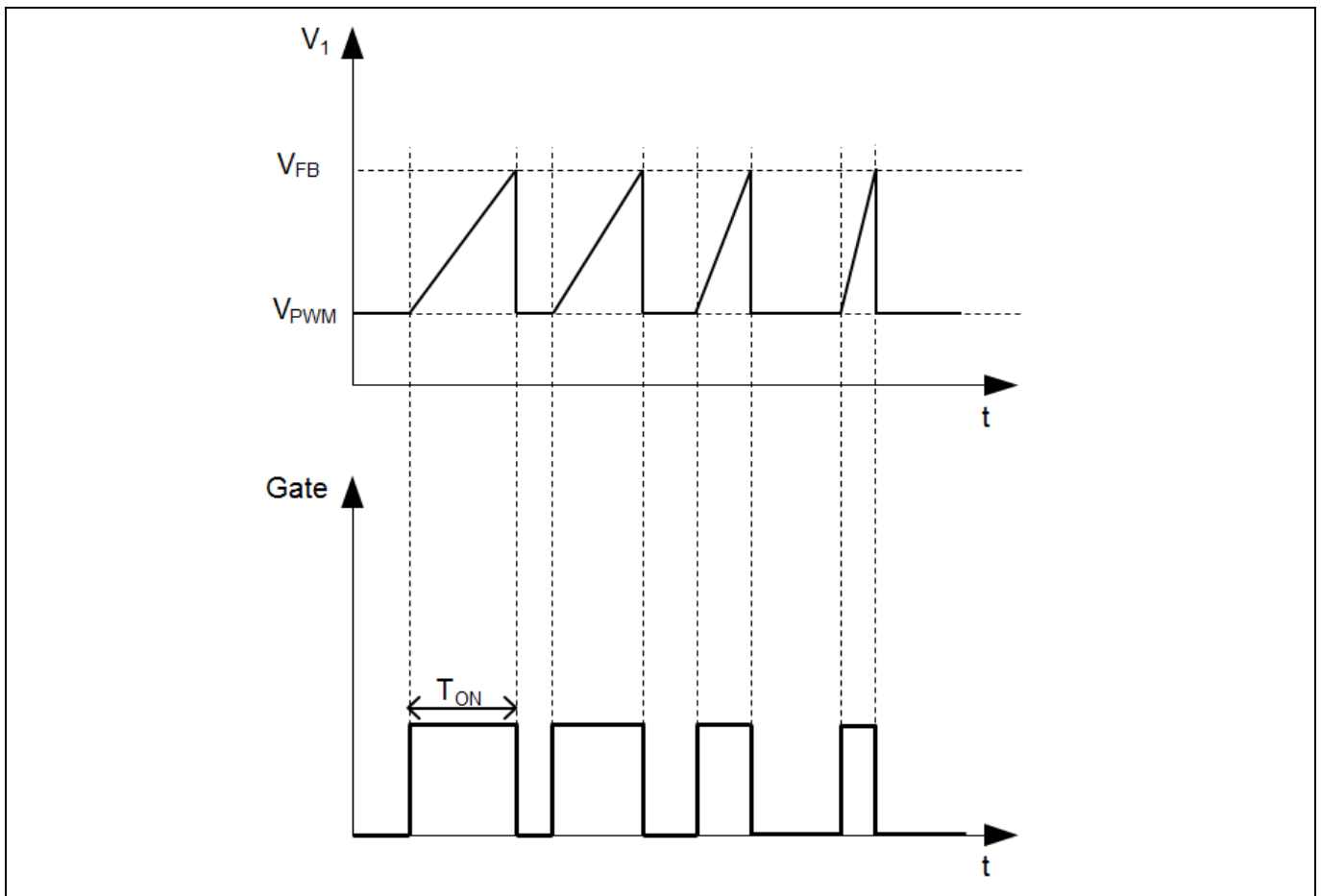
Figure 8   **Pulse width modulation**

3.3.2   Current sense

The power MOSFET current generates a voltage V_{CS} across the current sense resistor R_{CS} connected between the CS pin and the GND pin. V_{CS} is amplified with gain G_{PWM}, then, added with an offset V_{PWM} to become V_1 as described below in equation 3.

$$V_{CS} = I_D \times R_{CS} \tag{2}$$

$$V_1 = V_{CS} \times G_{PWM} + V_{PWM} \tag{3}$$

where:

V_{CS}	: CS pin voltage
I_D	: Power MOSFET current
R_{CS}	: Resistance of the current sense resistor
V_1	: Voltage level compared to V_{FB} as described in chapter **3.3.1.2**
G_{PWM}	: PWM-OP gain
V_{PWM}	: Offset for voltage ramp

If the voltage at the current sense pin is lower than the preset threshold V_{CS_STG} after the time $t_{CS\_STG\_SAM}$ for three consecutive pulses during on-time of the power switch, this abnormal V_{CS} triggers the IC into auto restart mode.

3.3.3 Frequency reduction

Frequency reduction is implemented in ICE5xRxxxxxZ to achieve a better efficiency during the light load. At light load, the reduced switching frequency F_{SW} improves efficiency by reducing the switching loses.

When the load decreases, V_{FB} decreases as well. F_{SW} is dependent on the V_{FB} as shown in **Figure 9**. Therefore, F_{SW} decreases as the load decreases.

For example, F_{SW} at high load is 65 kHz and starts to decrease at V_{FB} = 1.7 V. There is no further frequency reduction once it reached the f_{OSC2_MIN} even the load is further reduced.
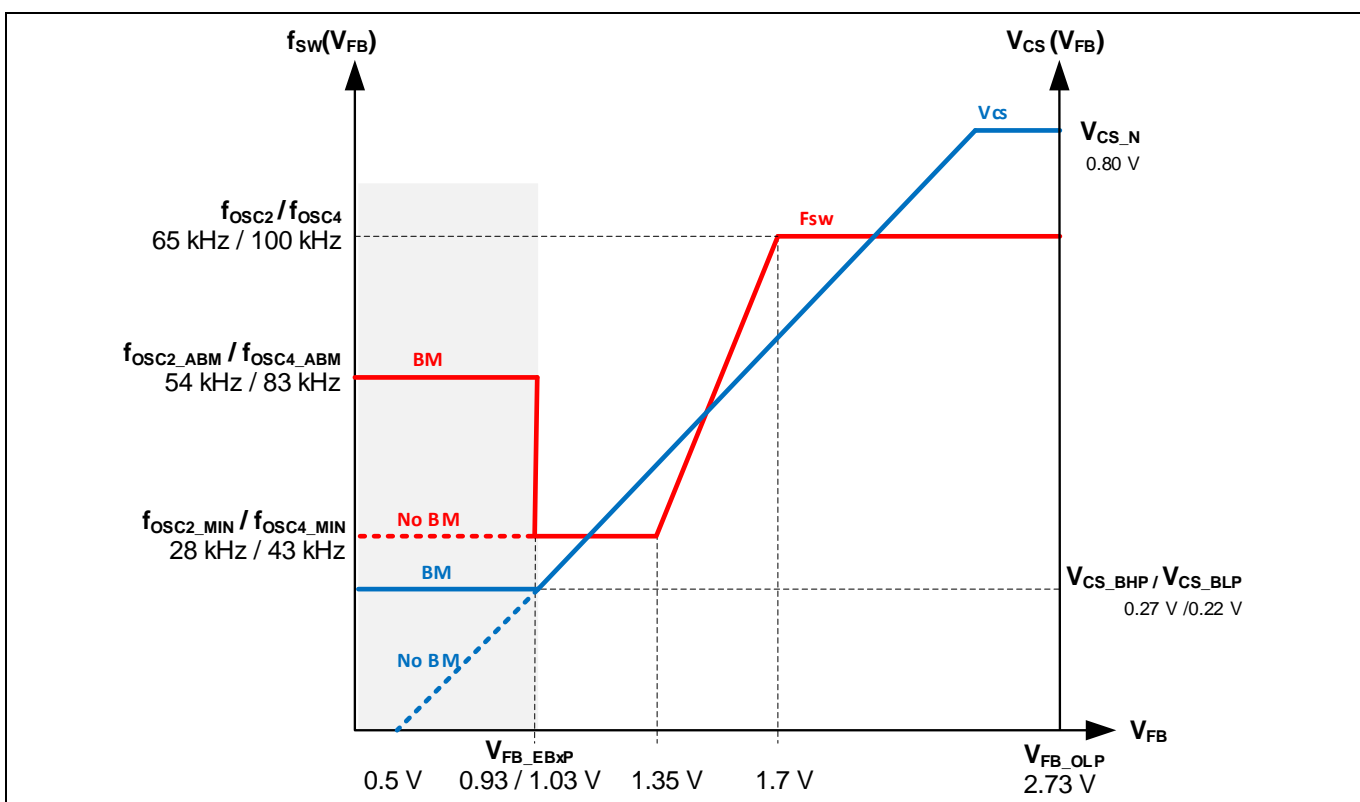

Figure 9 Frequency reduction curve

3.3.4 Slope compensation

ICE5xRxxxxxZ can operate at continuous conduction mode (CCM). At CCM operation, a duty cycle greater than 50% may generate a subharmonic oscillation. To avoid the subharmonic oscillation, slope compensation is added to V_{CS} pin when the gate of the power MOSFET is turned on for more than 40% of the switching cycle period.

The relationship between V_{FB} and the V_{CS} for CCM operation is described in equation 4:

$$V_{FB} = V_{CS} \times G_{PWM} + V_{PWM} + M_{COMP} \times (T_{ON} - 40\% \times T_{PERIOD})$$ (4)

where:

T_{ON} : Gate turn on time of the power MOSFET

M_{COMP} : Slope compensation rate

T_{PERIOD} : Switching cycle period

Slope compensation circuit is disabled and no slope compensation is added into the V_{CS} pin during Active Burst mode to save the power consumption.

3.3.5   Oscillator and frequency jittering

The oscillator generates a frequency of 65 kHz / 100 kHz with frequency jittering of ±4% at a jittering period of T_{JITTER} (4 ms). The frequency jittering helps to reduce conducted EMI.

A capacitor, a current source, and a current sink that determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed to achieve a highly accurate switching frequency.

Once the soft start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.

3.3.6   Modulated gate drive

The drive-stage is optimized for EMI consideration. The switch-on speed is slowed down before it reaches the CoolMOS™ turn on threshold. That is a slope control of the rising edge at the output of the driver (see **Figure 10**). Thus the leading switch spike during turn on is minimized.
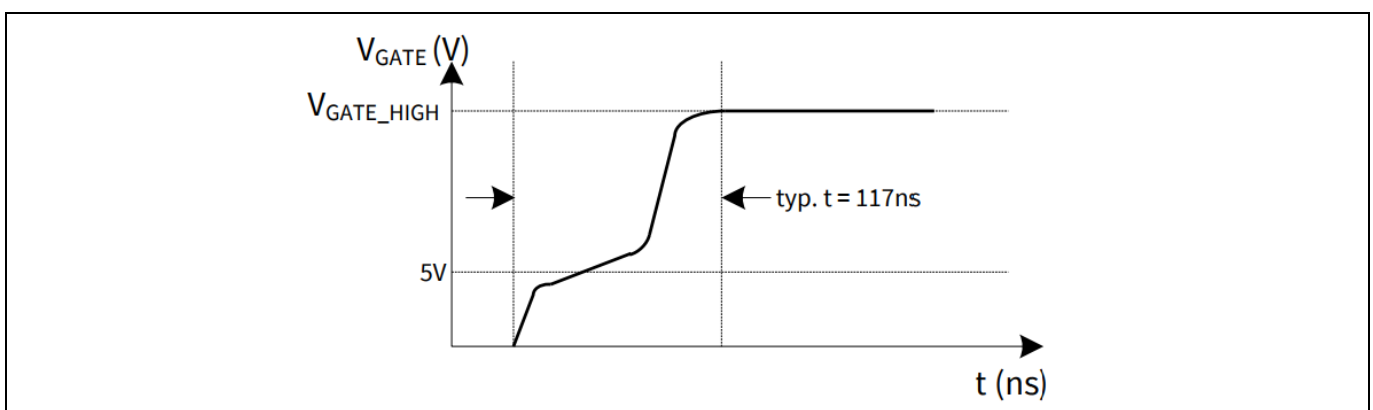

Figure 10   Gate rising waveform

3.4   Peak current limitation

There is a cycle-by-cycle peak current limitation realized by the current limit comparator to provide primary over-current protection. The primary current generates a voltage V_{CS} across the current sense resistor R_{CS} connected between the CS pin and the GND pin. If the voltage V_{CS} exceeds an internal voltage limit V_{CS_N}, the comparator immediately turns off the gate drive.

The primary peak current I_{PEAK_PRI} can be calculated as below:

$$I_{PEAK\_PRI} = V_{CS\_N}/R_{CS} \tag{5}$$

To avoid mistriggering caused by the MOSFET switch on transient voltage spikes, a leading edge-blanking time (t_{CS_LEB}) is integrated in the current sensing path.

3.4.1 Propagation delay compensation

In case of an overcurrent detection, there is always a propagation delay from sensing the V_{CS} to switching the power MOSFET off. An overshoot on the peak current I_{peak} caused by the delay depends on the ratio of dI/dt of the primary current (see **Figure 11**).
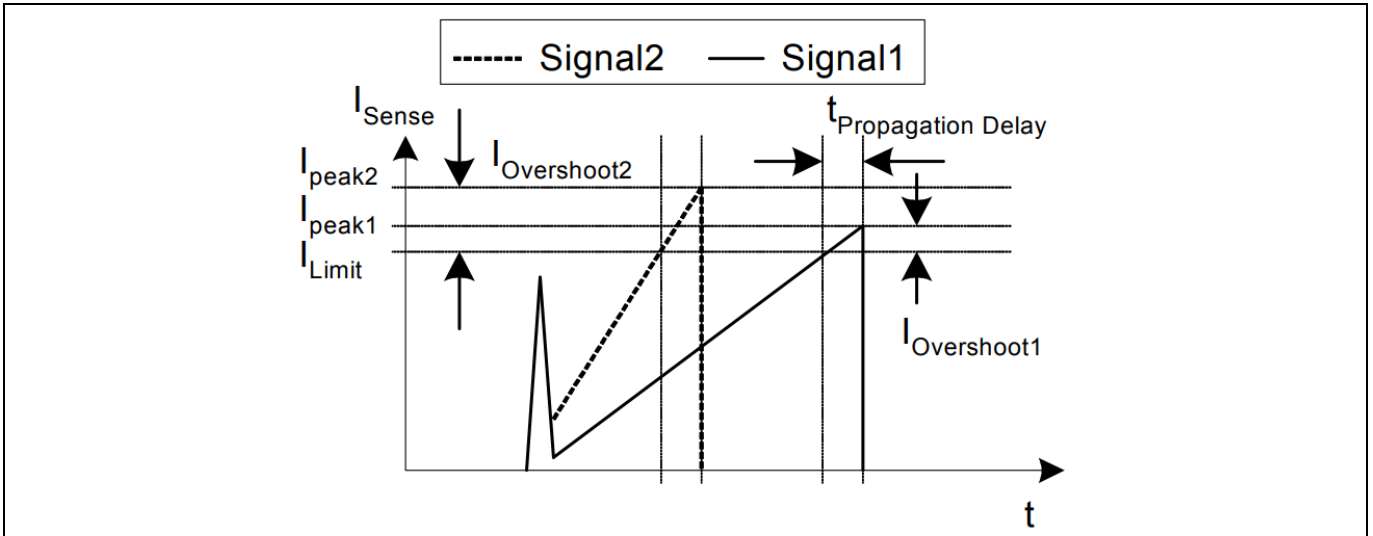

Figure 11   Current limiting

The overshoot of Signal2 is larger than Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation delay compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold V_{CS_N} and the switching off of the power MOSFET is compensated over wide bus voltage range. Current limiting becomes more accurate, which results in a minimum difference of overload protection triggering power between low and high AC line input voltage.

Under CCM operation, the same V_{CS} do not result in the same power. To achieve a close overload triggering level for CCM, ICE5xRxxxxxZ has implemented a two compensation curve as shown **Figure 12**. One of the curve is used for T_{ON} greater than 0.40 duty cycle and the other is for lower than 0.40 duty cycle.
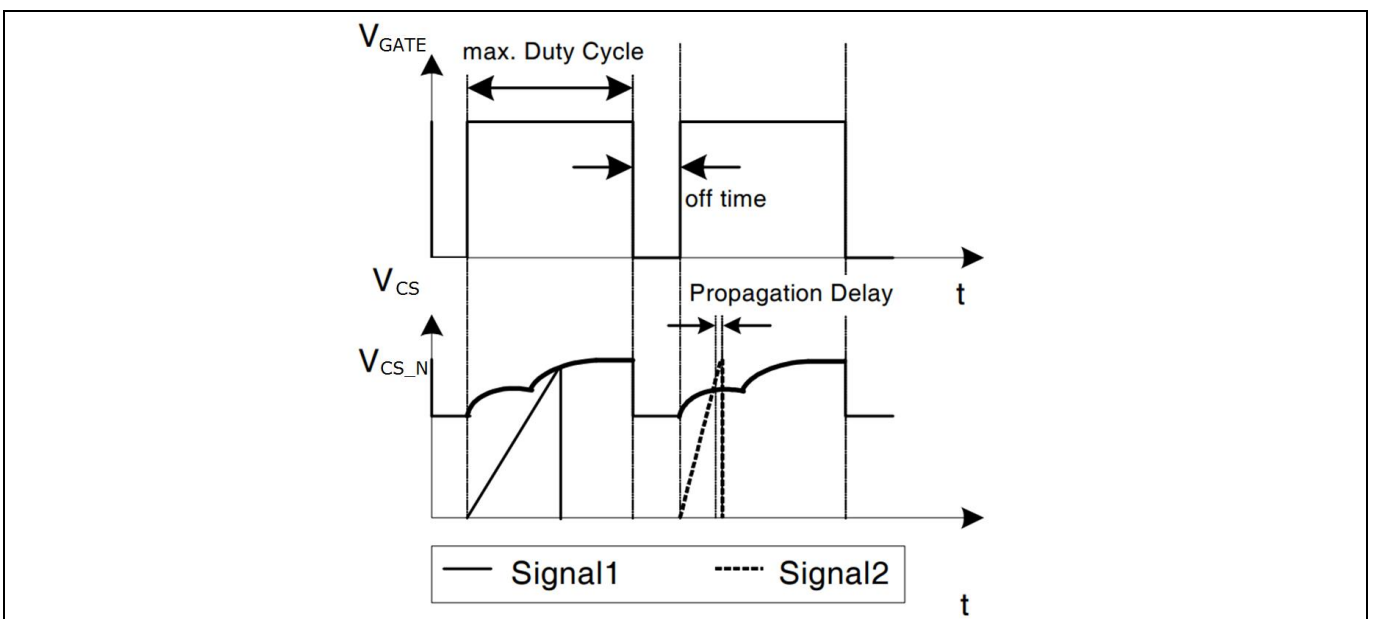

Figure 12   Dynamic voltage threshold V_{CS_N}

Similarly, the same concept of propagation delay compensation is also implemented in ABM with reduced level. With this implementation, the entry and exit Burst mode power can be close between low and high AC line input voltage.

3.5 Active burst mode with selectable power level

At light load condition, the IC enters Active Burst mode (ABM) operation to minimize the power consumption. Details about the ABM operation are explained in the following paragraphs.

3.5.1 Entering ABM operation

The system enters into ABM operation when the two conditions below are met:

- The FB voltage is lower than the threshold of V_{FB_EBLP}/V_{FB_EBHP}, depending on the burst configuration option setup.
- A certain blanking time t_{FB_BEB}.

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This multicondition determination for entering ABM operation prevents mis-triggering of entering ABM operation, so that the controller enters ABM operation only when the output power is really low.

3.5.2 During ABM operation

After entering ABM, the PWM section is inactive, making the V_{OUT} start to decrease. As the V_{OUT} decreases, V_{FB} rises. Once V_{FB} exceeded V_{FB_BOn}, the internal circuit is again activated by the internal bias to start with the switching.

If the PWM is still operating and the output load is still low, V_{OUT} increases and V_{FB} signal starts to decrease. When V_{FB} reaches the low threshold V_{FB_BOff}, the internal bias is reset again and the PWM section is disabled with no switching until V_{FB} increases back to exceed V_{FB_BOn} threshold.

In ABM, V_{FB} is like a sawtooth waveform swinging between V_{FB_BOff} and V_{FB_BOn} shown in **Figure 13**.

During ABM, the peak current I_{PEAK_ABM} of the power MOSFET is defined by:

$$I_{PEAK\_ABM} = V_{CS\_BxP}/R_{CS} \hspace{2cm} (6)$$

where V_{CS_BxP} is the peak current limitation in ABM.

3.5.3 Leaving ABM operation

The FB voltage immediately increases if there is a sudden increase in the output load. When V_{FB} exceeds V_{FB_LB}, it leaves ABM and the peak current limitation threshold voltage returns back to V_{CS_N} immediately.
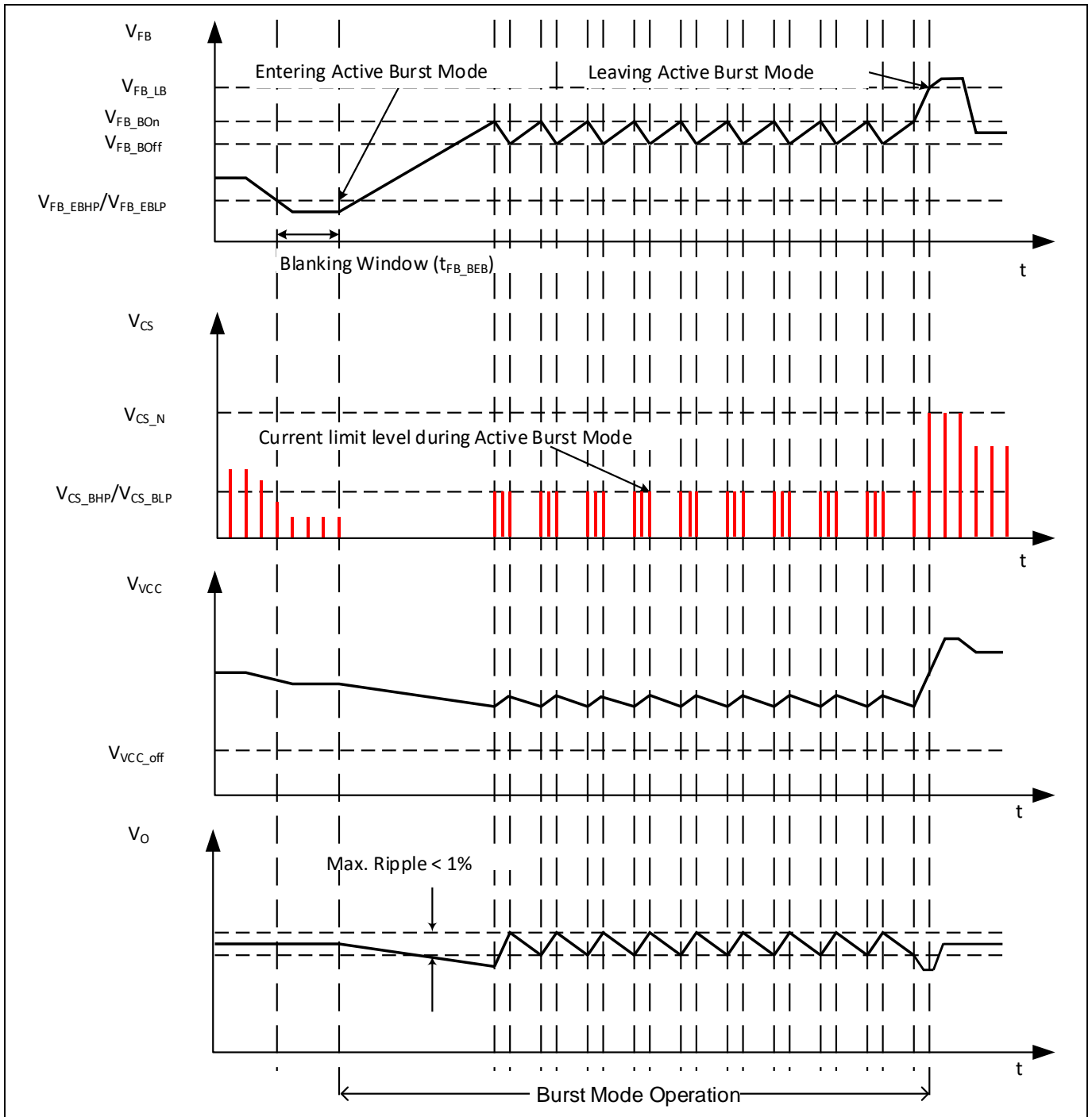
Figure 13   Signals in ABM

3.5.4 ABM configuration

The burst mode entry level can be selected by changing the different resistance R_{Sel} at FB pin. There are three configuration options depending on R_{Sel}, which corresponds to the options of no ABM (option 1), low range of ABM power (option 2) and high range of ABM power (option 3). The table below shows the control logic for the entry and exit level with the FB voltage.

Table 4   ABM configuration option setup

Option	R_{Sel}	V_{FB}	V_{CS_BxP}	Entry level	Exit level
				V_{FB_EBxP}	V_{FB_LB}
1	< 470 kΩ	$V_{FB} < V_{FB\_P\_BIAS1}$	-	No ABM	No ABM
2	720 kΩ ~ 790 kΩ	$V_{FB\_P\_BIAS1} < V_{FB} < V_{FB\_P\_BIAS2}$	0.22 V	0.93 V	2.73 V
3 (default)	> 1210 kΩ	$V_{FB} > V_{FB\_P\_BIAS2}$	0.27 V	1.03 V	2.73 V

During IC first startup, the controller preset the ABM selection to option 3, the FB resistor (R_{FB}) is turned off by internal switch S2 (see **Figure 14**) and a current source I_{sel} is turned on instead. From $V_{CC} = 4.44$ V to V_{CC} on threshold, the FB pin starts to charge resistor R_{Sel} with current I_{Sel} to a certain voltage level. When V_{CC} reaches V_{CC} on threshold, the FB voltage is sensed. The burst mode option is then chosen according to the FB voltage level. After finishing the selection, any change on the FB level does not change the burst mode option and the current source (I_{sel}) is turned off while the FB resistor (R_{FB}) is connected back to the circuit (**Figure 14**).
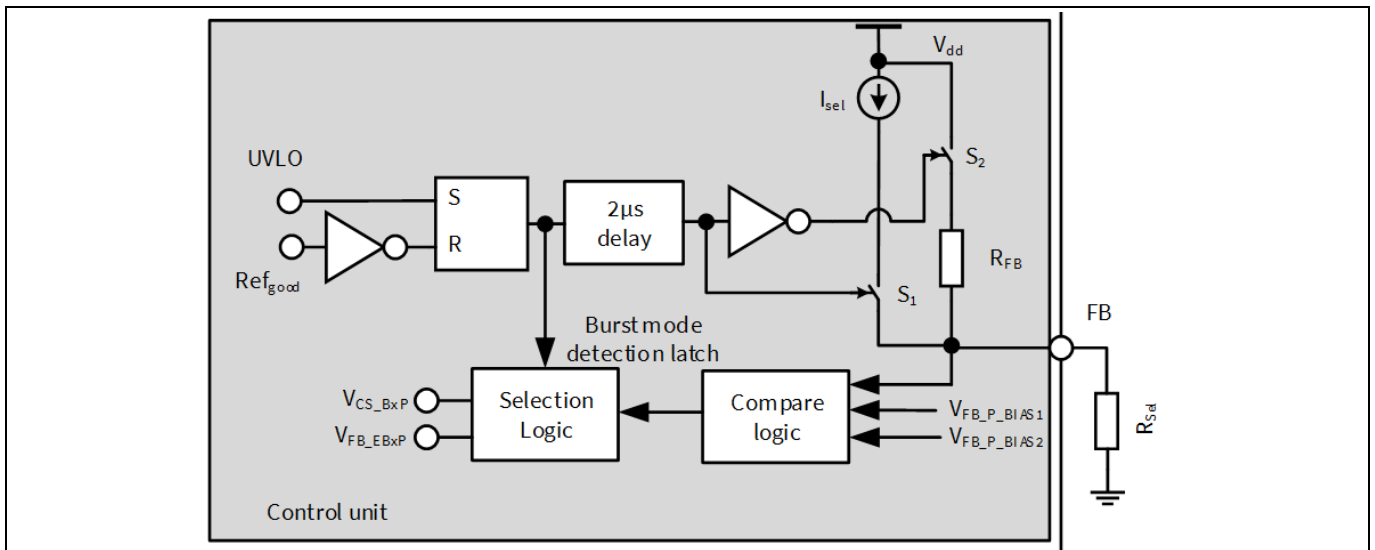

Figure 14   ABM detect and adjust

3.6 Non-isolated/isolated configuration

ICE5xRxxxxBZ has a VERR pin, which is connected to the input of an integrated error amplifier to support a non-isolated converter (see **Figure 2**). When V_{CC} is charging and before reaching the V_{CC} on threshold, a current source $I_{ERR\_P\_BIAS}$ from the VERR pin together with R_{F1} and R_{F2} generates a voltage across it. If the VERR voltage is more than $V_{ERR\_P\_BIAS}$ (0.2 V), non-isolated configuration is selected, otherwise, isolated configuration is selected. In an isolated configuration, the error amplifier output is disconnected from the FB pin.

In case of non-isolated configuration, the voltage divider R_{F1} and R_{F2} are used to sense the output voltage and compared with the internal reference voltage V_{ERR_REF}. The difference between the sensed voltage and the

reference voltage is converted as an output current by the error amplifier. The output current charges or discharges the resistor and capacitor network connected at the FB pin for the loop compensation.

3.7 Protection functions

The ICE5xRxxxxxZ provides numerous protection functions that considerably improve the power supply system robustness, safety, and reliability. The following table summarizes these protection functions and the corresponding protection mode whether as a non-switch auto restart, auto restart or odd skip auto restart mode. Refer to **Figure 15**, **Figure 16** and **Figure 17** for the waveform illustration of protection modes.

Table 5   **Protection functions**

Protection functions	Normal mode	Burst mode		Protection mode
		Burst ON	**Burst OFF**	
Line overvoltage (CZ version)	√	√	√	Non-switch auto restart
V_{CC} overvoltage	√	√	n/a[1]	Odd skip auto restart
V_{CC} undervoltage	√	√	√	Auto restart
Overload or open loop	√	n/a[1]	n/a[1]	Odd skip auto restart
Overtemperature	√	√	√	Non-switch auto restart
V_{CC} short to GND	√	√	√	No startup

3.7.1 Line overvoltage (CZ version)

The AC line overvoltage protection (LOVP) is detected by the sensing bus capacitor voltage through the VIN pin via the voltage divider resistors, R_{l1} and R_{l2} (**Figure 1**). Once the V_{VIN} voltage is higher than the line overvoltage threshold (V_{VIN_LOVP}), the controller enters into protection mode until V_{VIN} is lower than V_{VIN_LOVP}. This protection can be disabled by connecting the VIN pin to GND.

3.7.2 V_{CC} overvoltage and undervoltage

During operation, the V_{CC} voltage is continuously monitored. If V_{CC} is either below V_{VCC_OFF} for 50 μs ($t_{VCC\_OFF\_B}$) or above V_{VCC_OVP} for 55 μs ($t_{VCC\_OVP\_B}$), the power MOSFET is kept switch off. After the V_{CC} voltage falls below the threshold V_{VCCoff}, the new startup sequence is activated. The V_{CC} capacitor is then charged up. Once the voltage exceeds the threshold V_{VCC_ON}, the IC begins to operate with a new soft start.

3.7.3 Overload or open loop

In case of open control loop or output overload, the FB voltage is pulled up. When V_{FB} exceeds V_{FB_OLP} after a blanking time of $t_{FB\_OLP\_B}$, the IC enters odd skip auto restart mode. The blanking time enables the converter to provide a peak power in case the increase in V_{FB} is due to a sudden load increase.

3.7.4 Overtemperature

If the junction temperature of the controller exceeds T_{jcon_OTP}, the IC enters into overtemperature protection (OTP) auto restart mode. The IC has also implemented with a 40°C hysteresis. That means the IC can only be recovered from OTP when the controller junction temperature is dropped 40°C lower than the overtemperature trigger point.

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[1] Not applicable.

3.7.5 V_{CC} short to GND

To limit the power dissipation of the startup circuit at V_{CC} short to GND condition, the V_{CC} charging current is limited to a minimum level of $I_{VCC\_Charge1}$. With such low current, the power loss of the IC is limited to prevent overheating.

3.7.6 Protection modes

All the protections are in auto restart mode with a new soft start sequence. The three auto restart modes are illustrated in the following figures.
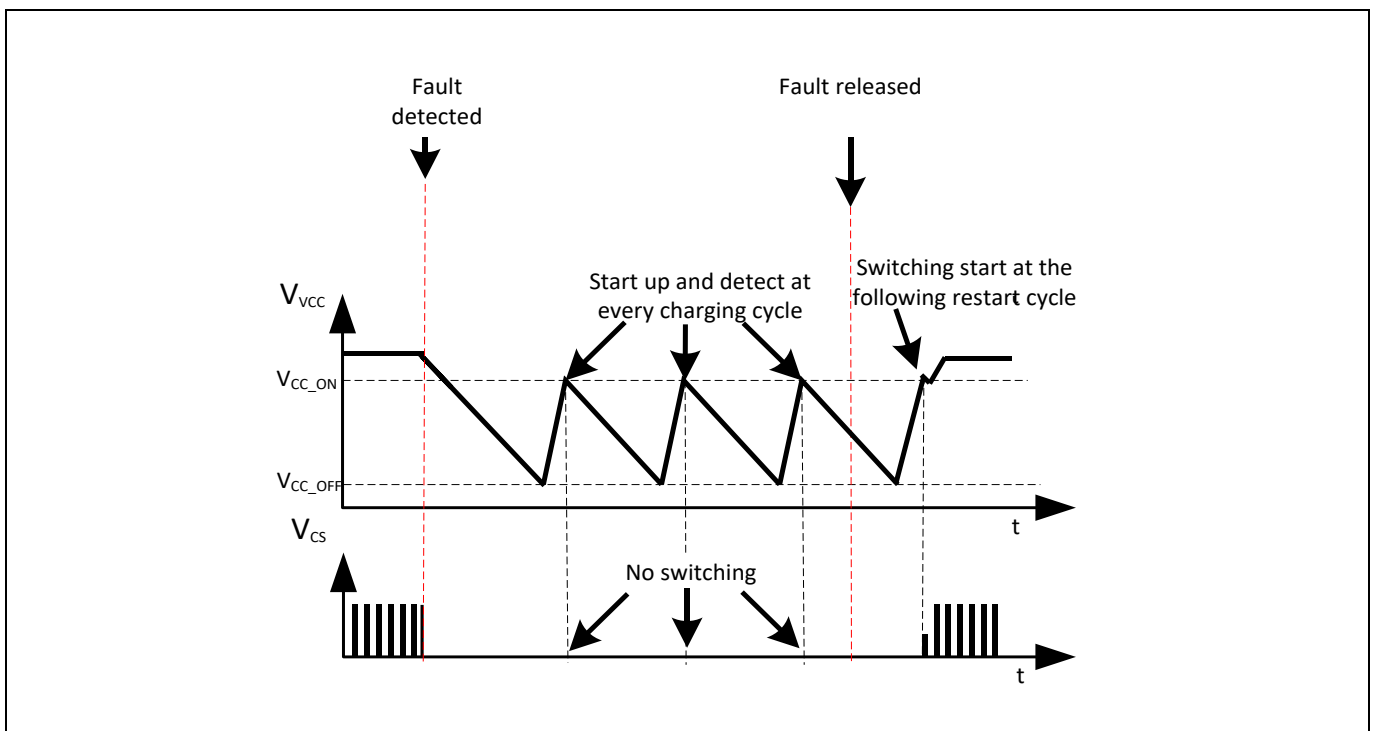

Figure 15   Non-switch auto restart mode
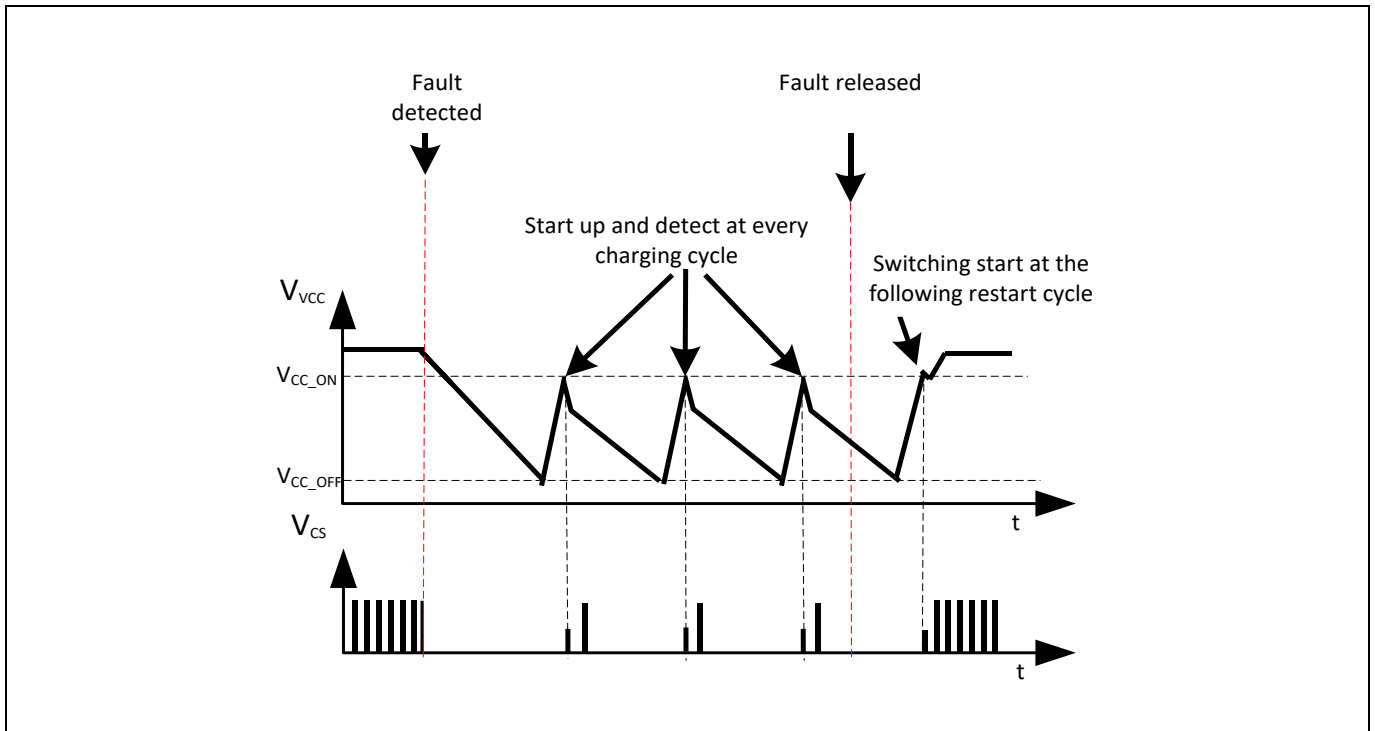
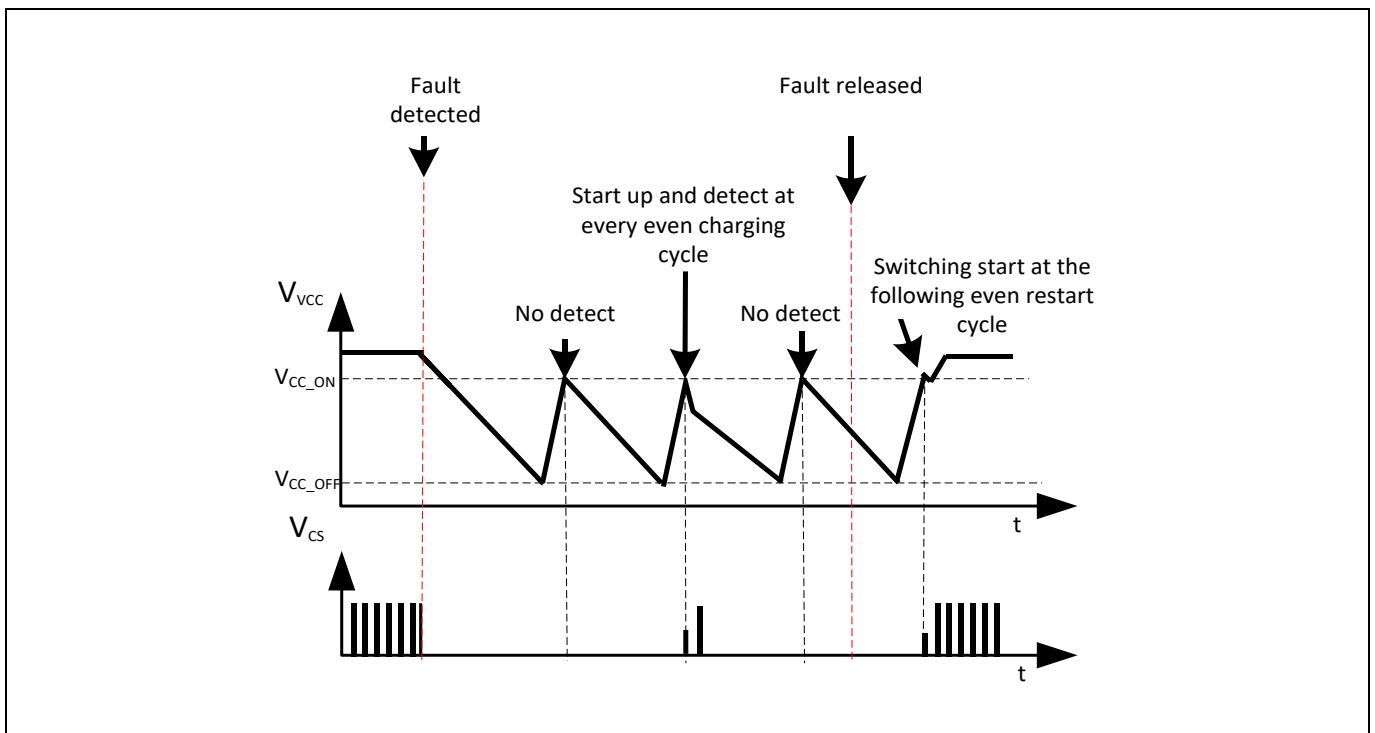**Figure 16   Auto restart mode**

Figure 17   Odd skip auto restart

4 Electrical characteristics

Attention: *All voltages are measured with respect to ground (pin 8). The voltage levels are valid if other ratings are not violated.*

4.1 Absolute maximum ratings

Attention: *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. For the same reason, make sure that any capacitor that is connected to pin 7 (VCC) is discharged before assembling the application circuit. T_a = 25°C unless otherwise specified.*

Table 6   **Absolute maximum ratings**

Parameter	Symbol	Limit values		Unit	Note or test condition
		Min.	Max.		
Drain voltage ICE5xRxx80xZ ICE5xR3995xZ	V_{DRAIN} 	 800 950	 – –	V	T_j = 25°C
Pulse drain current ICE5xR3995xZ ICE5BR4780BZ ICE5xR2280xZ	$I_{D,Pulse}$ 	 – – –	 5.0^1 2.6^1 5.8^2	A	
Avalanche energy, repetitive, t_{AR} limited by maximal T_j = 150°C and $T_{j,Start}$ = 25°C ICE5xR2280xZ ICE5BR4780BZ ICE5xR3995xZ	E_{AR} 	 – – –	 0.05 0.02 0.04	mJ	 I_D = 0.40 A, V_{DD} = 50 V I_D = 0.20 A, V_{DD} = 50 V I_D = 0.20 A, V_{DD} = 50 V
Avalanche current, repetitive, t_{AR} limited by maximal T_j = 150°C and $T_{j,Start}$ = 25°C ICE5BR4780BZ ICE5xR3995xZ ICE5xR2280xZ	I_{AR} 	 – – –	 0.20 0.20 0.40	A	
VCC supply voltage	V_{CC}	-0.3	27.0	V	
GATE voltage	V_{GATE}	-0.3	27.0	V	
FB voltage	V_{FB}	-0.3	3.6	V	
VERR voltage	V_{ERR}	-0.3	3.6	V	
CS voltage	V_{CS}	-0.3	3.6	V	
VIN voltage	V_{VIN}	-0.3	3.6	V	
Maximum DC current on any pin		-10.0	10.0	mA	Except DRAIN and CS pin.

---

[1] Pulse width t_P limited by $T_{j,max}$.

[2] Pulse width t_P = 20 µs and limited by $T_{j,max}$.

Parameter	Symbol	Limit values		Unit	Note or test condition
		Min.	Max.		
ESD robustness HBM	V_{ESD_HBM}	–	2000	V	According to EIA/JESD22.
ESD robustness CDM	V_{ESD_CDM}	–	500	V	
Junction temperature range	T_j	-40	150	°C	Controller and CoolMOS™.
Storage temperature	T_{STORE}	-55	150	°C	
Thermal resistance (junction-ambient) ICE5BR4780BZ ICE5xR3995xZ ICE5xR2280xZ	R_{thJA}	– – –	107 106 104	K/W	Setup according to the JEDEC standard JESD51 and using minimum drain pin copper area in a 2 oz copper single-sided PCB.

4.2 Operating range

Note: *Within the operating range, the IC operates as described in the functional description.*

Table 7 **Operating range**

Parameter	Symbol	Limit values		Unit	Note or test condition
		Min.	Max.		
VCC supply voltage	V_{VCC}	V_{VCC_OFF}	V_{VCC_OVP}		
Junction temperature of controller	T_{jCon_op}	-40	T_{jCon_OTP}	°C	Maximum value limited due to OTP of controller chip.
Junction temperature of CoolMOS™	$T_{jCoolMOS\_op}$	-40	150	°C	

4.3 Operating conditions

Note: *The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 40°C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 18 V is assumed.*

Table 8 **Operating conditions**

Parameter	Symbol	Limit values			Unit	Note or test Condition
		Min.	Typ.	Max.		
VCC charge current	$I_{VCC\_Charge1}$	-0.35	-0.20	-0.09	mA	V_{VCC} = 0 V, $R_{StartUp}$ = 50 MΩ and V_{DRAIN} = 90 V
	$I_{VCC\_Charge2}$	–	-3.2	–	mA	V_{VCC} = 3 V, $R_{StartUp}$ = 50 MΩ and V_{DRAIN} = 90 V
	$I_{VCC\_Charge3}$	-5	-3	-1	mA	V_{VCC} = 15 V, $R_{StartUp}$ = 50 MΩ and V_{DRAIN} = 90 V
Current consumption, startup current	$I_{VCC\_Startup}$	–	0.25	–	mA	V_{VCC} = 15 V
Current consumption, normal with Inactive Gate	$I_{VCC\_Normal1}$	–	0.9	–	mA	I_{FB} = 0 A

Parameter	Symbol	Limit values			Unit	Note or test Condition
		Min.	Typ.	Max.		
Current consumption, normal with Active Gate	$I_{VCC\_Normal2}$				mA	
ICE5BR2280BZ		–	–	1.89		
ICE5BR3995xZ		–	–	1.82		
ICE5AR3995BZ		–	–	2.21		
ICE5BR4780BZ		–	–	1.69		
ICE5AR2280CZ		–	–	2.31		
Current consumption, auto restart	I_{VCC_AR}	–	410	–	µA	
Current consumption, Burst mode – isolated	$I_{VCC\_Burst Mode\_ISO}$	–	0.54	–	mA	
Current consumption, Burst mode – non-isolated	$I_{VCC\_Burst Mode\_NISO}$	–	0.61	–	mA	
VCC turn-on threshold voltage	V_{VCC_ON}	15.3	16.0	16.5	V	
VCC turn-off threshold voltage	V_{VCC_OFF}	9.4	10.0	10.4	V	
VCC short circuit protection	V_{VCC_SCP}	–	1.1	1.9	V	
VCC turn-off blanking	$t_{VCC\_OFF\_B}$	–	50	–	µs	

4.4 Internal voltage reference

Table 9   Internal voltage reference

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Internal reference voltage	V_{REF}	3.20	3.30	3.39	V	Measured at FB pin $I_{FB} = 0$ A

4.5 PWM section

Table 10   PWM section

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Fixed oscillator frequency – 100 kHz	f_{OSC3}	92	100	108	kHz	
	f_{OSC4}	94	100	106	kHz	$T_j = 25°C$
Fixed oscillator frequency – 100 kHz (ABM)	f_{OSC4_ABM}	71	83	94	kHz	$T_j = 25°C$
Fixed oscillator frequency – 100 kHz (minimum F_{sw})	f_{OSC4_MIN}	36	43	51	kHz	$T_j = 25°C$
Fixed oscillator frequency – 65 kHz	f_{OSC1}	59.8	65	70.2	kHz	
	f_{OSC2}	61.1	65	68.9	kHz	$T_j = 25°C$
Fixed oscillator frequency – 65 kHz (ABM)	f_{OSC2_ABM}	46.2	54	61.1	kHz	$T_j = 25°C$

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Fixed oscillator frequency – 65 kHz (minimum F_{sw})	f_{OSC2_MIN}	23.4	28	33.2	kHz	$T_j = 25°C$
Frequency jittering range	F_{JITTER}	–	± 4	–	%	$T_j = 25°C$
Frequency jittering period	T_{JITTER}	–	4	–	ms	$T_j = 25°C$
Maximum duty cycle	D_{MAX}	70	75	80	%	
Feedback pull-up resistor	R_{FB}	11	15	20	kΩ	
PWM-OP gain	G_{PWM}	1.91	2.03	2.16		
Offset for voltage ramp	V_{PWM}	0.42	0.50	0.58	V	
Slope compensation rate - 100 kHz	M_{COMP}	41	50	58	mV/µs	$V_{cs} = 0\ V$
Slope compensation rate - 65 kHz	M_{COMP}	26.5	32.5	38	mV/µs	$V_{cs} = 0\ V$

4.6   Error amplifier

Table 11   Error amplifier

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Transconductance	G_{ERR_M}	2.14	2.80	3.44	mA/V	
Transconductance – Burst mode	G_{ERR_BM}	6.9	9.2	11.6	mA/V	
Error amplifier source current	I_{ERR_SOURCE}	85	150	223	µA	
Error amplifier sink current	I_{ERR_SINK}	85	150	223	µA	
Error amplifier reference voltage	V_{ERR_REF}	1.76	1.80	1.84	V	
Error amplifier output dynamic range of transconductance	V_{ERR_DYN}	0.05	–	3.15	V	
Error amplifier mode bias current	$I_{ERR\_P\_BIAS}$	9.5	14.0	18.5	µA	
Error amplifier mode threshold	$V_{ERR\_P\_BIAS}$	0.16	0.20	0.24	V	

4.7   Current sense

Table 12   Current sense

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	V_{CS_N}	0.72	0.80	0.88	V	$dV_{sense}/dt = 0.41\ V/µs$
Peak current limitation in normal operation, 15% of T_{ON}	V_{CS_N15}	0.74	0.79	0.84	V	
Leading edge-blanking time	t_{CS_LEB}	70	220	365	ns	
Peak current limitation in ABM - high power	V_{CS_BHP}	0.23	0.27	0.31	V	

Peak current limitation in ABM - low power	V_{CS_BLP}	0.18	0.22	0.26	V	
Abnormal CS voltage threshold	V_{CS_STG}	0.06	0.10	0.15	V	
Abnormal CS voltage consecutive trigger	P_{CS_STG}	–	3	–	cycle	
Abnormal CS voltage sample period	$t_{CS\_STG\_SAM}$	t_{PERIOD} × 0.36	t_{PERIOD} × 0.4	t_{PERIOD} × 0.44	µs	

4.8 Soft start

Table 13   Soft start

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Soft start time	t_{SS}	7.3	12.0	–	ms	
Soft start time step	t_{SS_s}[1]	–	3	–	ms	
CS peak voltage at first step of soft start	V_{SS1}[1]	–	0.30	–	V	CS peak voltage.
Step increment of CS peak voltage in soft start	V_{SS_s}[1]	–	0.15	–	V	CS peak voltage.

4.9 Active burst mode

Table 14   Active Burst mode

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Charging current to select burst mode	I_{sel}	2.5	3.0	3.5	µA	
Burst mode selection reference voltage threshold	$V_{FB\_P\_BIAS1}$	1.65	1.73	1.80	V	
Burst mode selection reference voltage threshold	$V_{FB\_P\_BIAS2}$	2.76	2.89	3.01	V	
Feedback voltage for entering ABM for high power	V_{FB_EBHP}	0.98	1.03	1.08	V	
Feedback voltage for entering ABM for low power	V_{FB_EBLP}	0.88	0.93	0.98	V	
Blanking time for entering ABM	t_{FB_BEB}	–	36	–	ms	
Feedback voltage for leaving ABM	V_{FB_LB}	2.63	2.73	2.83	V	
Feedback voltage for burst-on – isolated case	$V_{FB\_Bon\_ISO}$	2.26	2.35	2.45	V	
Feedback voltage for burst-off – isolated case	$V_{FB\_BOff\_ISO}$	1.88	2.00	2.05	V	

[1] Not subject to production test, specified by design.

Feedback voltage for burst-on – non-isolated case	$V_{FB\_Bon\_NISO}$	1.88	1.95	2.05	V	
Feedback voltage for burst-off – non-isolated case	$V_{FB\_BOff\_NISO}$	1.50	1.55	1.64	V	

4.10 Line overvoltage protection (CZ version)

Table 15   Line OVP

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line overvoltage threshold	V_{VIN_LOVP}	2.75	2.85	2.95	V	
Line overvoltage blanking	$t_{VIN\_LOVP\_B}$	–	250	–	µs	

4.11 V_{CC} overvoltage protection

Table 16 V_{CC} overvoltage protection

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
VCC overvoltage threshold	V_{VCC_OVP}	24.0	25.5	27.0	V	
VCC overvoltage blanking	$t_{VCC\_OVP\_B}$	–	55	–	µs	

4.12 Overload protection

Table 17   Overload protection

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Overload detection threshold for OLP protection at FB pin	V_{FB_OLP}	2.63	2.73	2.83	V	
Overload protection blanking time	$t_{FB\_OLP\_B}$	30	54	–	ms	

4.13 Thermal protection

Table 18   Thermal protection

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Overtemperature protection	T_{jcon_OTP}[1]	129	140	150	℃	Junction temperature of the controller chip (not the CoolMOS™ chip).
Overtemperature hysteresis	T_{jHYS_OTP}	–	40	–	℃	
Overtemperature blanking time	$T_{jcon\_OTP\_B}$	–	50	–	µs	

[1]Not subject to production test, specified by design.

4.14 CoolMOS™ section

Table 19   ICE5xRxxxxxZ

Parameter	Symbol	Limit values			Unit	Note or test condition
		Min.	Typ.	Max.		
Drain source breakdown voltage	$V_{(BR)DSS}$				V	$T_j = 25°C$
ICE5xRxx80xZ		800	–	–		
ICE5xR3995xZ		950	–	–		
Drain source on-resistance (inclusive of low side MOSFET)	R_{DSon}				Ω	
ICE5BR4780BZ		–	4.13	4.85		$T_j = 25°C$
		–	8.69^1	–		$T_j = 125°C$ at $I_D = 0.4$ A
ICE5xR2280xZ		–	2.13	2.35		$T_j = 25°C$
		–	4.31^1	–		$T_j = 125°C$ at $I_D = 1$ A
ICE5xR3995xZ		–	3.46	4.05		$T_j = 25°C$
		–	7.69^1	–		$T_j = 125°C$ at $I_D = 0.8$ A
Effective output capacitance, energy related[1]	$C_{o(er)}$				pF	
ICE5BR4780BZ		–	3	–		$V_{GS} = 0$ V, $V_{DS} = 0 \sim 500$ V
ICE5xR2280xZ		–	7	–		$V_{GS} = 0$ V, $V_{DS} = 0 \sim 500$ V
ICE5xR3995xZ		–	5	–		$V_{GS} = 0$ V, $V_{DS} = 0 \sim 400$ V
Rise time	t_{rise}^2	–	30	–	ns	
Fall time	t_{fall}^2	–	30	–	ns	

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[1]Not subject to production test, specified by design.

[2]Measured in a typical flyback / buck converter application.

5   CoolMOS™ performance characteristics
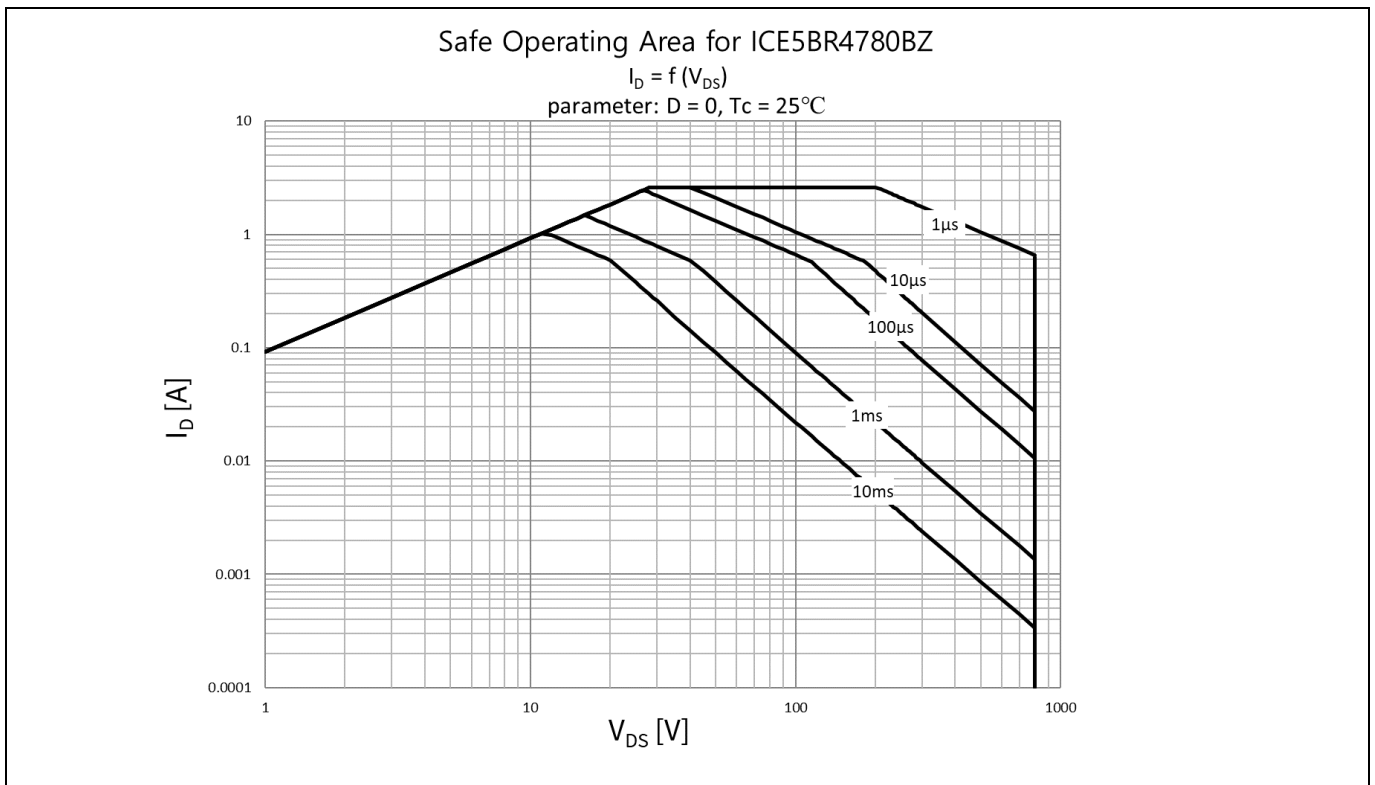
Figure 18   Safe operating area (SOA) curve for ICE5BR4780BZ
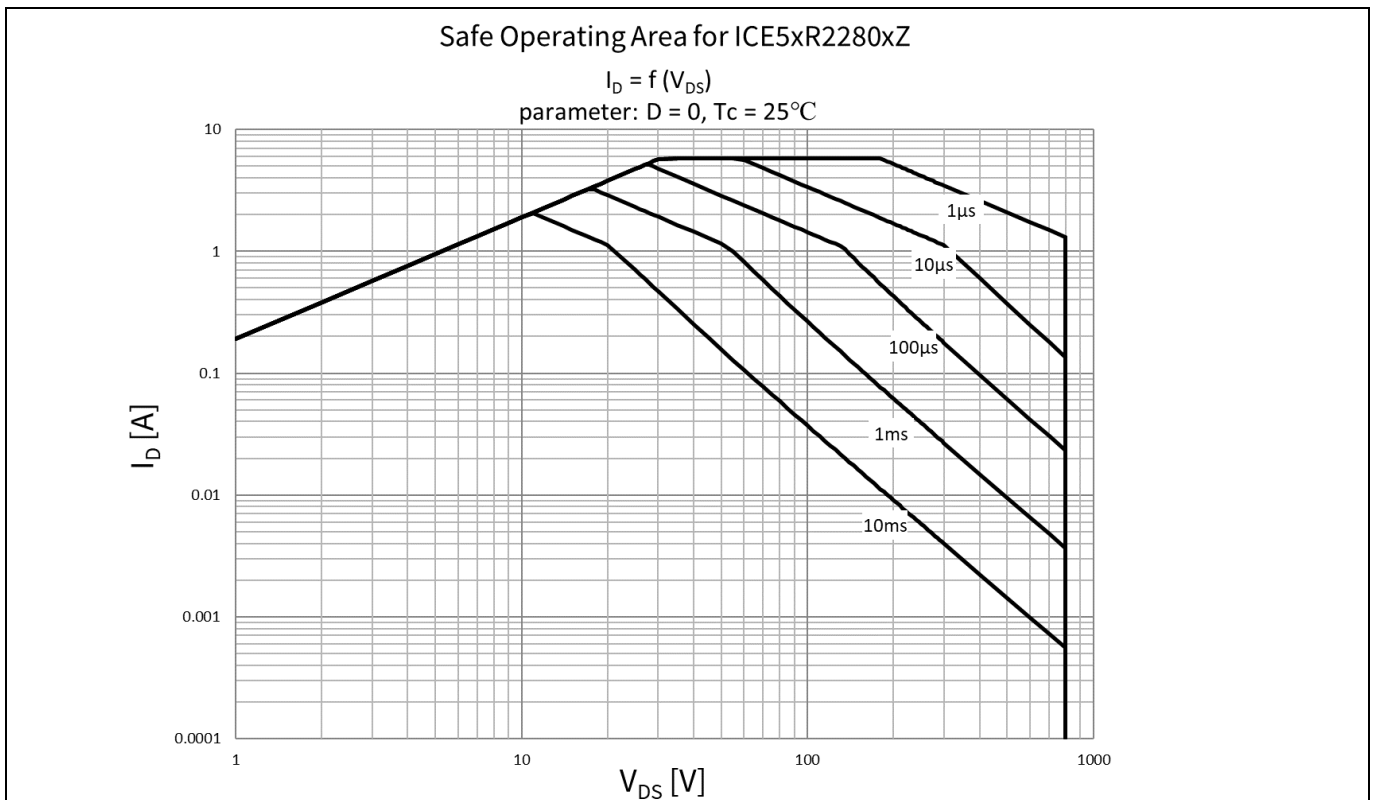
Figure 19   Safe operating area (SOA) curve for ICE5xR2280xZ

Figure 20   Safe operating area (SOA) curve for ICE5xR3995xZ
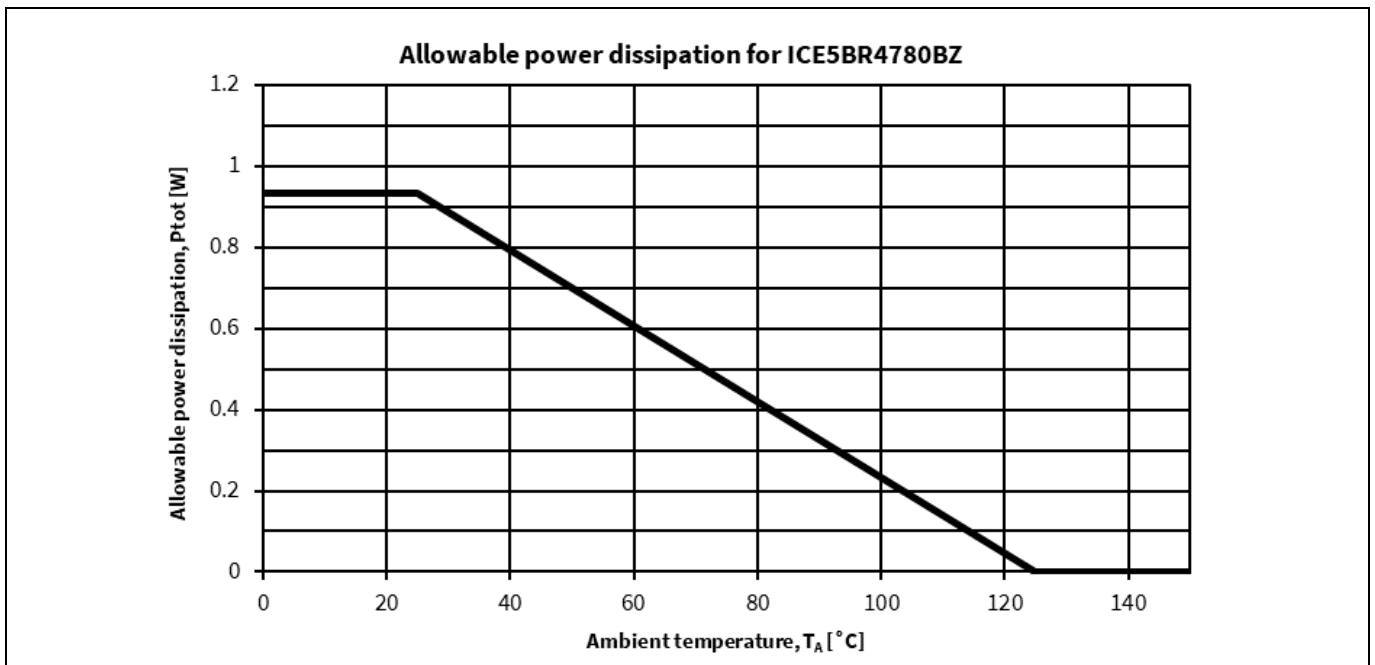
Figure 21   Power dissipation of ICE5BR4780BZ; P_{tot} = f(T_a) (Maximum ratings as given in chapter 4.1 must not be exceeded)
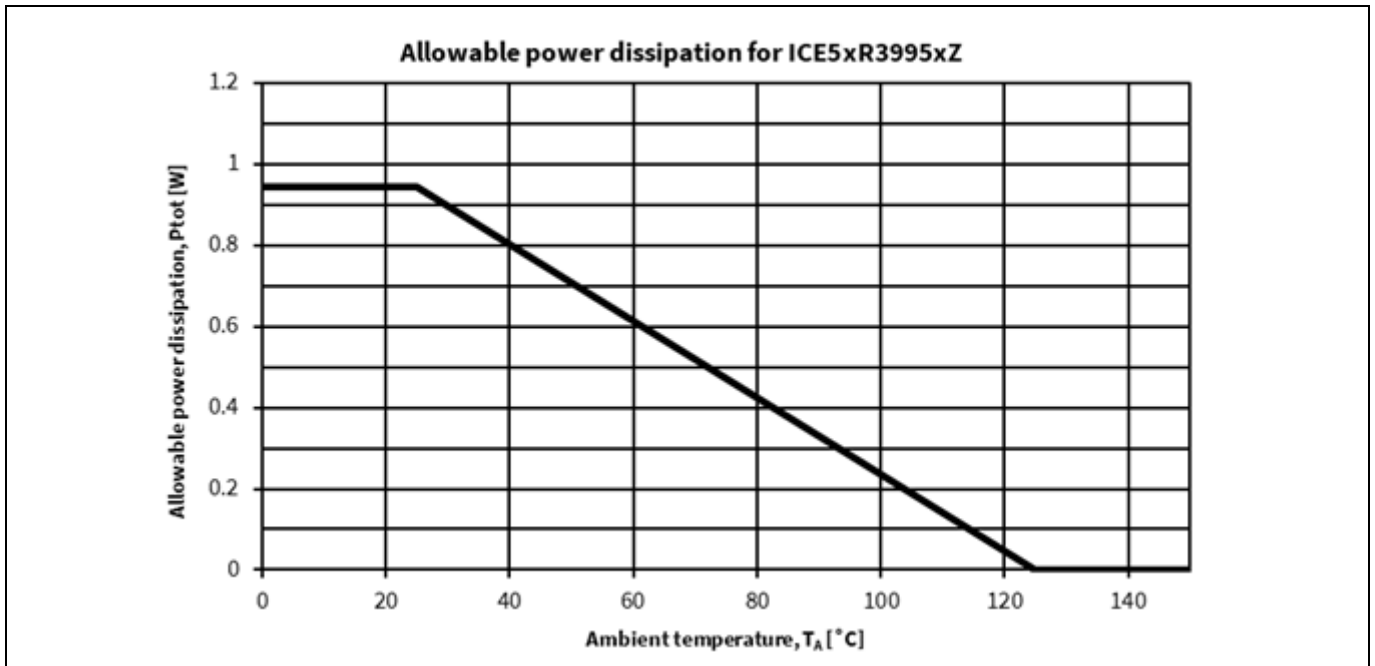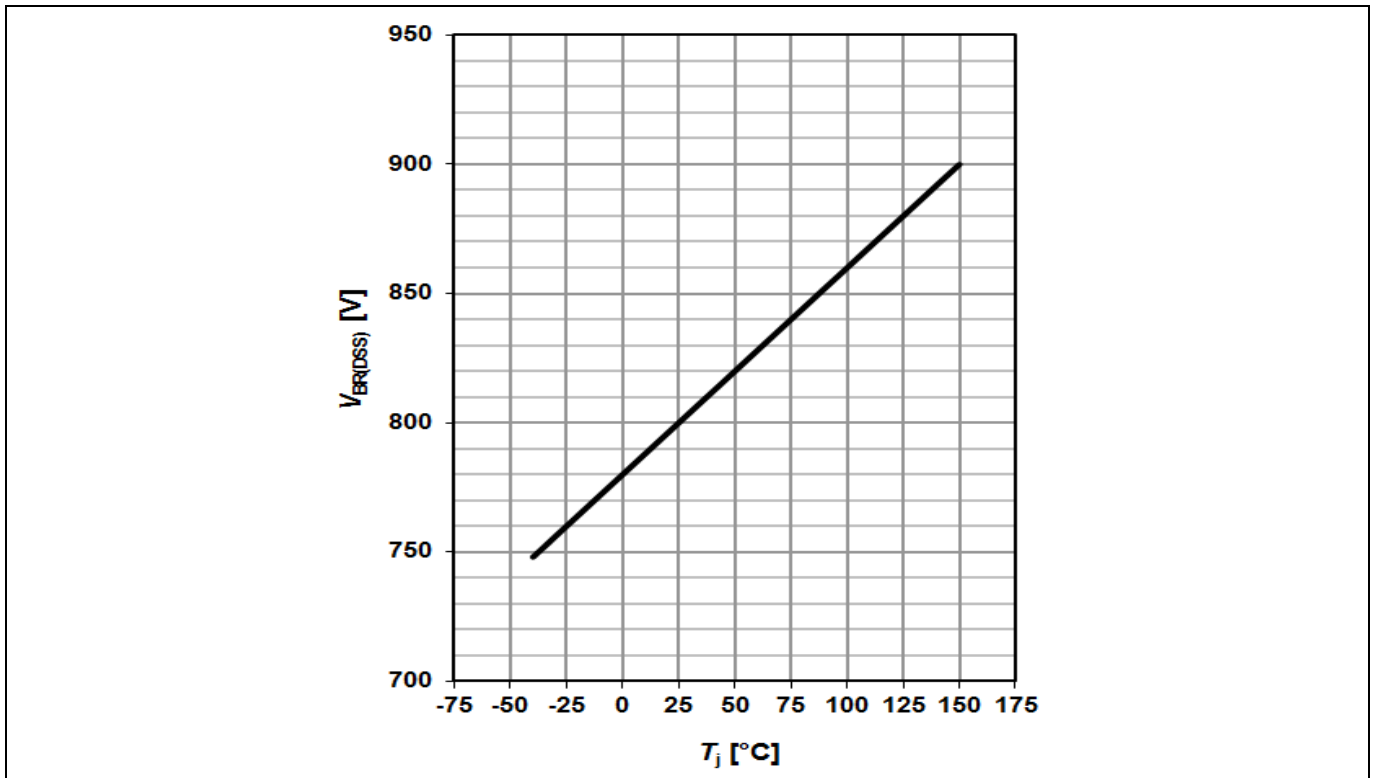
Figure 22 Power dissipation of ICE5xR3995xZ; P_{tot} = f(T$_a$) (Maximum ratings as given in chapter 4.1 must not be exceeded)
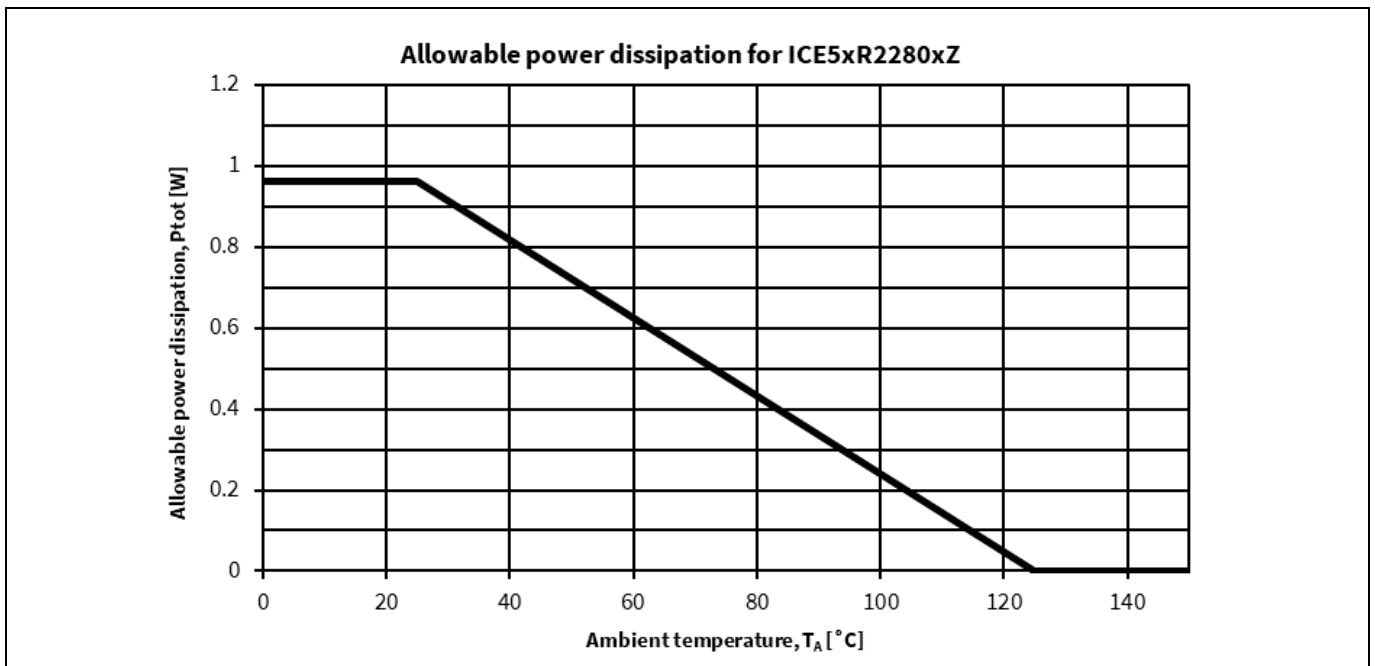
Figure 23 Power dissipation of ICE5xR2280xZ; P_{tot} = f(T$_a$) (Maximum ratings as given in chapter 4.1 must not be exceeded)

Figure 24   Drain-source breakdown voltage ICE5xRxx80xZ; $V_{BR(DSS)}$ = f(T$_J$), I_D = 1 mA
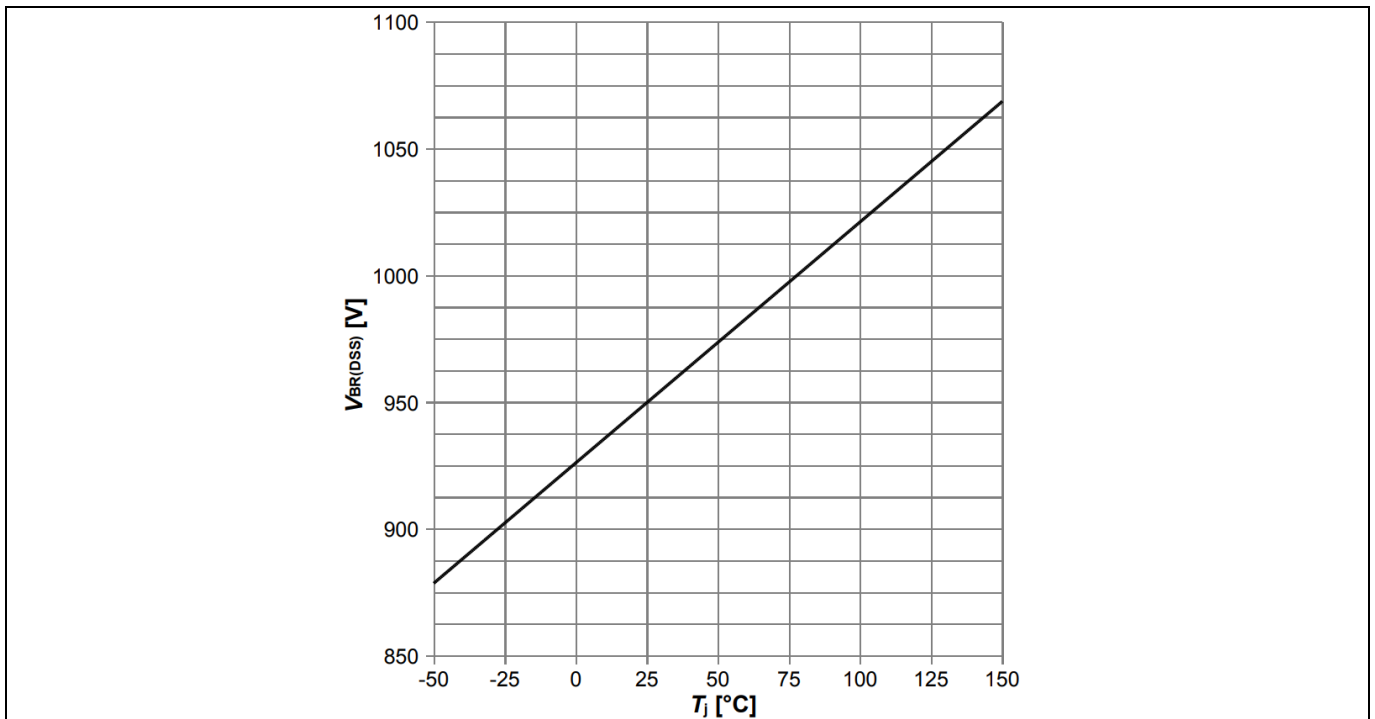
Figure 25   Drain-source breakdown voltage ICE5xR3995xZ; $V_{BR(DSS)}$ = f(T$_J$), I_D = 1 mA

CoolMOS™ performance characteristics
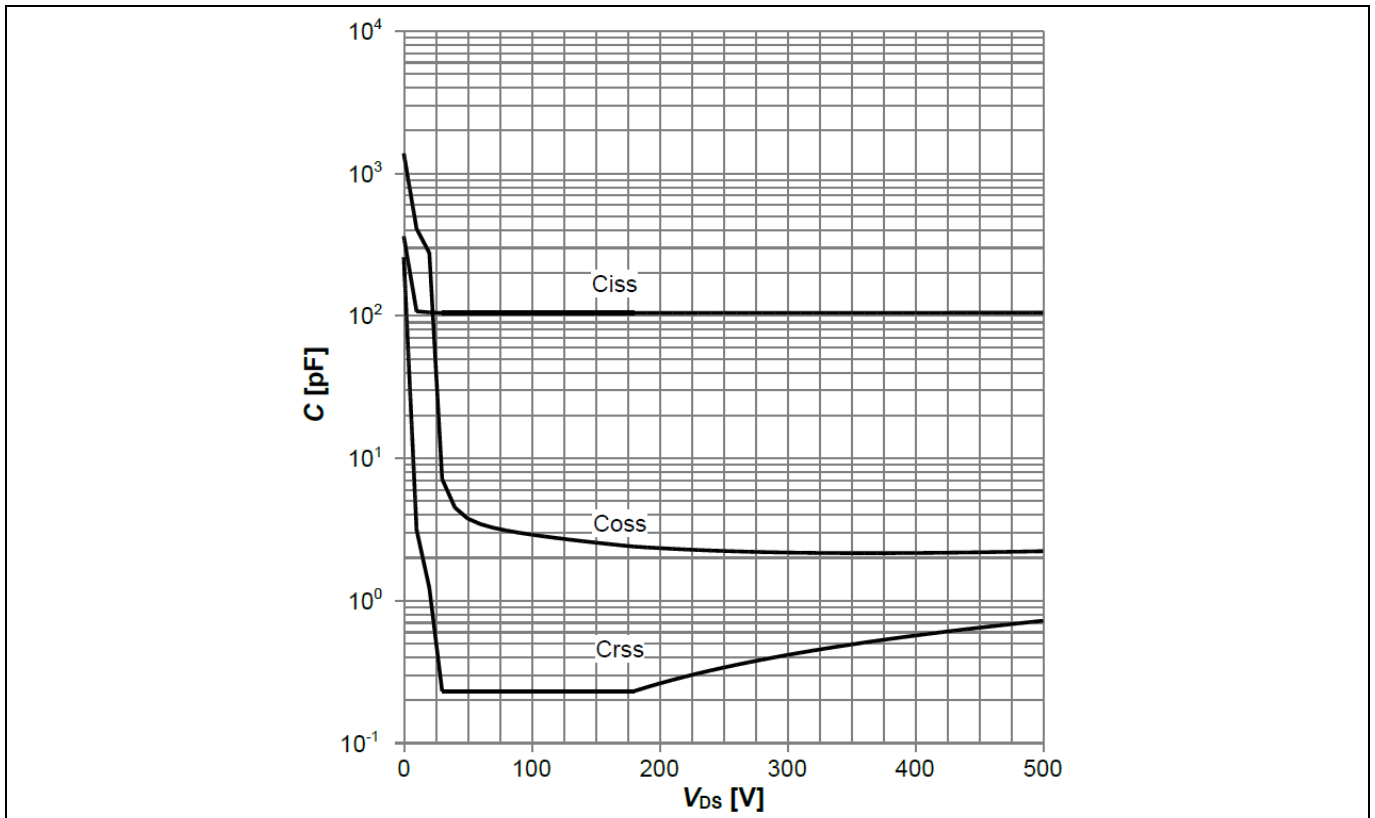
Figure 26   Typical CoolMOS™ capacitances of ICE5BR4780BZ (C = f(V_{DS}); V_{GS} = 0 V; f = 250 kHz)
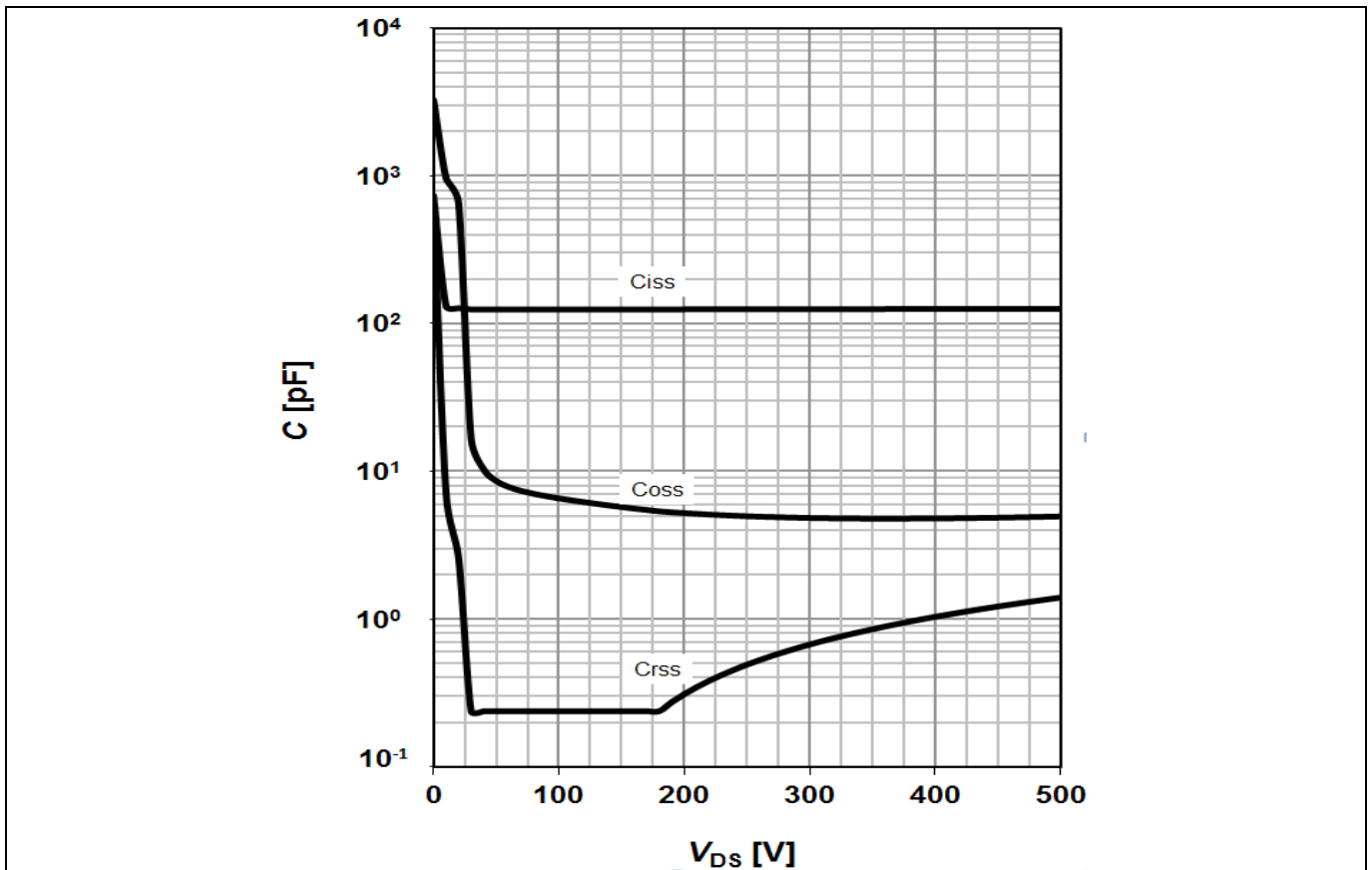
Figure 27   Typical CoolMOS™ capacitances of ICE5xR2280xZ (C = f(V_{DS}); V_{GS} = 0 V; f = 250 kHz)

CoolMOS™ performance characteristics
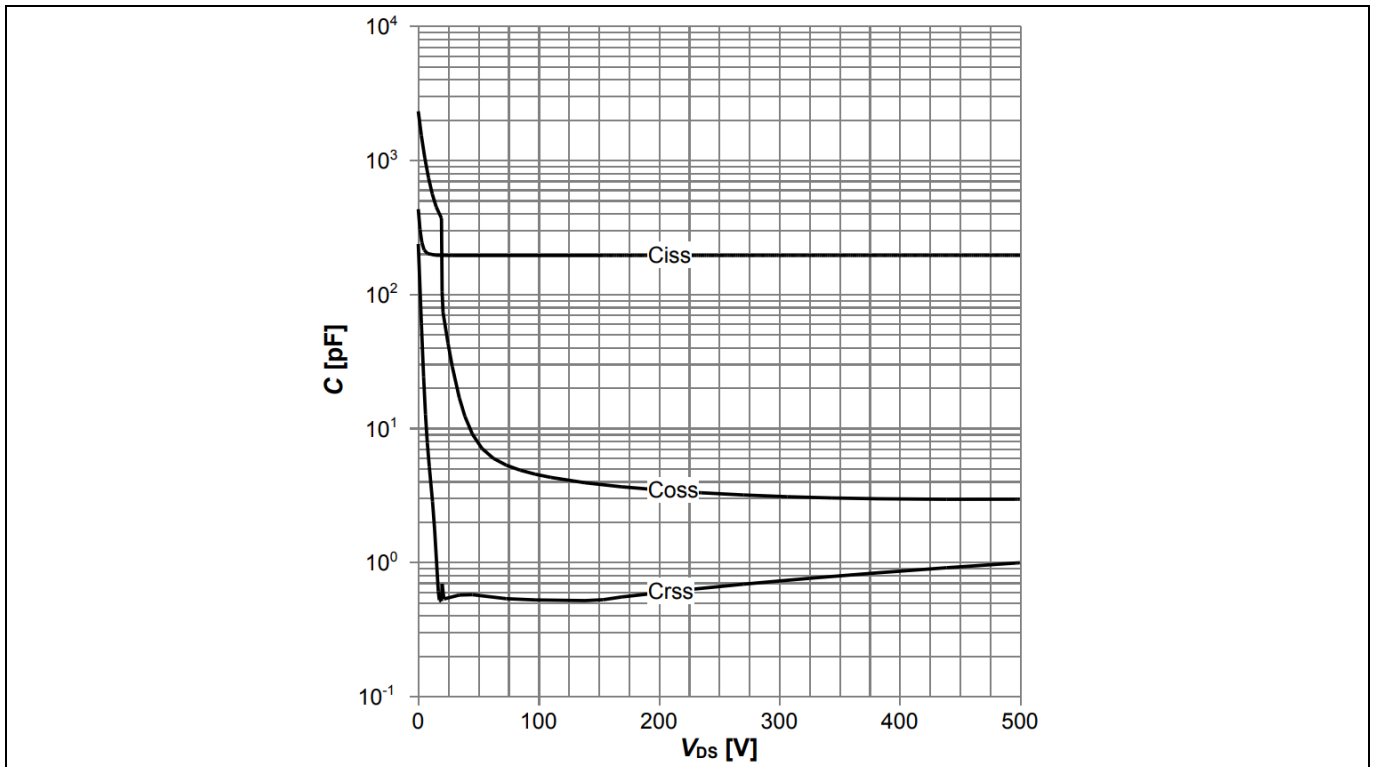
Figure 28 **Typical CoolMOS™ capacitances of ICE5xR3995xZ (C = f(V_{DS}); V_{GS} = 0 V; f = 250 kHz)**

6 Output power curve

The calculated output power curves versus ambient temperature are shown below. The curves are derived based on a typical DCM/CCM flyback in an open frame design setting the maximum T_j of the integrated CoolMOS™ at 125°C, using minimum drain pin copper area in a 2 oz copper single-sided PCB and steady state operation only (no design margins for abnormal operation modes are included).

The output power figure is for selection purpose only. The actual power can vary depending on a particular design. In a power supply system, appropriate thermal design margins must be considered to make sure that the operation of the device is within the maximum ratings given in chapter **4.1**.
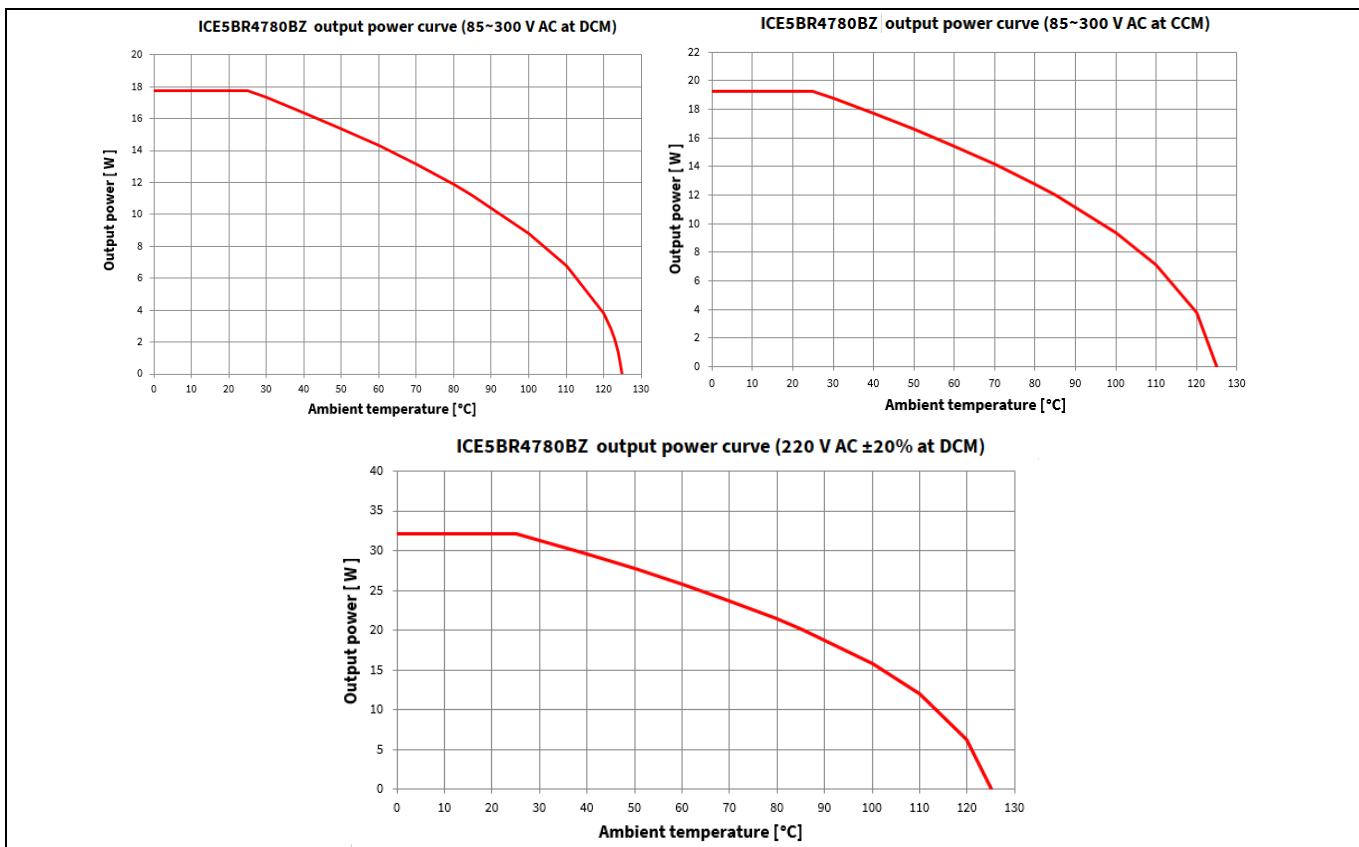
Figure 29   Output power curve of ICE5BR4780BZ

Output power curve
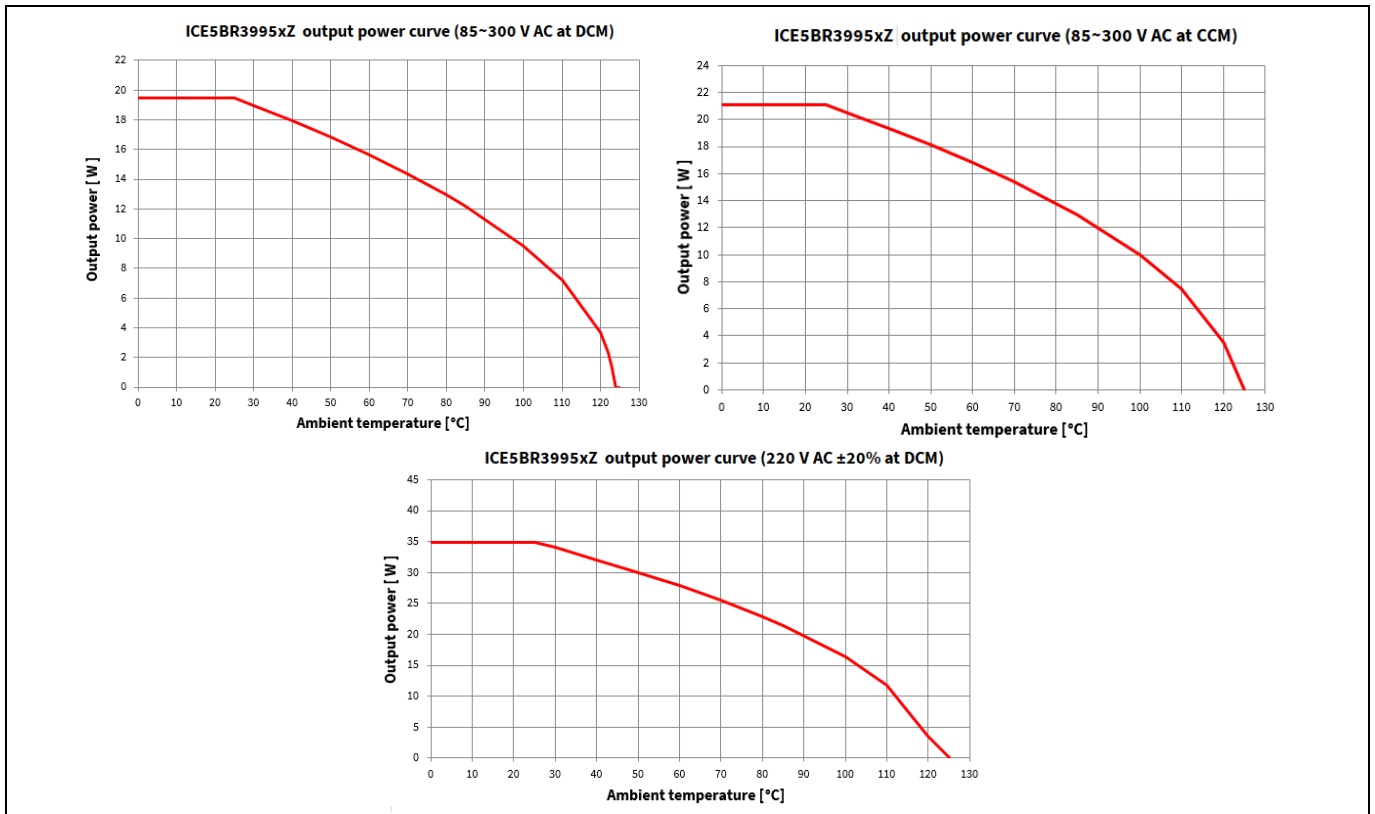
Figure 30   Output power curve of ICE5BR3995xZ
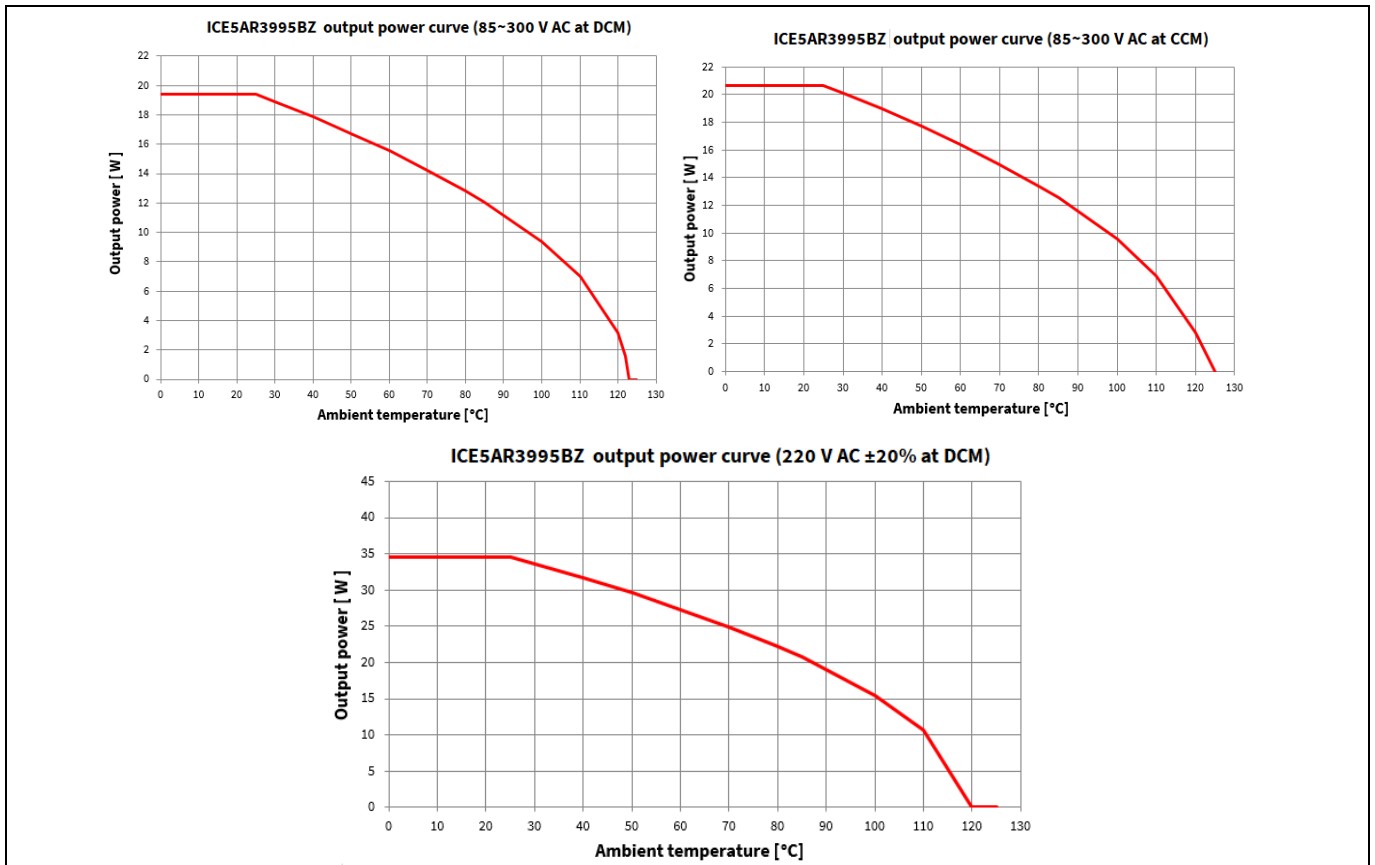
Figure 31   Output power curve of ICE5AR3995BZ
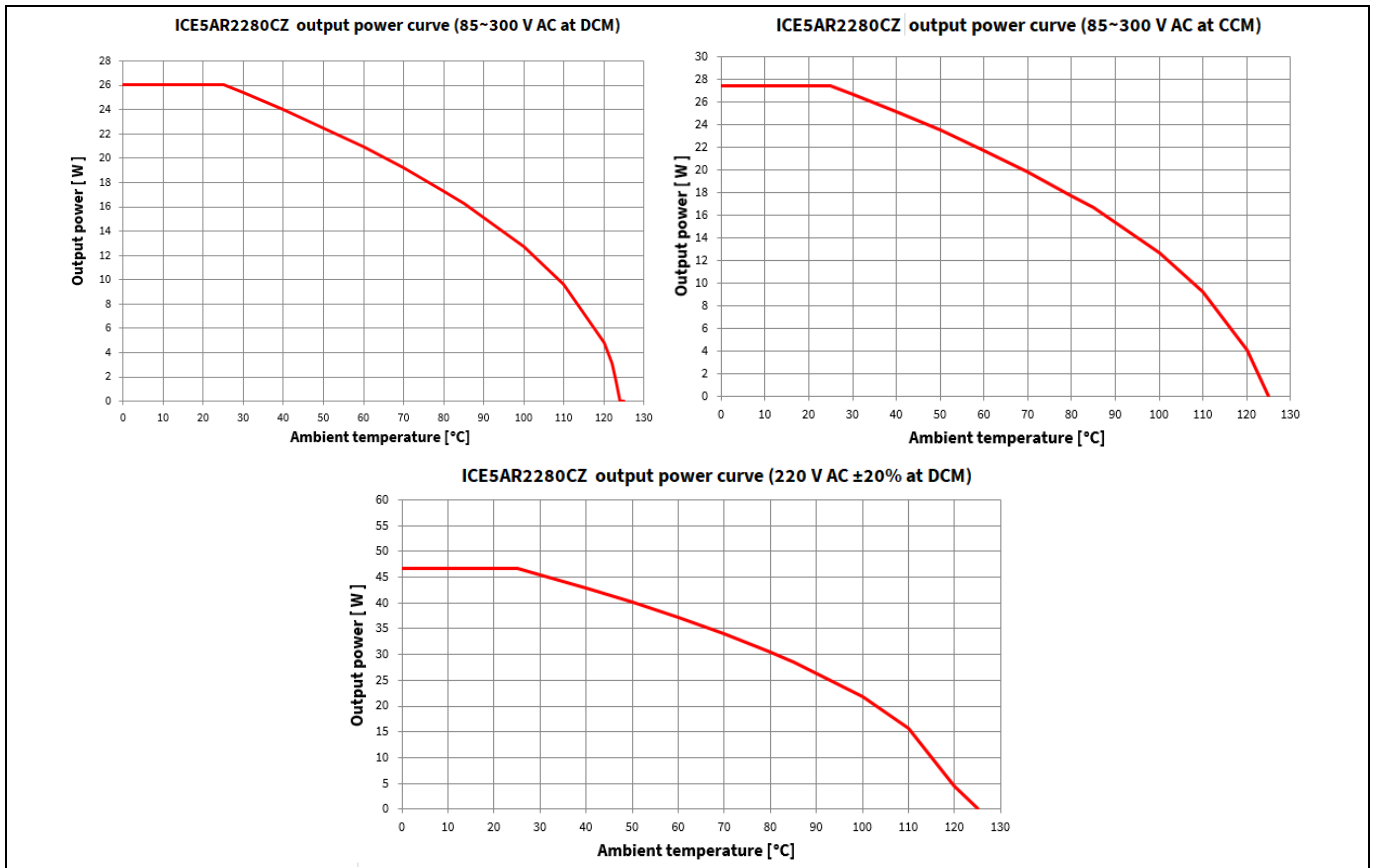
Output power curve

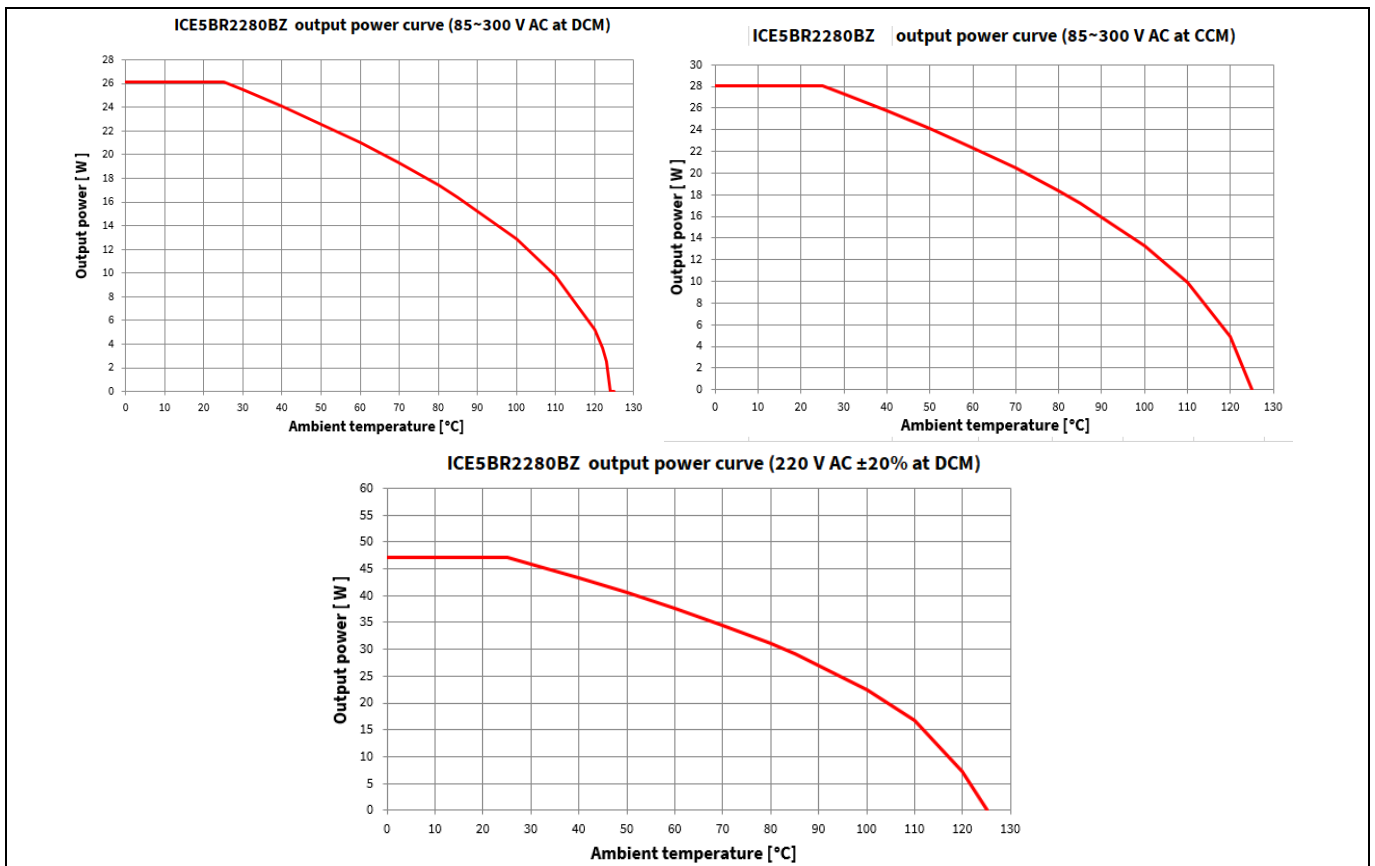**Figure 32   Output power curve of ICE5AR2280CZ**

Figure 33   Output power curve of ICE5BR2280BZ

7   Output current curve

The calculated output current curves showing typical output power against ambient temperature are shown below. The curves are derived based on an open-frame design at T_a = 50°C, T_J = 125°C (integrated HV MOSFET for CoolSET™), using the minimum 100 mm² drain pin copper area in a 2 oz copper single-sided PCB and steady-state operation only (no design margins for abnormal operation modes are included). The output power figure is for selection purposes only. The actual power can vary depending on the specific design.
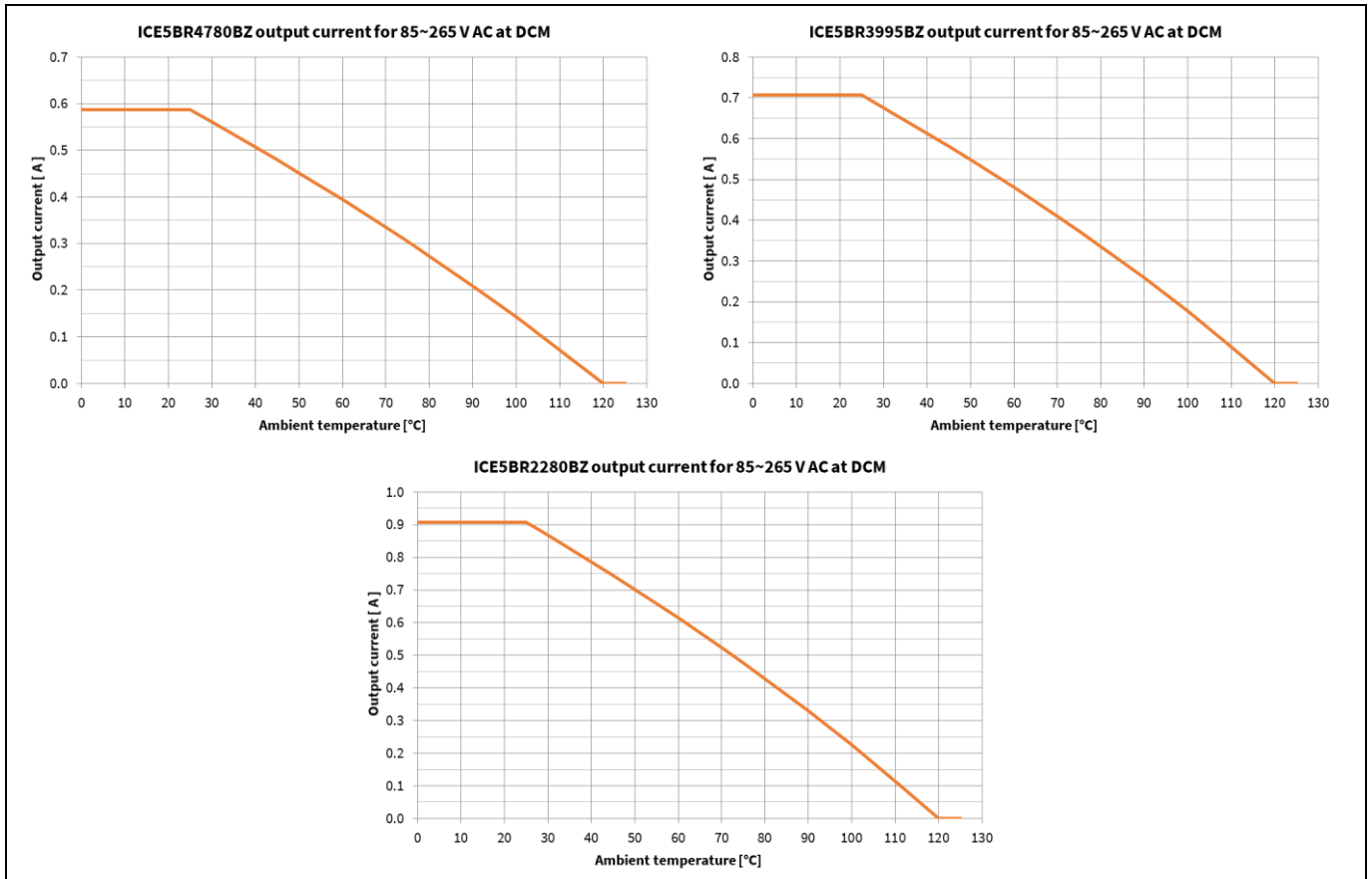

Figure 34   Output current curve of ICE5BRxxxxBZ

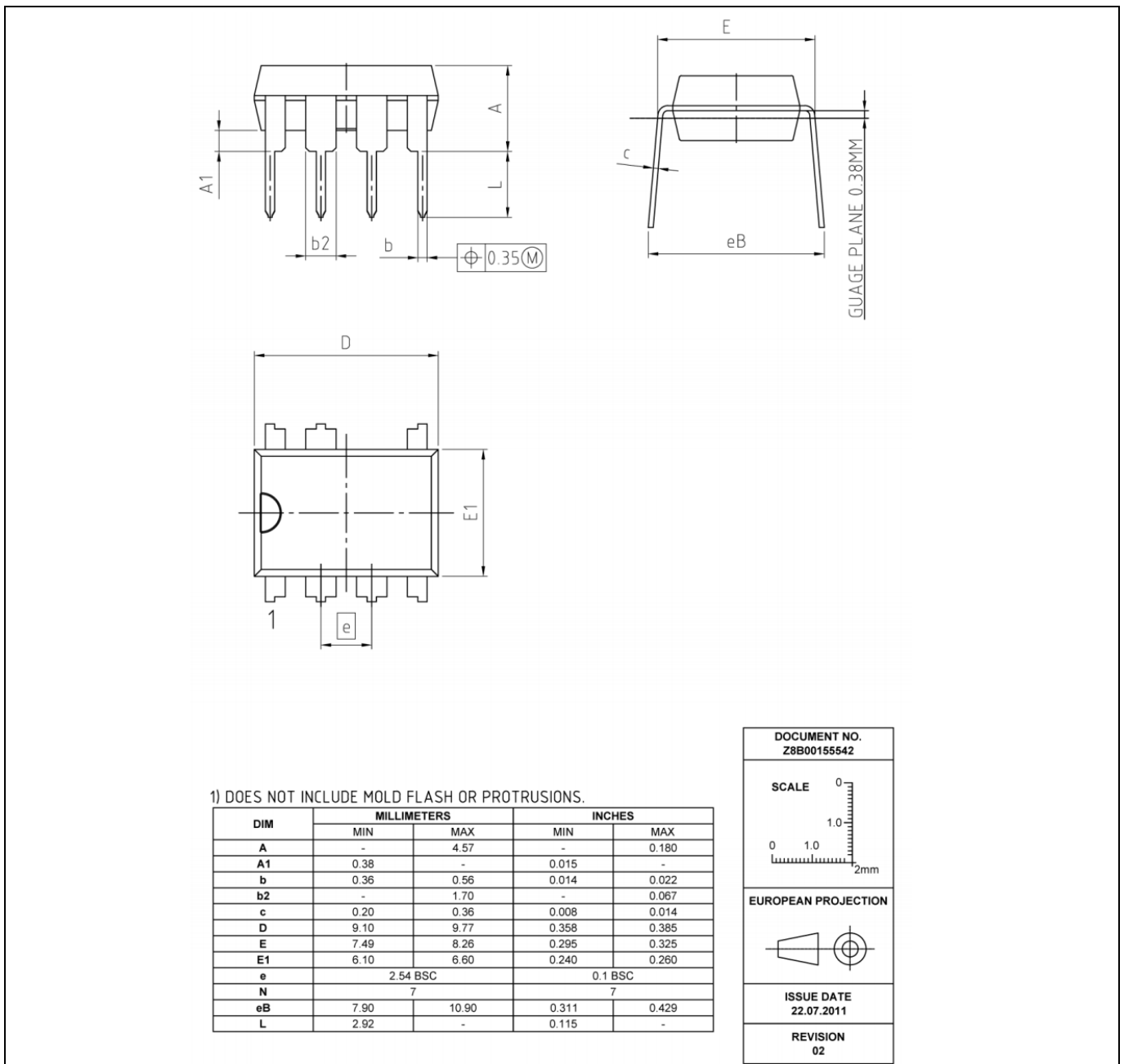# 8 Package information

Figure 35   PG-DIP-7

Green product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-compliant (i.e., Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).
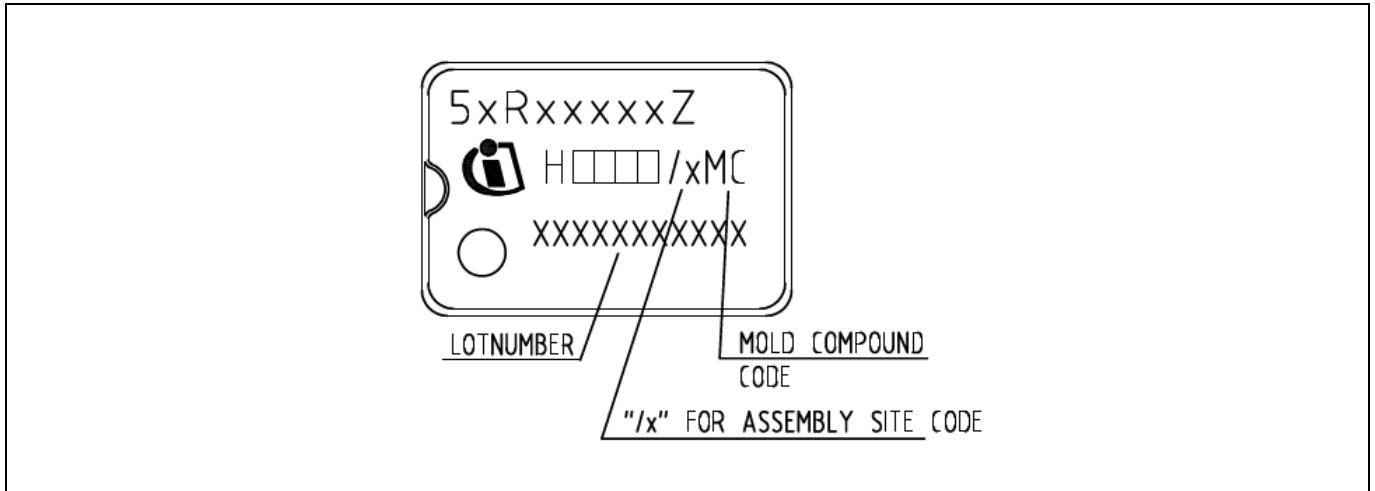
Further information on packages

https://www.infineon.com/packages

8.1 Marking

Figure 36   Marking of PG-DIP-7

9 Revision history

Revision	Date	Changes
Rev 1.0	22 February 2022	Initial release
Rev 1.1	19 July 2022	Add new part number - ICE5AR3995BZ

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