

MC74HC139A

Dual 1-of-4 Decoder/ Demultiplexer

High-Performance Silicon-Gate CMOS

The MC74HC139A is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit Address to one-of-four active-low outputs. Active-low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

Features

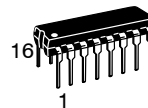
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



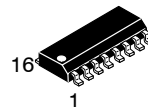
ON Semiconductor®

<http://onsemi.com>

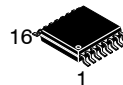
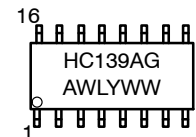
MARKING DIAGRAMS



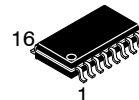
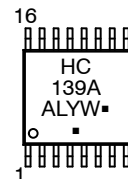
PDIIP-16
N SUFFIX
CASE 648



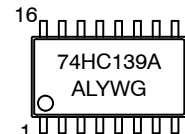
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74HC139A

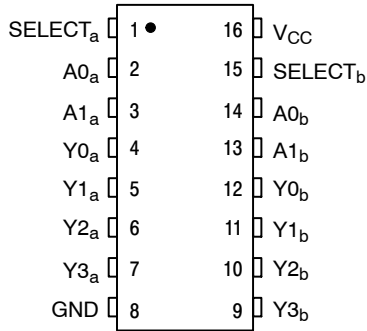


Figure 1. Pin Assignment

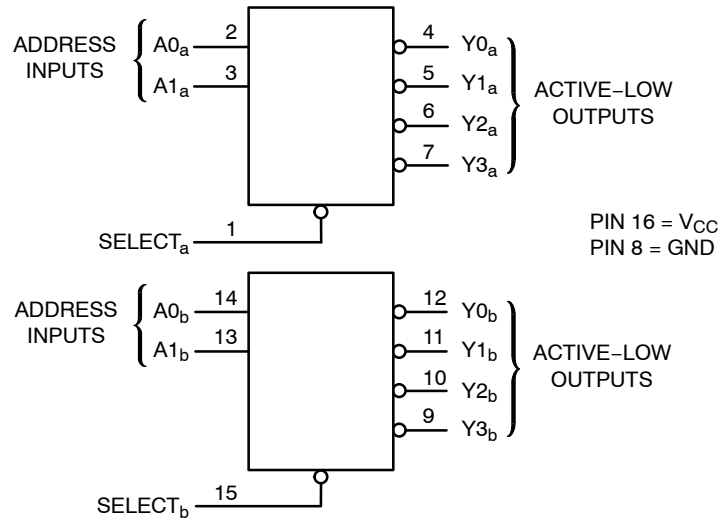


Figure 2. Logic Diagram

FUNCTION TABLE

Inputs			Outputs			
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC139ANG	PDIP-16 (Pb-Free)	2000 Units / Box
MC74HC139ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC139ADR2G	SOIC-16 (Pb-Free)	2500 Units / Reel
MC74HC139ADTR2G	TSSOP-16*	2500 Units / Reel
MC74HC139AFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	- 1.5 to V_{CC} + 1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND) (Note 1)	- 0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} Pin	± 50	mA
I_{GND}	DC Ground Current per Ground Pin	± 50	mA
T_{STG}	Storage Temperature Range	- 65 to + 150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$
T_J	Junction Temperature Under Bias	+ 150	$^{\circ}C$
θ_{JA}	Thermal Resistance	PDIP SOIC TSSOP	78 112 148 $^{\circ}C/W$
P_D	Power Dissipation in Still Air at 85 $^{\circ}C$	PDIP SOIC TSSOP	750 500 450 mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating	Oxygen Index: 30% - 35%	UL 94 V-0 @ 0.125 in
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 > 1000 V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 85 $^{\circ}C$ (Note 5)	± 300 mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	- 55	+ 125	$^{\circ}C$
t_r, t_f	Input Rise and Fall Time (Figure 3)	$V_{CC} = 2.0 V$ $V_{CC} = 4.5 V$ $V_{CC} = 6.0 V$	0 1000 500 400	ns

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC}	Guaranteed Limit			Unit
			V	-55°C to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.70	
6.0	5.48	5.34	5.20				
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.40	
6.0	0.26	0.33	0.40				
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0	4	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC}	Guaranteed Limit			Unit
		V	-55°C to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 1 and 3)	2.0	115	145	175	ns
		4.5	23	29	35	
		6.0	20	25	30	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 3)	2.0	115	145	175	ns
		4.5	23	29	35	
		6.0	20	25	30	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	-	10	10	10	pF

7. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Decoder) (Note 8)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		55	

8. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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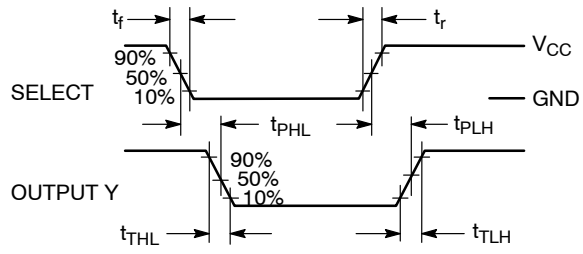


Figure 3. Switching Waveform

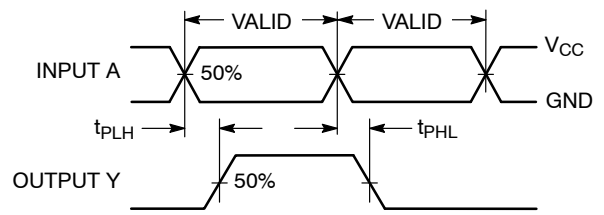
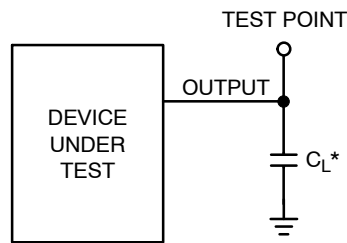


Figure 4. Switching Waveform



* Includes all probe and jig capacitance

Figure 5. Test Circuit

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PIN DESCRIPTIONS

ADDRESS INPUTS

A0_a, A1_a, A0_b, A1_b (Pins 2, 3, 14, 13)

Address inputs. These inputs, when the respective 1-of-4 decoder is enabled, determine which of its four active-low outputs is selected.

CONTROL INPUTS

Select_a, Select_b (Pins 1, 15)

Active-low select inputs. For a low level on this input, the outputs for that particular decoder follow the Address

inputs. A high level on this input forces all outputs to a high level.

OUTPUTS

Y0_a – Y3_a, Y0_b – Y3_b (Pins 4 – 7, 12, 11, 10, 9)

Active-low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

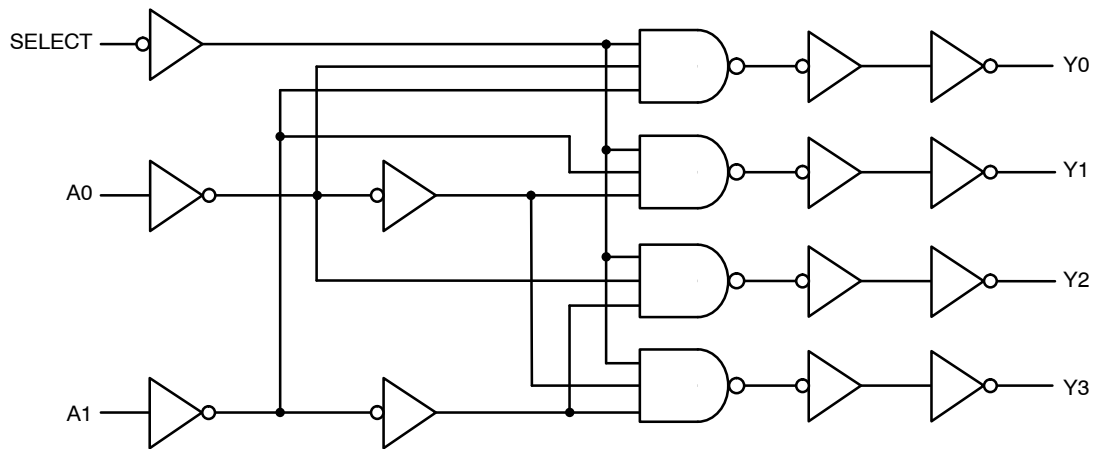
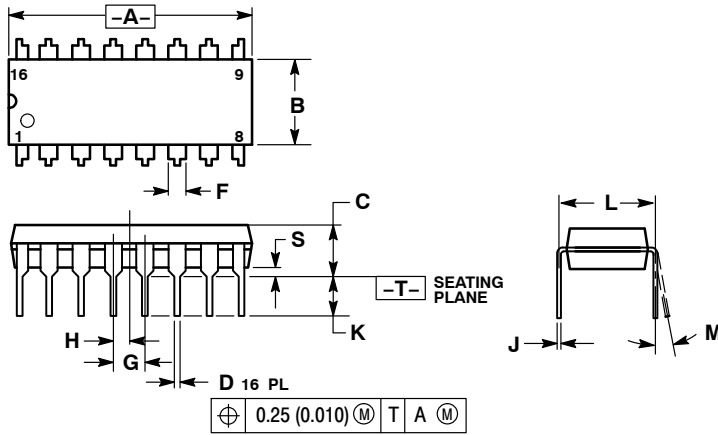


Figure 6. Expanded Logic Diagram
(1/2 of Device)

MC74HC139A

PACKAGE DIMENSIONS

PDIP-16
CASE 648-08
ISSUE T



NOTES:

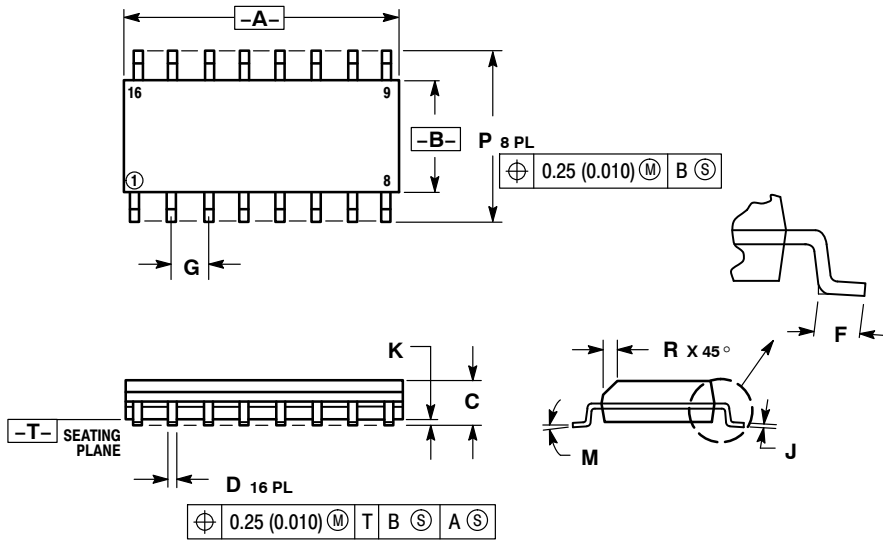
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

MC74HC139A

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

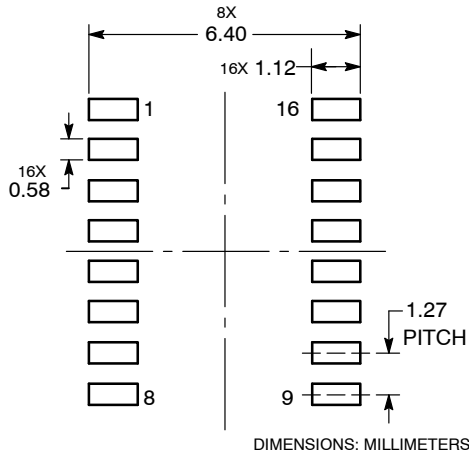


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° - 7°		0° - 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

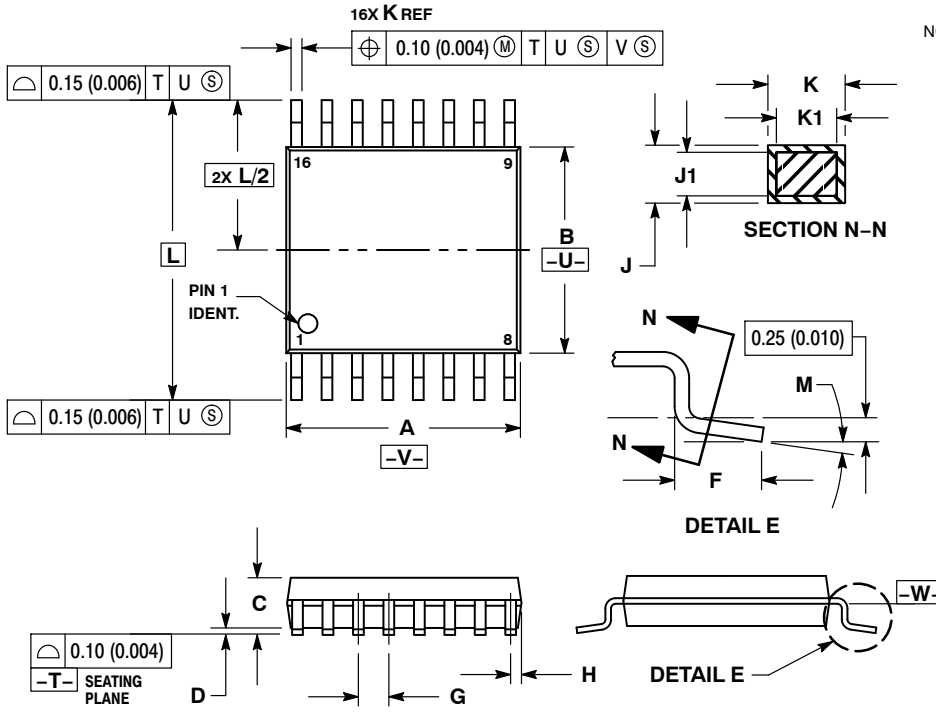
SOLDERING FOOTPRINT



MC74HC139A

PACKAGE DIMENSIONS

TSSOP-16
CASE 948F-01
ISSUE B

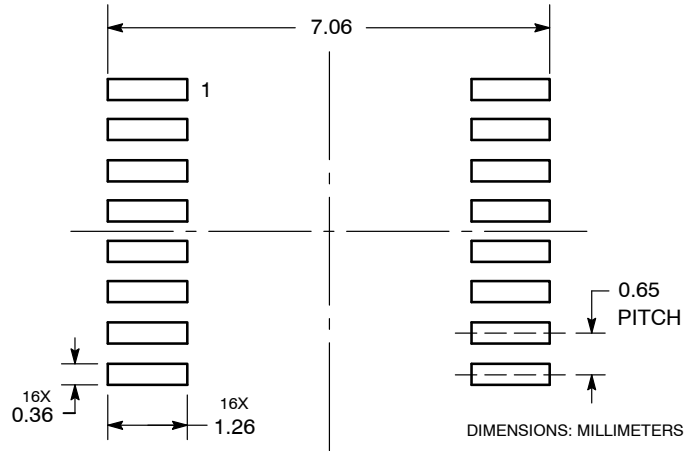


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

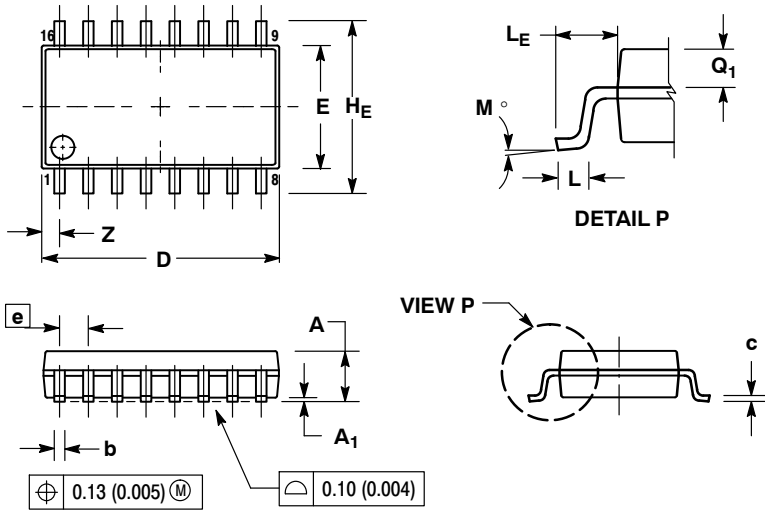
SOLDERING FOOTPRINT



MC74HC139A

PACKAGE DIMENSIONS

SOEIAJ-16
CASE 966-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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