NCP5368

Product Preview

Integrated Driver and MOSFET

The NCP5368 integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a 5 mm x 5 mm QFN package. The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP5368 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution and is designed to work with the NCP81111 controller.

Features

- Capable of Switching Frequencies of 5 MHz or Higher
- Capable of Output Currents up to 23 A, 40 A Pk
- Internal Bootstrap Diode
- Undervoltage Lockout
- SMOD Control turns off LS MOSFET
- These are Pb−Free Devices

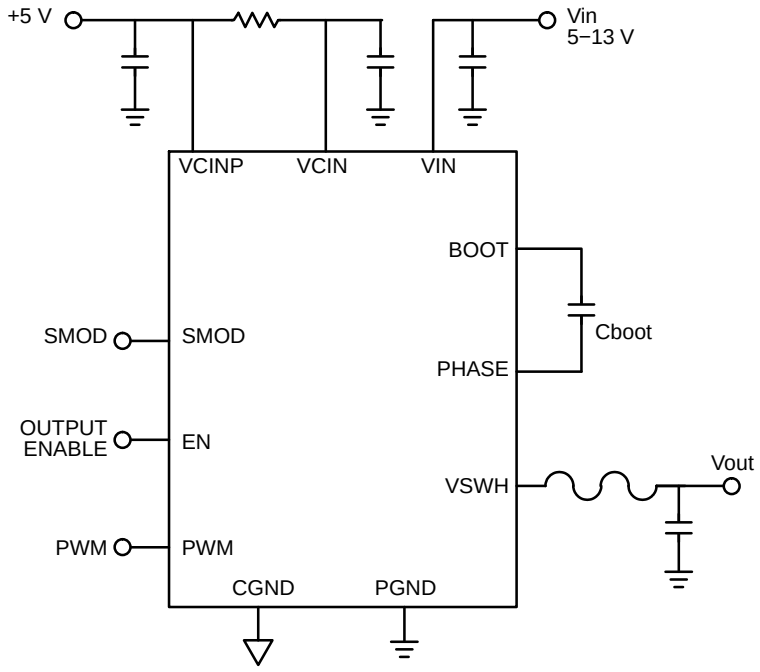

Figure 1. Application Schematic

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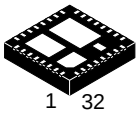
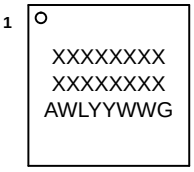


QFN32 5x5, 0.5P
CASE 485CY

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5368MNTXG	QFN32 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

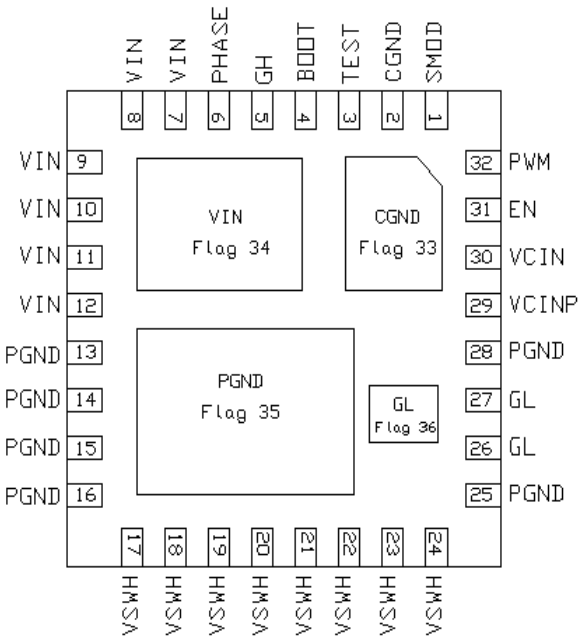


Figure 2. Pin Out
(Top View)

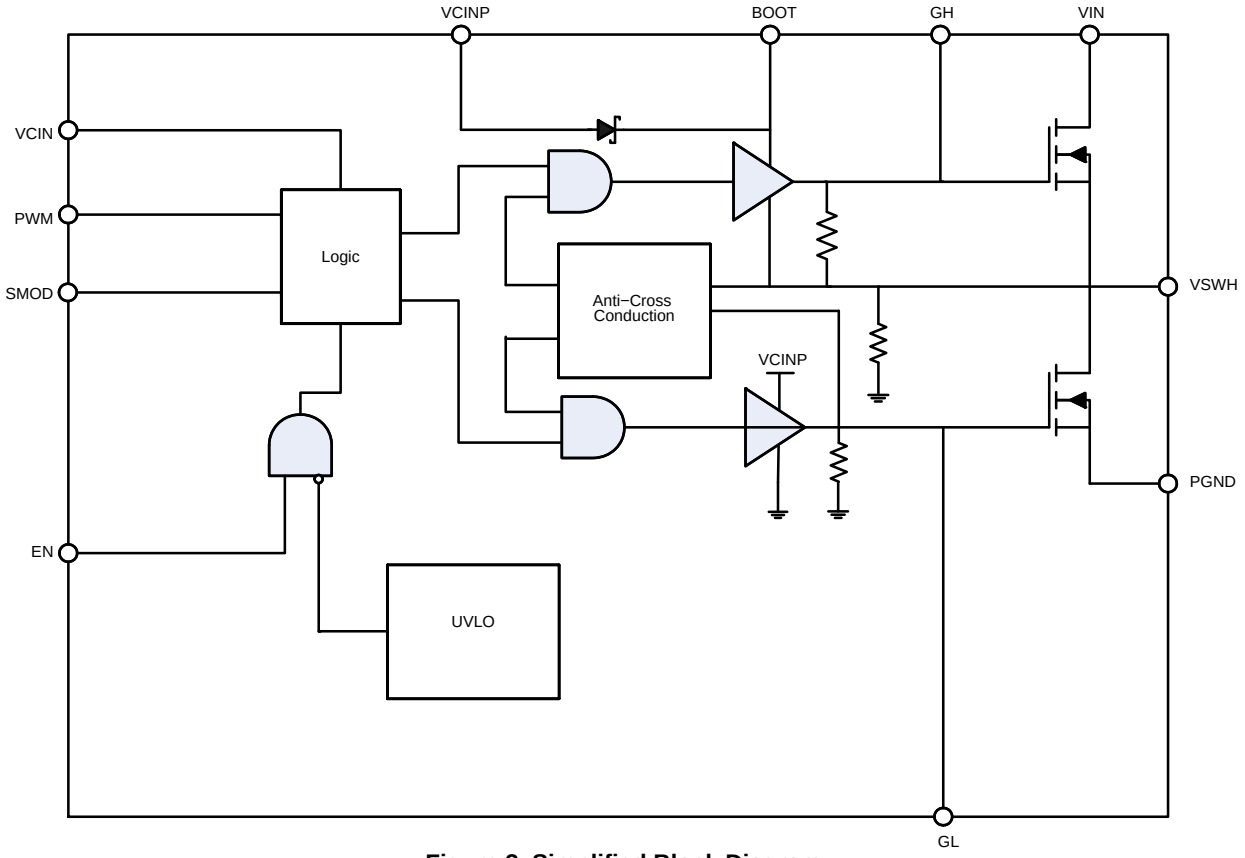


Figure 3. Simplified Block Diagram

PIN FUNCTION TABLE

Pin No.	Pin Name	Description
29	VCINP	Power for Driver
30	VCIN	Control Power for Driver
13−16, 25, 28, 35	PGND	Power Ground (Note: Pins 35 and 33 are solder pads on the Low Side FET and driver respectively)
4	BOOT	Bootstrap Voltage
5	GH	High Side FET Gate Access
6	PHASE	Provides a return path for the high side driver of the internal IC. Place a high frequency ceramic capacitor of 0.1 μF to 1.0 μF from this pin to BOOT pin.
7−12, 34	VIN	Input Voltage (Note: Pin 34 is the solder pad of the high side FET)
17−24	VSWH	Switch Node Output
26−27,36	GL	Low−side FET Gate Access
1	SMOD	SMOD Control Input
2,33	CGND	Control Ground
31	EN	Enable Input
32	PWM	PWM Control Input
3	TEST	Test Mode

ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	Min	Max
VCIN	Control Input Voltage	−0.3 V	6.5 V
VCINP	Low−Side Gate Driver Power	−0.3 V	6.5 V
VIN	Power Input Voltage	−0.3 V	15 V
BOOT	Bootstrap Voltage	−0.3 V wrt/VSWH	22 V wrt/PGND 30 V < 50 ns wrt/PGND 6.5 V wrt/VSWH
VSWH	Switch Node Output	−0.3 V	15 V 25 V < 5 ns
PWM	PWM Drive Logic	−0.3 V	6.5 V
EN	Enable	−0.3 V	6.5 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, High−Side FET	$R_{\Theta JPCB}$	2.8	°C/W
Thermal Resistance, Low−Side FET	$R_{\Theta JPCB}$	3.0	°C/W
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_S	−55 to 150	°C
Moisture Sensitivity Level	MSL	3	

OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
Control Input Voltage	VCIN	4.5	5	5.5	V
Low−Side Gate Driver Power	VCINP	4.5	5	5.5	V
Input Voltage	VIN	4.5	5	13	V

ELECTRICAL CHARACTERISTICS

(Note 1) (VCIN = 5 V, VIN = 5 V, T_A = −10°C to +100°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CURRENT						
VCIN Current (normal mode)		EN = 5V, PWM = OSC, FSW = 5 MHz		55		mA
VCIN Current (shutdown mode)		EN = GND		15	30	μA
UNDERVOLTAGE LOCKOUT						
UVLO Startup			3.6	3.75	3.9	V
UVLO Hysteresis			150	200	250	mV
BOOTSTRAP DIODE						
Forward Voltage		VCIN = 5 V, forward bias current = 2 mA	0.1	0.4	0.6	V
PWM INPUT						
PWM Input Voltage High	V_{PWM_HI}		4.0			V
PWM Input Voltage Hysteresis				1.3		V
PWM Input Voltage Low	V_{PWM_LO}				1.0	V
PWM Input Leakage					50	nA
PWM Input High to SWN High Delay		VCIN = 5 V		12		ns
PWM Input Low to SWN Low Delay		VCIN = 5 V		10		ns
EN						
Input Voltage High	V_{EN_HI}		4.0			V
Hysteresis	V_{EN_LO}			1.3		V
Input Voltage Low					1.0	V
Output Disable Leakage					50	nA
Low to SWN Open Delay		VCIN = 5 V		8.0		ns
SMOD INPUT						
Input Voltage High	V_{EN_HI}		4.0			V
Hysteresis	V_{EN_LO}			1.3		V
Input Voltage Low					1.0	mV
Leakage					50	nA
Low to Bottom Gate Low Delay		VCIN = 5 V		6.0		ns

1. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

APPLICATIONS INFORMATION

Theory of Operation

The NCP5368 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. With EN and SMOD in an enabled state, a single PWM input signal is all that is required to properly drive the high−side and low−side MOSFETs.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCINP and PGND.

High−Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSWH) through the PHASE pin.

The bootstrap circuit is comprised of the internal diode and an external bootstrap capacitor. When the NCP5368 is starting up, the VSWH pin is at ground, so the bootstrap capacitor will charge up to VCIN through the bootstrap diode See Figure 1. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the VSWH pin will rise. When the high−side MOSFET is fully on, the switch node will be at 5 V, and the BST pin will be at 5 V plus the charge of the bootstrap capacitor (approaching 10 V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Power Supply Decoupling

The NCP5368 can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage (VCINP, VCIN) a low ESR capacitor should be placed near the power and ground pins. A 1 μF to 4.7 μF multi layer ceramic capacitor (MLCC) is usually sufficient, using multiple capacitors in parallel to minimize the inductance is recommended.

Input Pins

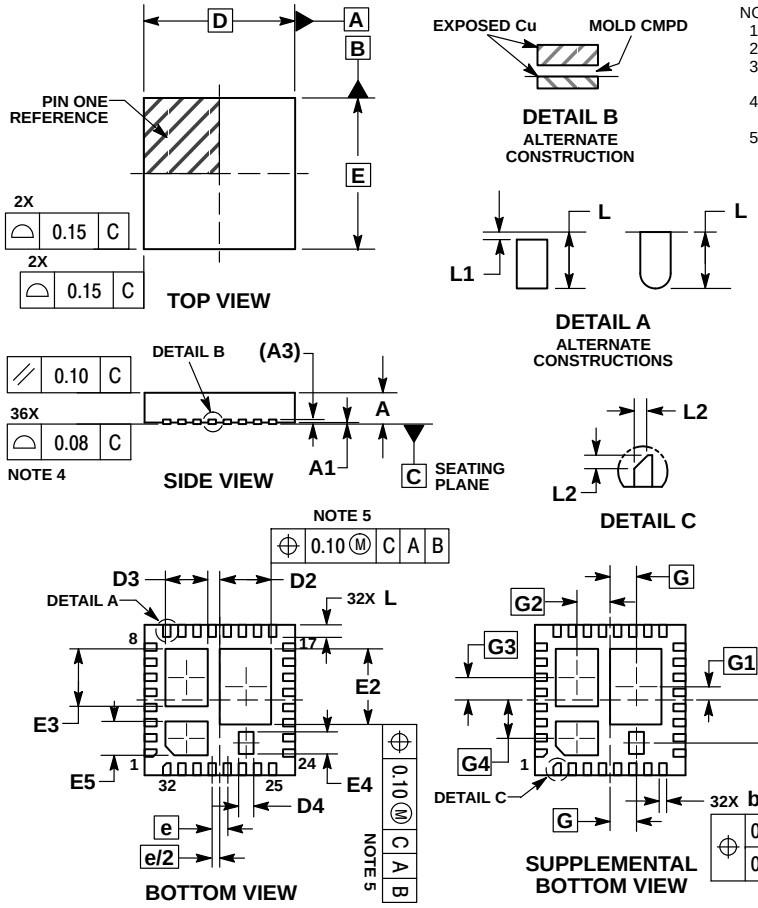
The PWM, EN, and the SMOD pins of the NCP5368 have internal protection for Electro Static Discharge (ESD), but in normal operation they present a relatively high input impedance. If the PWM controller does not have internal pull−down resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its under voltage lockout threshold.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal diode. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. A bootstrap capacitance greater than 10 nF and a minimum 50 V rating is recommended. A good quality ceramic capacitor should be used.

PACKAGE DIMENSIONS

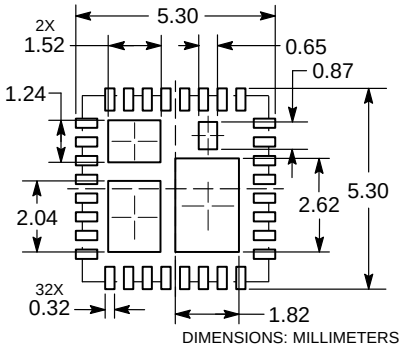
QFN32 5x5, 0.5P
CASE 485CY
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

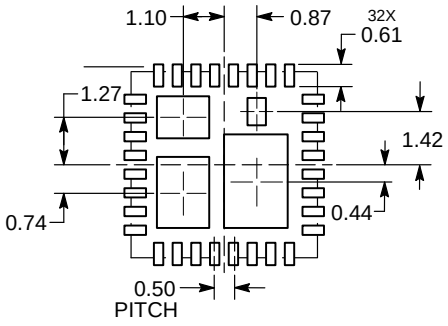
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	1.60	1.80
D3	1.30	1.50
D4	0.39	0.59
E	5.00 BSC	
E2	2.40	2.60
E3	1.80	2.00
E4	0.63	0.83
E5	1.02	1.22
e	0.50 BSC	
G	0.875 BSC	
G1	0.440 BSC	
G2	1.095 BSC	
G3	0.740 BSC	
G4	1.268 BSC	
G5	1.418 BSC	
L	0.30	0.50
L1	---	0.15
L2	0.13 REF	

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

RECOMMENDED SOLDERING FOOTPRINT SUPPLEMENTAL VIEW



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