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## 74ACTQ16373 16-Bit Transparent Latch with 3-STATE Outputs

### General Description

The ACTQ16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state. The ACTQ16373 utilizes Fairchild's Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control for superior performance.

### Features

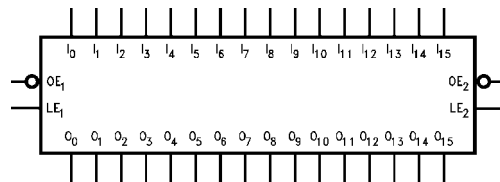
- Utilizes Fairchild FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Separate control logic for each byte
- 16-bit version of the ACTQ373
- Outputs source/sink 24 mA
- Additional specs for Multiple Output Switching
- Output Loading specs for both 50 pF and 250 pF loads

### Ordering Code:

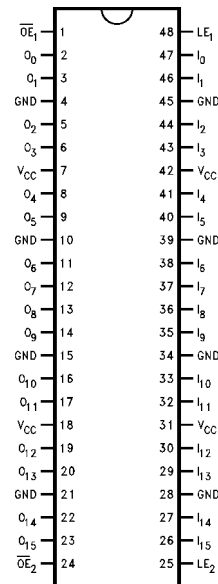
Order Number	Package Number	Package Description
74ACTQ16373SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACTQ16373MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$LE_n$	Latch Enable Input
$I_0-I_{15}$	Inputs
$O_0-O_{15}$	Outputs

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## Functional Description

The ACTQ16373 contains sixteen D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $D_n$  enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When  $LE_n$  is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of  $LE_n$ . The 3-STATE standard outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

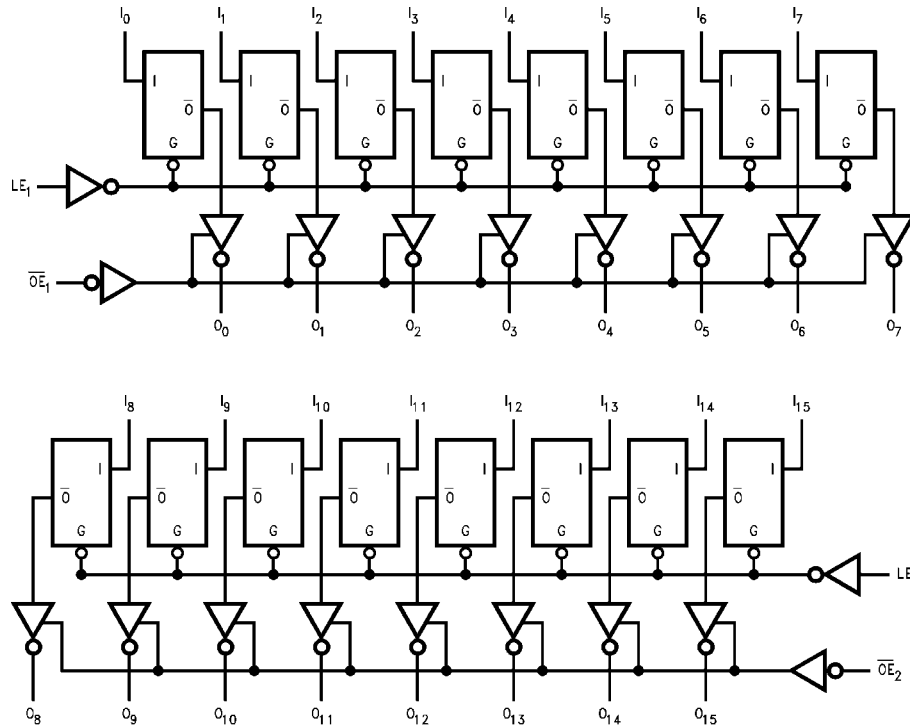
## Truth Tables

Inputs			Outputs
$LE_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

Inputs			Outputs
$LE_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	(Previous)

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 Previous = previous output prior to HIGH-to-LOW transition of LE

## Logic Diagrams



**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current ( $I_O$ )	+50 mA
DC $V_{CC}$ or Ground Current per Output Pin	+50 mA
Junction Temperature	+140°C
Storage Temperature	-65°C to +150°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0			
$V_{IL}$	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8			
$V_{OH}$	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4		V	$I_{OUT} = -50 \mu\text{A}$
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$
		5.5		4.86	4.76			$I_{OH} = -24 \text{ mA}$ (Note 2)
$V_{OL}$	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1		V	$I_{OUT} = 50 \mu\text{A}$
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$
		5.5		0.36	0.44			$I_{OL} = 24 \text{ mA}$ (Note 2)
$I_{OZ}$	Maximum 3-STATE Leakage Current	5.5		$\pm 0.5$	$\pm 5.0$		$\mu\text{A}$	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$		$\mu\text{A}$	$V_I = V_{CC}, \text{GND}$
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	5.5	0.6		1.5		mA	$V_I = V_{CC} - 2.1V$
$I_{CC}$	Max Quiescent Supply Current	5.5		8.0	80.0		mA	$V_{IN} = V_{CC}$ or GND
$I_{OLD}$	Minimum Dynamic Output Current (Note 3)	5.5			75		mA	$V_{OLD} = 1.65V$ Max
$I_{OHD}$					-75		mA	$V_{OHD} = 3.85V$ Min
$V_{OLP}$	Quiet Output	5.0	0.5	0.8			V	Figures 1, 2 (Note 5)(Note 6)
	Maximum Dynamic $V_{OL}$							
$V_{OLV}$	Quiet Output	5.0	-0.5	-1.0			V	Figures 1, 2 (Note 5)(Note 6)
	Minimum Dynamic $V_{OL}$							
$V_{OHP}$	Maximum Overshoot	5.0	$V_{OH} + 1.0$	$V_{OH} + 1.5$			V	Figures 1, 2 (Note 4)(Note 6)
$V_{OHV}$	Minimum $V_{CC}$ Droop	5.0	$V_{OH} - 1.0$	$V_{OH} - 1.8$			V	Figures 1, 2 (Note 4)(Note 6)
$V_{IHD}$	Minimum HIGH Dynamic Input Voltage Level	5.0	1.7	2.0			V	(Note 4)(Note 7)
$V_{ILD}$	Maximum LOW Dynamic Input Voltage Level	5.0	1.2	0.8			V	(Note 4)(Note 7)

**Note 2:** All outputs loaded; thresholds associated with output under test.

**Note 3:** Maximum test duration 2.0 ms; one output loaded at a time.

**Note 4:** Worst case package

**Note 5:** Maximum number of outputs that can switch simultaneously is n. (n - 1) outputs are switched LOW and one output held LOW.

**Note 6:** Maximum number of outputs that can switch simultaneously is n. (n - 1) outputs are switched HIGH and one output held HIGH.

**Note 7:** Max number of data inputs (n) switching, (n - 1) input switching 0V to 3V. Input under test switching 3V to threshold ( $V_{ILD}$ )

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	5.0	3.1	5.3	7.9	3.1	8.4	ns
t <sub>PHL</sub>	D <sub>n</sub> to O <sub>n</sub>		2.6	4.6	7.3	2.6	7.8	
t <sub>PLH</sub>	Propagation Delay	5.0	3.1	5.4	7.9	3.2	8.4	ns
t <sub>PHL</sub>	LE to O <sub>n</sub>		2.8	4.9	7.3	2.8	7.8	
t <sub>PZH</sub>	Output Enable	5.0	2.5	4.7	7.4	2.5	7.9	ns
t <sub>PZL</sub>	Delay		2.7	4.8	7.5	2.7	8.0	
t <sub>PHZ</sub>	Output Disable	5.0	2.1	5.1	7.9	2.1	8.2	ns
t <sub>PLZ</sub>	Delay		2.0	4.5	7.4	2.0	7.9	

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V.

## Extended AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF 16 Outputs Switching (Note 10)		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 250 pF (Note 11)		Units
			Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	5.0V	4.7	12.7	6.6	15.7	ns
t <sub>PHL</sub>	Data to Output		4.6	10.6	6.4	14.5	
t <sub>PLH</sub>	Propagation Delay	5.0V	4.6	13.3	6.3	15.3	ns
t <sub>PHL</sub>	Latch Enable to Output		4.1	10.4	5.8	13.6	
t <sub>PZH</sub>	Output Enable	5.0V	3.5	10.4	(Note 12)		ns
t <sub>PZL</sub>	Time		3.6	10.9			
t <sub>PHZ</sub>	Output Disable	5.0V	3.4	8.5	(Note 13)		ns
t <sub>PLZ</sub>	Time		3.1	8.1			
t <sub>OSSL</sub> (Note 14)	Pin-to-Pin Skew HL Data to Output	5.0V		1.3			ns
t <sub>OSLH</sub> (Note 14)	Pin-to-Pin Skew LH Data to Output	5.0V		2.1			ns
t <sub>OST</sub> (Note 14)	Pin-to-Pin Skew LH/HL Data to Output	5.0V		4.0			ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V.

Note 10: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 11: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 12: 3-STATE delays are load dominated and have been excluded from the datasheet.

Note 13: The Output Disable Time is dominated by the RC Network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t<sub>OSSL</sub>), LOW-to-HIGH (t<sub>OSLH</sub>), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t<sub>OST</sub>).

AC Operating Requirements					
Symbol	Parameter	V <sub>CC</sub> (V) (Note 15)	T <sub>A</sub> = +25°C	T <sub>A</sub> = -40°C to +85°C	Units
			C <sub>L</sub> = 50 pF	C <sub>L</sub> = 50 pF	
t <sub>S</sub>	Setup Time, HIGH or LOW, Input to Clock	5.0	3.0	3.0	ns
t <sub>H</sub>	Hold Time, HIGH or LOW Input to Clock	5.0	1.5	1.5	ns
t <sub>W</sub>	CS Pulse Width, HIGH or LOW	5.0	4.0	4.0	ns
<b>Note 15:</b> Voltage Range 5.0 is 5.0V ± 0.5V					
Capacitance					
Symbol	Parameter	Typ	Units	Conditions	
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0V	
C <sub>PD</sub>	Power Dissipation Capacitance	30	pF	V <sub>CC</sub> = 5.0V	

## FACT Noise Characteristics

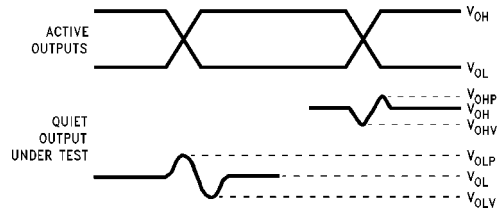
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

### Equipment:

Hewlett Packard Model 8180A Word Generator  
PC-163A Test Fixture  
Tektronics Model 7854 Oscilloscope

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



**Note A:**  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference.

**Note B:** Input pulses have the following characteristics:  $f = 1$  MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, skew  $< 150$  ps.

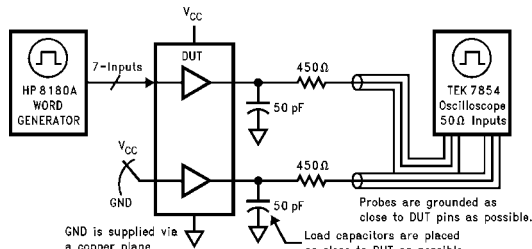
**FIGURE 1. Quiet Output Noise Voltage Waveforms**

$V_{OLP}/V_{OLV}$  and  $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the worst case transition for active and enable. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

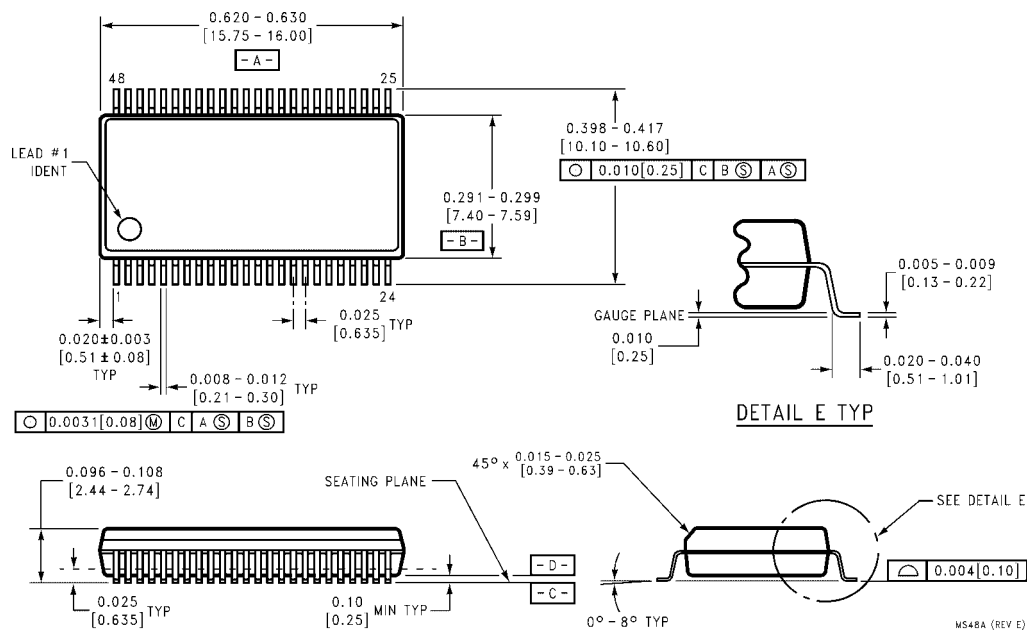
$V_{ILD}$  and  $V_{IHD}$ :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next decrease the input HIGH voltage level,  $V_{IH}$  until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.



**FIGURE 2. Simultaneous Switching Test Circuit**

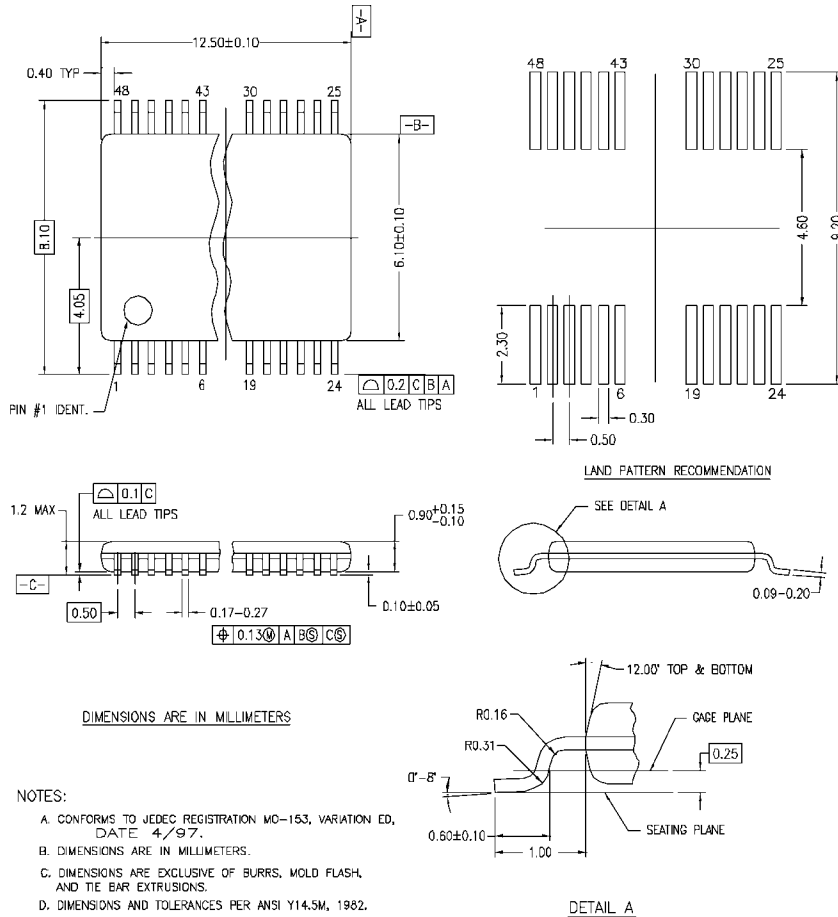
**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



MTD48REV C

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

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