NCV8660B

LDO Regulator - Very Low I_q, RESET, Delay Time Select

150 mA

The NCV8660B is a precision very low Iq low dropout voltage regulator. Quiescent currents as low as 28 μA typical make it ideal for automotive applications requiring low quiescent current with or without a load. Integrated control features such as Reset and Delay Time Select make it ideal for powering microprocessors.

It is available with a fixed output voltage of 5.0 V and 3.3 V and regulates within ±2.0%.

Features

- Fixed Output Voltage of 5 V and 3.3 V
- ±2.0% Output Voltage up to V_{BAT} = 40 V
- Output Current up to 150 mA
- Microprocessor Compatible Control Functions:
  - Delay Time Select
  - RESET Output
- NCV Prefix for Automotive
  - Site and Change Control
  - AEC−Q100 Qualified
- Low Dropout Voltage
- Low Quiescent Current of 28 μA Typical
- Stable Under No Load Conditions
- Protection Features:
  - Thermal Shutdown
  - Short Circuit
- These are Pb−Free Devices

Applications

- Automotive:
  - Body Control Module
  - Instrument and Clusters
  - Occupant Protection and Comfort
  - Powertrain
- Battery Powered Consumer Electronics

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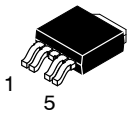
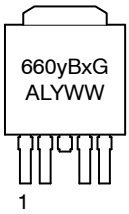
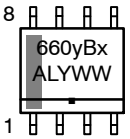
MARKING DIAGRAMS



DPAK 5−PIN
DT SUFFIX
CASE 175AA



SOIC−8 FUSED
CASE 751



x	= 5 for 5 V Output, 3 for 3.3 V Output
y	= 1 for 8 ms, 128 ms Reset Delay, = 2 for 8 ms, 32 ms Reset Delay = 3 for 16 ms, 64 ms Reset Delay = 4 for 32 ms, 128 ms Reset Delay
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 13 of this data sheet.

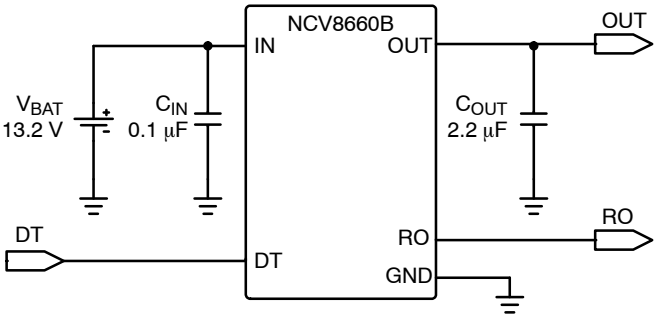


Figure 1. Application Diagram

PIN DESCRIPTIONS

Pin		Symbol	Function
DPAK	SOIC−8 FUSED		
1	1	IN	Input Supply Voltage. 0.1 μF bypass capacitor to GND at the IC.
2	2	R_O	Reset Output. CMOS compatible output. Goes low when V_{OUT} drops by more than 7% from nominal.
3, Tab	5−8	GND	Ground
4	3	DT	Reset Delay Time Select. Short to GND or connect to OUT to select time.
5	4	OUT	Regulated Voltage Output. 2.2 μF to ground for typical applications.

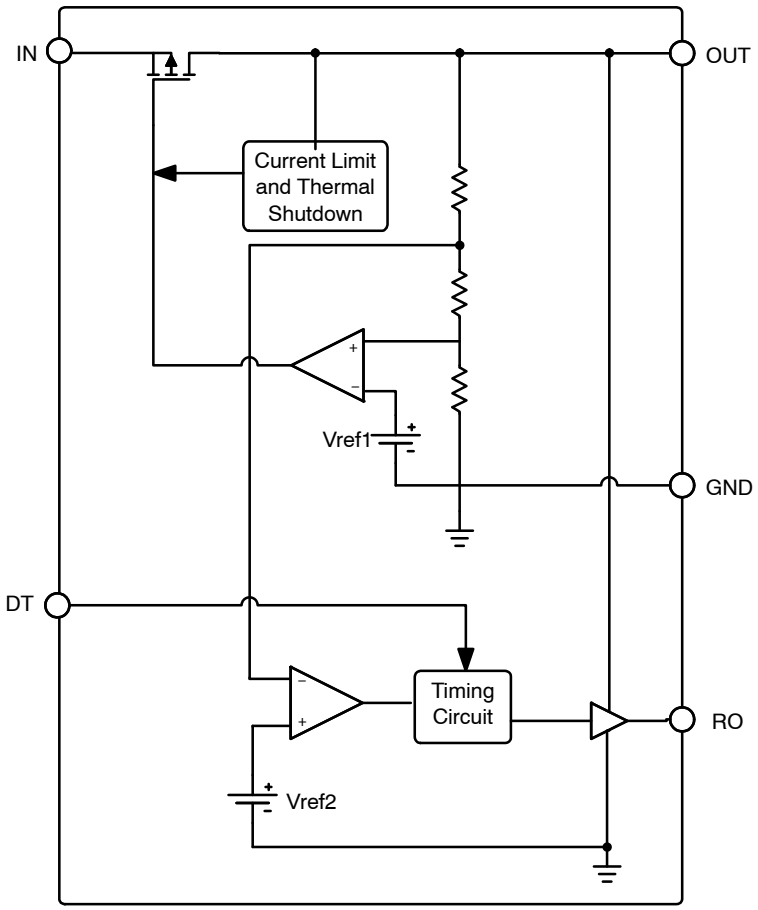


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage (IN)	V_{IN}	−0.3	40	V
Input Current	I_{IN}	−1.0	−	mA
Output Voltage (OUT) DC Transient, t < 10 s (Note 1)	V_{OUT}	 −0.3 −0.3	 5.5 16	V
Output Current (OUT)	I_{OUT}	−1.0	Current Limited	mA
Storage Temperature Range	T_{STG}	−55	150	°C
DT (Reset Delay Time Select) Voltage (Note 2)	V_{DT}	−0.3	16	V
DT (Reset Delay Time Select) Current (Note 2)	I_{DT}	−1.0	1.0	mA
RO (Reset Output) Voltage DC Transient, t < 10 s	V_{RO}	 −0.3 −0.3	 5.5 16	V
RO (Reset Output) Current	I_{RO}	−1.0	1.0	mA

ESD CAPABILITY

ESD Capability, Human Body Model (Note 3)	ESD_{HB}	−2.0	2.0	kV
ESD Capability, Machine Model (Note 3)	ESD_{MM}	−200	200	V
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	−1.0	1.0	kV

THERMAL RESISTANCE

Junction−to−Case (Note 4) DPAK 5	$R_{\theta JC}$	15		°C/W
Junction−to−Ambient (Note 4) DPAK 5	$R_{\theta JA}$	66		°C/W
Junction−to−Tab (Note 4) DPAK 5	$R_{\theta JT}$	4.0		°C/W
Junction−to−Ambient (Note 4) SOIC−8 FUSED	$R_{\theta JA}$	104		°C/W
Junction−to−Lead (pin 6) (Note 4) SOIC−8 FUSED	$R_{\theta JT}$	33		°C/W

LEAD SOLDERING TEMPERATURE AND MSL

Moisture Sensitivity Level DPAK 5 SOIC−8 FUSED	MSL	1 3		−
Lead Temperature Soldering: SMD style only, Reflow (Note 5) Pb−Free Part 60 − 150 sec above 217°C, 40 sec max at peak	SLD	−	265 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The output voltage must not exceed the input voltage.
2. External resistor required to minimize current to less than 1 mA when the control voltage is above 16 V.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD CDM tested per EIA/JESD22/C101, Field Induced Charge Model
4. Values represented typical steady−state thermal performance on 1 oz. copper FR4 PCB with 1 in^2 copper area.
5. Per IPC / JEDEC J−STD−020C.

OPERATING RANGE

Pin Symbol, Parameter	Symbol	Min	Max	Unit
V_{IN}, Input Voltage Operating Range	V_{IN}	4.5	40	V
Junction Temperature Range	T_J	−40	150	°C

ELECTRICAL CHARACTERISTICS 5.5 V < V_{IN} < 40 V, −40°C ≤ T_J ≤ +150°C, unless otherwise specified

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Quiescent Current	I_q	100μA < I_{OUT} < 150mA, V_{IN} = 13.2V, T_J = 25°C	–	25	30	μA
		100μA < I_{OUT} < 150mA, V_{IN} = 13.2V, T_J ≤ 85°C	–	–	40	
Thermal Shutdown (Note 6)	T_{SD}		150	175	195	°C
Thermal Hysteresis (Note 6)	T_{HYS}		–	25	–	°C
OUT						
Output Voltage	V_{OUT}	6 V ≤ V_{IN} ≤ 16 V, 0.1 mA ≤ I_{OUT} ≤ 150 mA	4.9	5.0	5.1	V
		6 V ≤ V_{IN} ≤ 40 V, 0.1 mA ≤ I_{OUT} ≤ 100 mA	4.9	5.0	5.1	
		5.6 V ≤ V_{IN} ≤ 16 V, 0 mA ≤ I_{OUT} ≤ 150 mA, −40°C ≤ T_J ≤ +125°C	4.9	5.0	5.1	
Output Voltage	V_{OUT}	5.5 V ≤ V_{IN} ≤ 16 V, 0.1 mA ≤ I_{OUT} ≤ 150 mA	3.234	3.3	3.366	V
		5.5 V ≤ V_{IN} ≤ 40 V, 0.1 mA ≤ I_{OUT} ≤ 100 mA	3.234	3.3	3.366	
Output Current Limit	I_{CL}	OUT = 96% x V_{OUT} nominal	205	–	525	mA
Output Current Limit, Short Circuit	I_{SCKT}	OUT = 0 V	205	–	525	mA
Load Regulation	ΔV_{OUT}	V_{IN} = 13.2 V, I_{OUT} = 0.1 mA to 150 mA	−40	10	40	mV
Line Regulation	ΔV_{OUT}	I_{OUT} = 5 mA, V_{IN} = 6 V to 28 V	−20	0	20	mV
Dropout Voltage – 5.0 V Only	V_{DR}	I_{OUT} = 100 mA, (Note 7) V_{DR} = V_{IN} − V_{OUT}, (ΔV_{OUT} = −100 mV)	–	0.225	0.45	V
		I_{OUT} = 150 mA, (Note 7) V_{DR} = V_{IN} − V_{OUT}, (ΔV_{OUT} = −100 mV)	–	0.30	0.60	
Output Load Capacitance	C_O	Output capacitance for stability	2.2	–	–	μF
Power Supply Ripple Rejection	PSRR	V_{IN} = 13.2 V, 0.5 V_{PP}, 100 Hz	–	60	–	dB
DT (Reset Delay Time Select)						
Threshold Voltage High Low			2 –	– –	– 0.8	V V
Input Current		DT = V_{OUT}	–	–	1.0	μA
RO, Reset Output						
RESET Threshold	V_{Rf}	V_{OUT} decreasing	90	93	96	%V_{OUT}
RESET Threshold Hysteresis	V_{Rhys}		–	2.0	–	%V_{OUT}
RO Output Low	V_{RL}	10 kΩ RESET to OUT, V_{OUT} = 4.5 V	–	0.2	0.4	V
RO Output High (OUT−RO)	V_{RH}	10 kΩ RESET to GND	V_{OUT} −0.4	V_{OUT} −0.2	V_{OUT}	V
Reset Reaction Time	t_{RR}	V_{OUT} into UV to RESET Low	16	25	38	μsec
Input Voltage Reset Threshold	V_{IN_RT}	V_{IN} Decreasing, V_{OUT} > V_{RT}	–	3.8	4.25	V
RESET Delay with DT Selection						
Delay Time Out of RESET – 8 ms version – 16 ms version – 32 ms version – 64 ms version – 128 ms version	t_{dRx}	V_{OUT} into regulation to RO High	 5.0 10 20 40 80	 8.0 16 32 64 128	 11.5 23 46 92 184	msec

6. Not production tested, guaranteed by design.
7. Dropout at a given current level is defined as the voltage difference of V_{IN} to V_{OUT} with V_{IN} decreasing until the output drops by 100 mV.

TYPICAL OPERATING CHARACTERISTICS

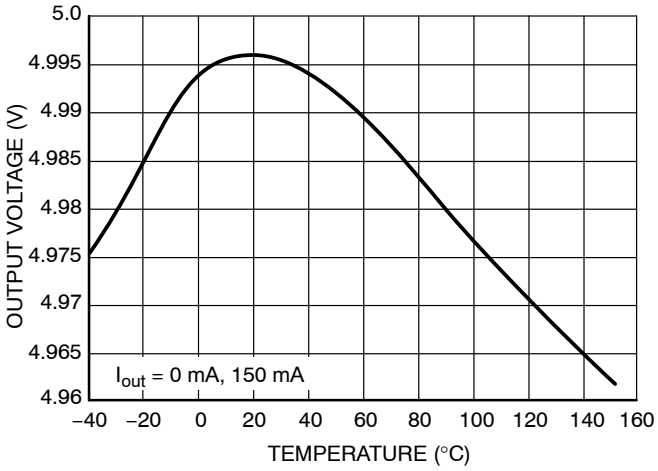


Figure 3. Output Voltage vs. Temperature (OUT = 5 V)

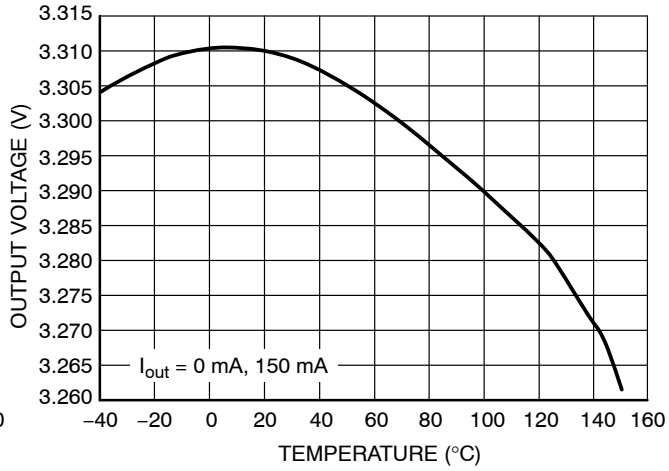


Figure 4. Output Voltage vs. Temperature (OUT = 3.3 V)

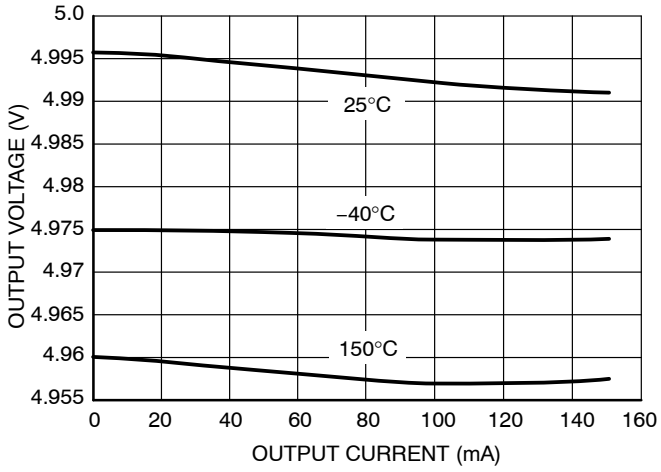


Figure 5. Output Voltage vs. Output Current (OUT = 5 V)

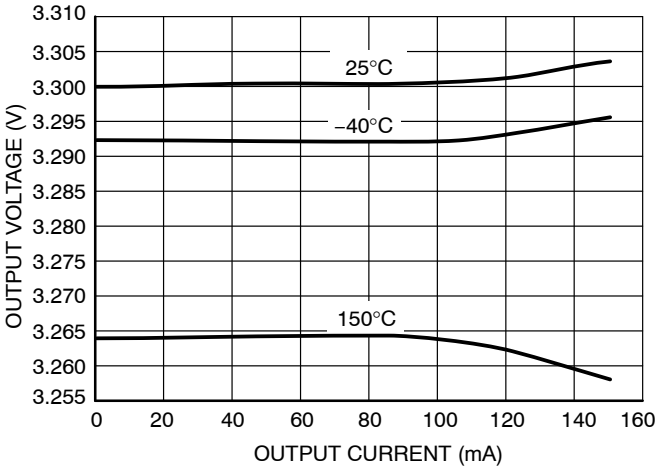


Figure 6. Output Voltage vs. Output Current (OUT = 3.3 V)

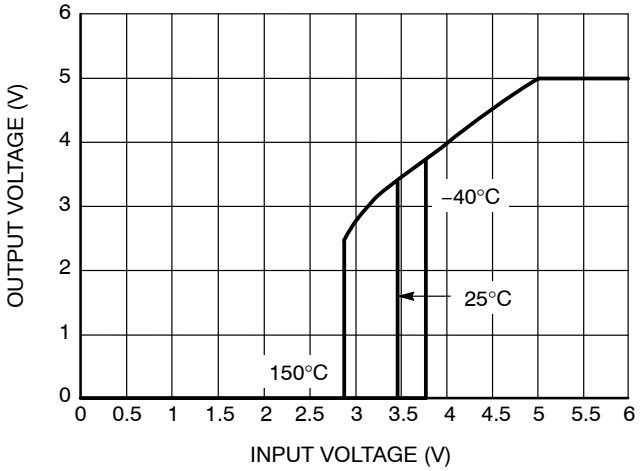


Figure 7. Output Voltage vs. Input Voltage (R_{LOAD} = 51 k, I_{out} = 100 μA, OUT = 5 V)

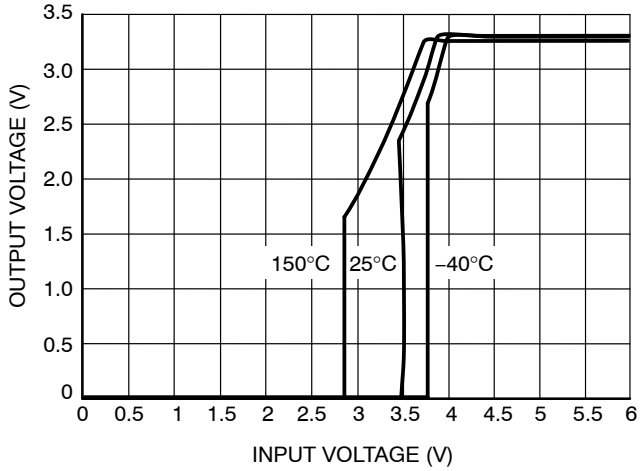


Figure 8. Output Voltage vs. Input Voltage (R_{LOAD} = 33 k, I_{out} = 100 μA, OUT = 3.3 V)

TYPICAL OPERATING CHARACTERISTICS

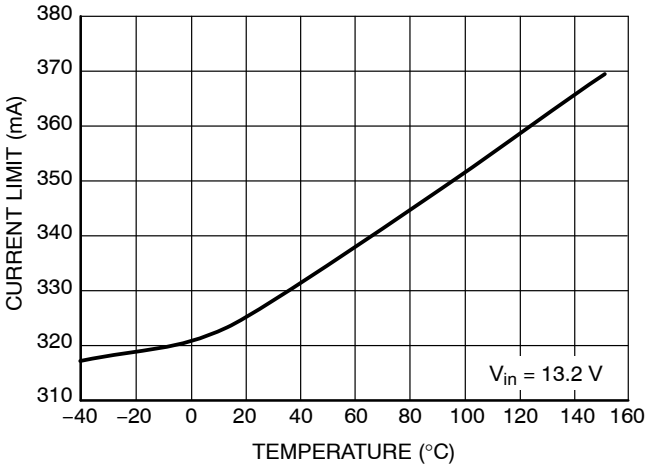


Figure 9. Current Limit vs. Temperature

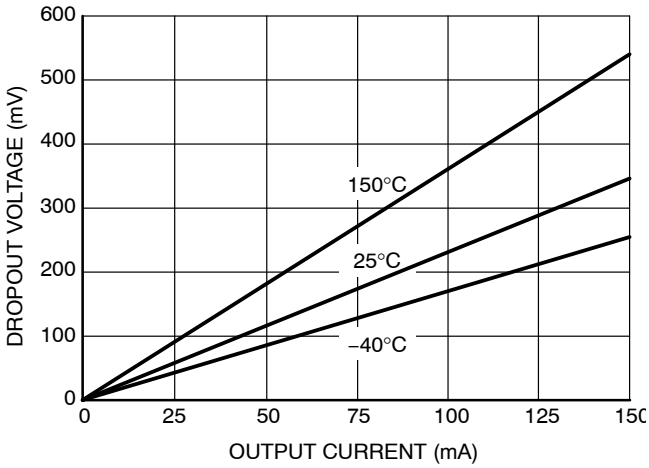


Figure 10. Dropout Voltage vs. Output Current

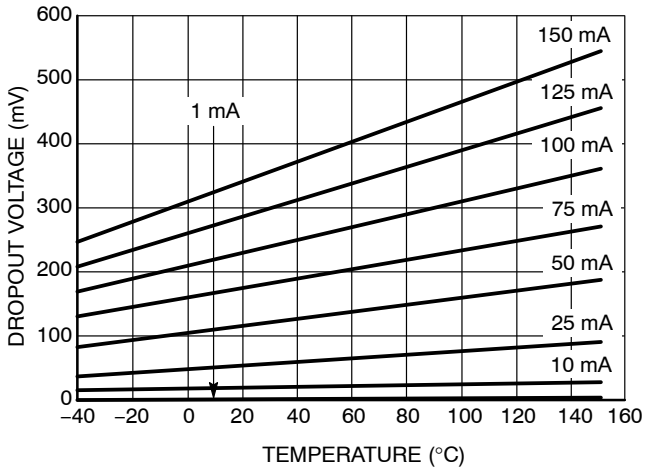


Figure 11. Dropout Voltage vs. Temperature

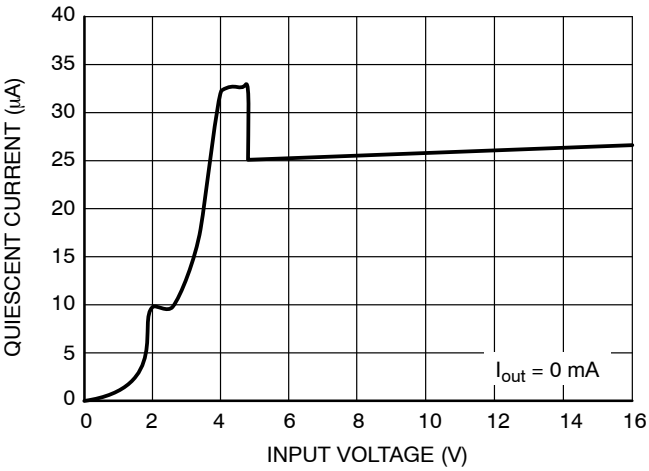


Figure 12. Quiescent Current vs. Input Voltage

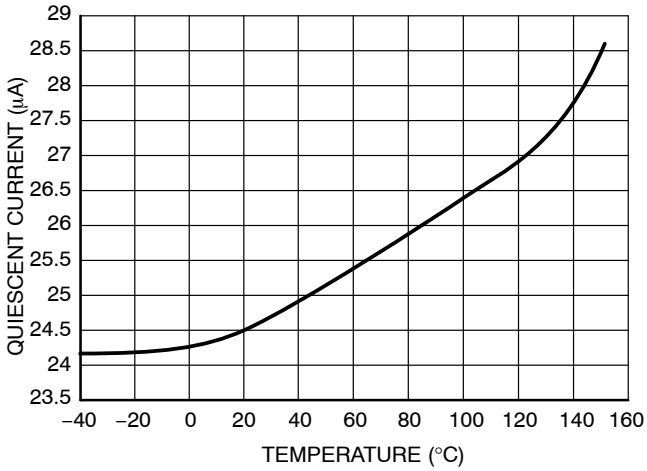


Figure 13. Quiescent Current vs. Temperature

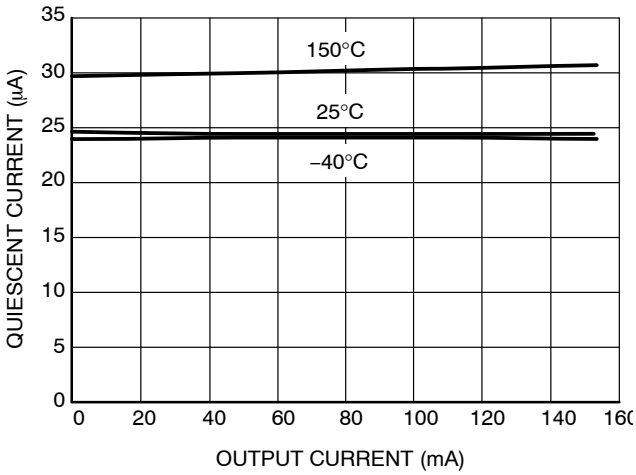


Figure 14. Quiescent Current vs. Output Current

TYPICAL OPERATING CHARACTERISTICS

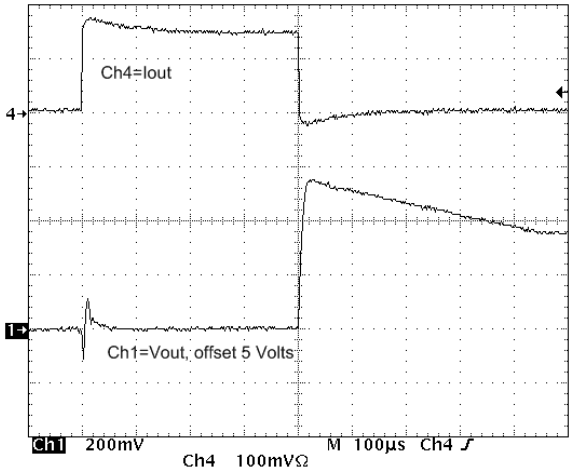


Figure 15. Load Transient (V_{IN} = 13.2 V, OUT = 5 V)

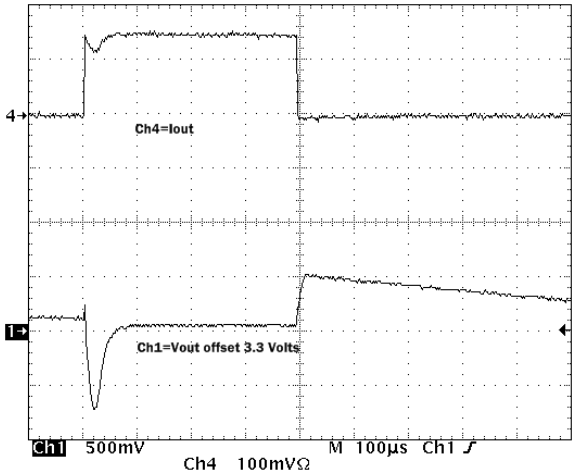


Figure 17. Load Transient (V_{IN} = 13.2 V, OUT = 3.3 V)

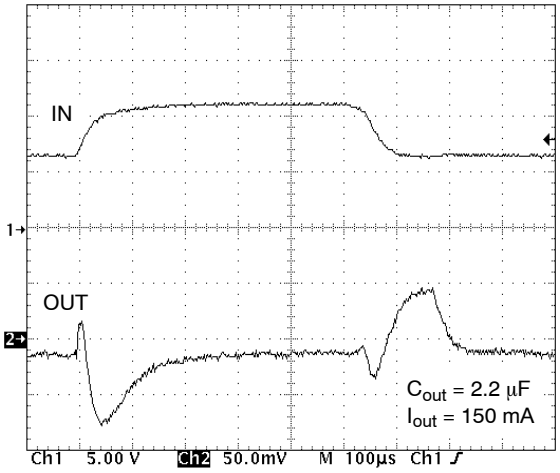


Figure 16. Line Transient (OUT = 5 V)

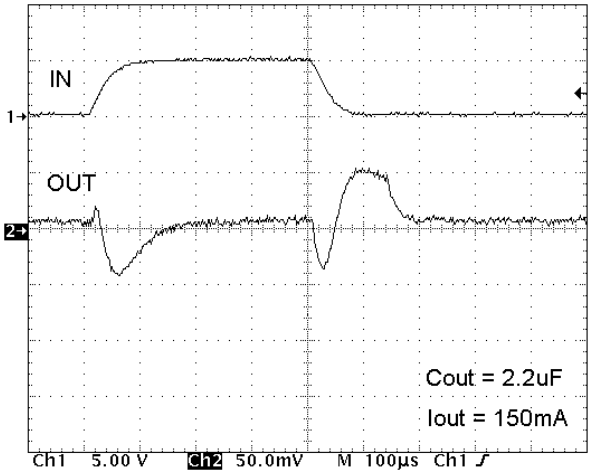


Figure 18. Line Transient (OUT = 3.3 V)

TYPICAL OPERATING CHARACTERISTICS

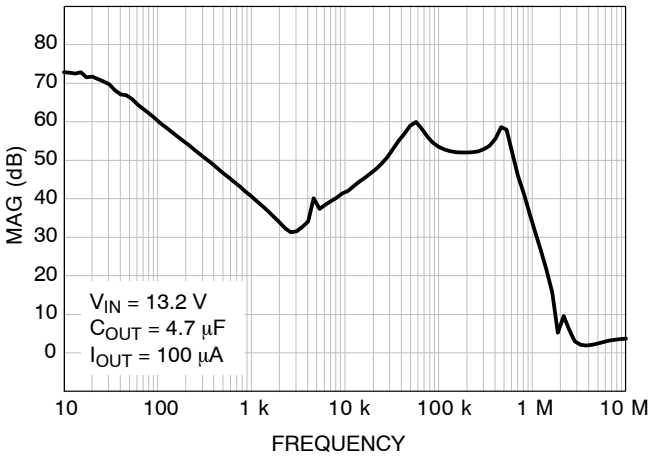


Figure 19. Ripple Rejection vs. Frequency (V_{IN} = 13.2 V, I_{OUT} = 100 μA)

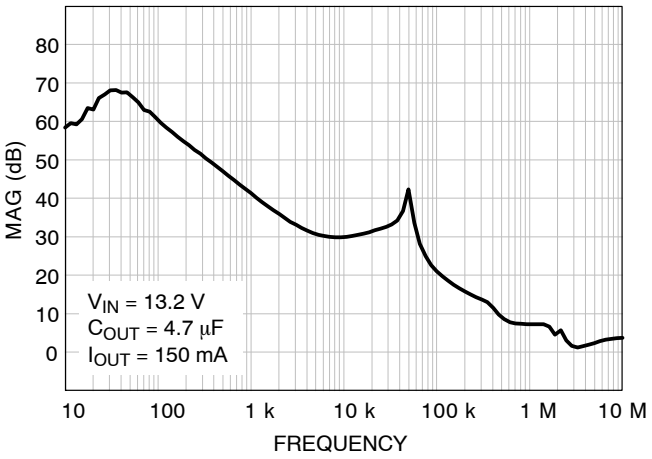


Figure 20. Ripple Rejection vs. Frequency (V_{IN} = 13.2 V, I_{OUT} = 150 mA)

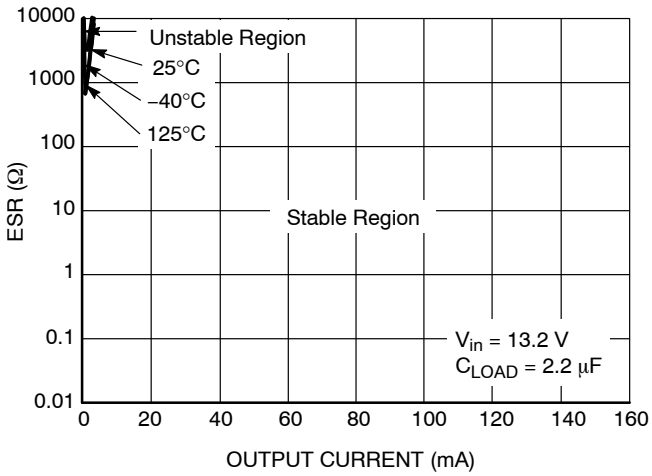


Figure 21. Output Capacitor ESR vs. Output Current (OUT = 5 V)

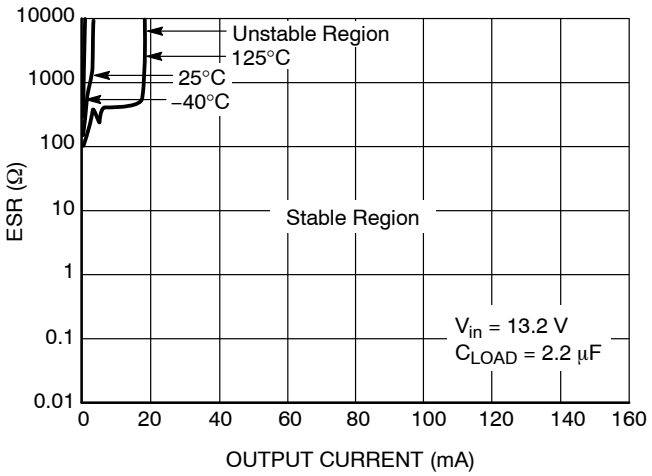


Figure 22. Output Capacitor ESR vs. Output Current (OUT = 3.3 V)

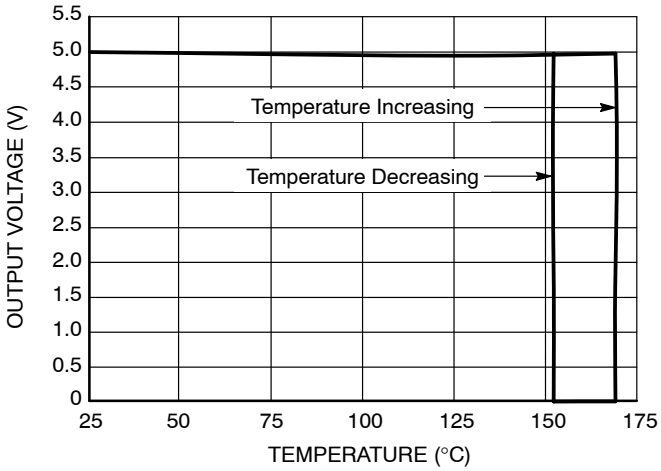


Figure 23. Thermal Shutdown vs. Temperature

DETAILED OPERATING DESCRIPTION

General

The NCV8660B is a 5 V and 3.3 V linear regulator providing low drop−out voltage for 150 mA at low quiescent current levels. Also featured in this part is a reset output with selectable delay times. Delay times are selectable via part selection and control through the Delay Time Select (DT) pin. No pull−up resistor is needed on the reset output (RO). Pull−up and pull−down capability are included. Only a small bypass capacitor on the input (IN) supply pin and output (OUT) voltage pin are required for normal operation. Thermal shutdown functionality protects the IC from damage caused from excessively high temperatures appearing on the IC.

Output Voltage

Output stability is determined by the capacitor selected from OUT to GND. The NCV8660B has been designed to work with low ESR (equivalent series resistance) ceramic capacitors. The device is extremely stable using virtually any capacitor 2.2 μF and above. Reference the Output Capacitor Stability graph in Figure 21.

The output capacitor value will affect overshoot during power−up. A lower value capacitor will cause higher overshoot on the output. System evaluation should be performed with minimum loading for evaluation of overshoot.

Selection of process technology for the NCV8660B allows for low quiescent current independent of loading. Quiescent current will remain flat across the entire range of loads providing a low quiescent current condition in standby and under heavy loads. This is highly beneficial to systems requiring microprocessor interrupts during standby mode as duty cycle and load changes have no impact on the standby current. Reference Figure 14 for Quiescent Current vs Output Current.

Current Limit

Current limit is provided on OUT to protect the IC. The minimum specification is 205 mA. Current limit is specified under two conditions (OUT = 96% x OUT nominal) and (OUT = 0 V). No fold−back circuitry exists. Any measured differences can be attributed to change in die temperature. The part may be operated up to 205 mA provided thermal die temperature is considered and is kept below 150°C. Degradation of electrical parameters at this current is expected at these elevated levels. A reset (RO) will not occur with a load less than 205 mA.

Reset Output

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. This is in the form of a logic signal on RO. Output (OUT) voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to OUT = 1.0 V.

The Reset Output (RO) circuitry includes an active internal pullup to the output (OUT) as shown in Figure 24. No external pullup is neccessary.

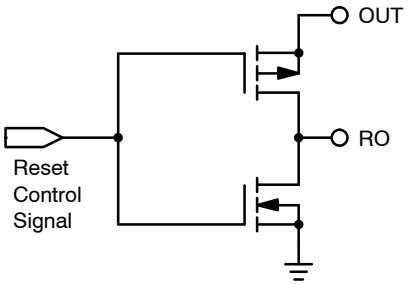


Figure 24. Reset Output Circuitry

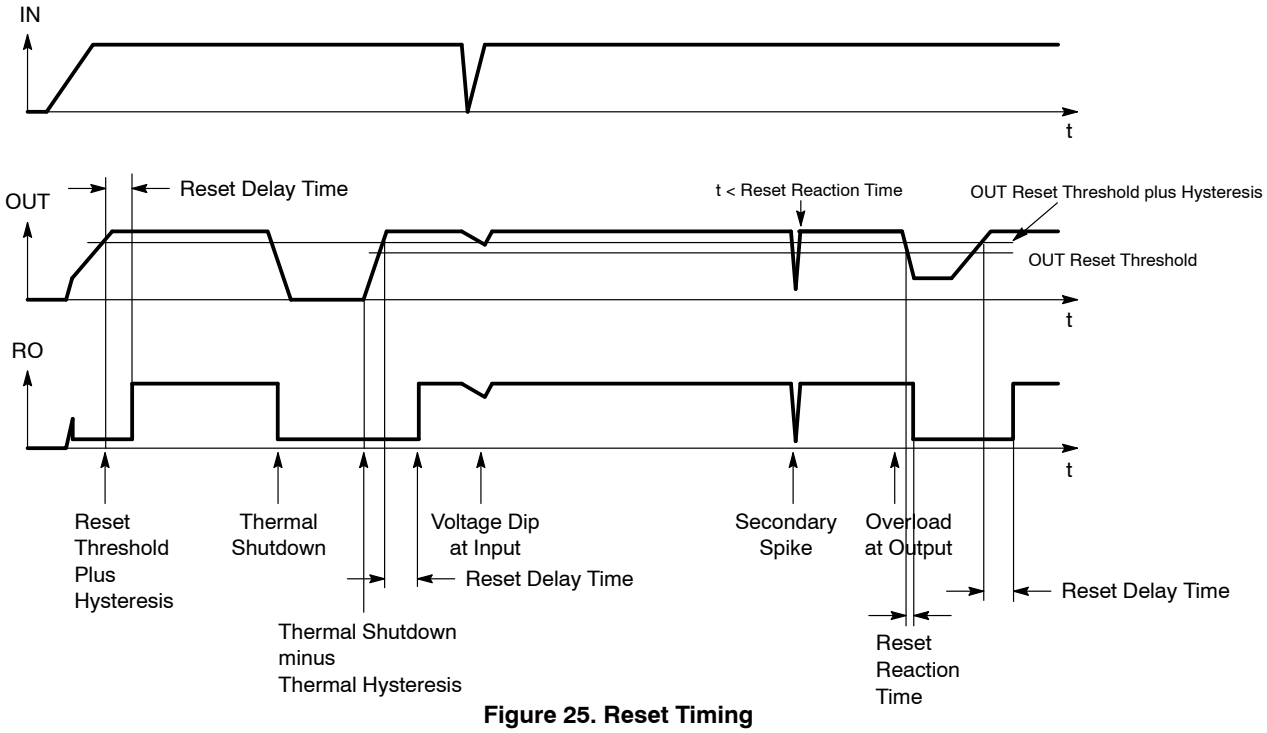


Figure 25. Reset Timing

During power−up (or restoring OUT voltage from a reset event), the OUT voltage must be maintained above the Reset threshold for the Reset Delay time before RO goes high. The time for Reset Delay is determined by the choice of IC and the state of the DT pin.

Reset Delay Time Select

Selection of the NCV8660B device and the state of the DT pin determines the available Reset Delay times. The part is designed for use with DT tied to ground or OUT, but may be controlled by any logic signal which provides a threshold between 0.8 V and 2 V. The default condition for an open DT pin is the slower Reset time (DT = GND condition). Times are in pairs and are highlighted in the chart below. Consult factory for availability.

	DT=GND	DT=OUT
	Reset Time	**Reset Time**
NCV86601B	8 ms	128 ms
NCV86602B	8 ms	32 ms
NCV86603B	16 ms	64 ms
NCV86604B	32 ms	128 ms

The Delay Time select (DT) pin is logic level controlled and provides Reset Delay time per the chart. Note the DT pin is sampled only when RO is low, and changes to the DT pin when RO is high will not effect the reset delay time.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold, a Thermal Shutdown event is detected OUT is turned off, and RO goes low. The IC will remain in this state until the die temperature moves below the shutdown threshold (175°C typical) minus the hysteresis factor (25°C typical). The output will then turn back on and RO will go high after the RESET Delay time.

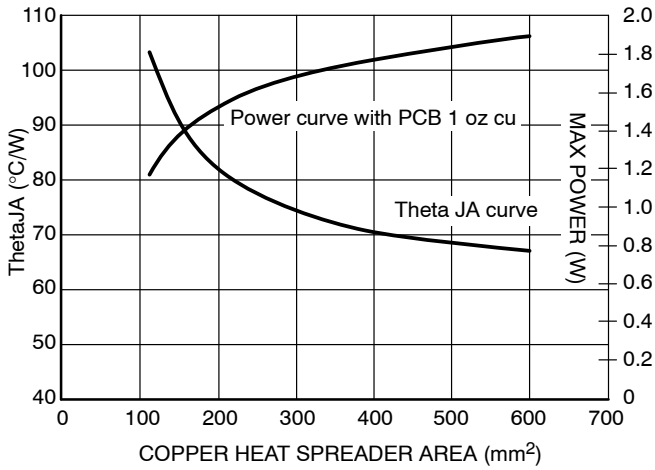


Figure 26. $R_{\theta JA}$ vs. PCB Copper Area (DPAK)

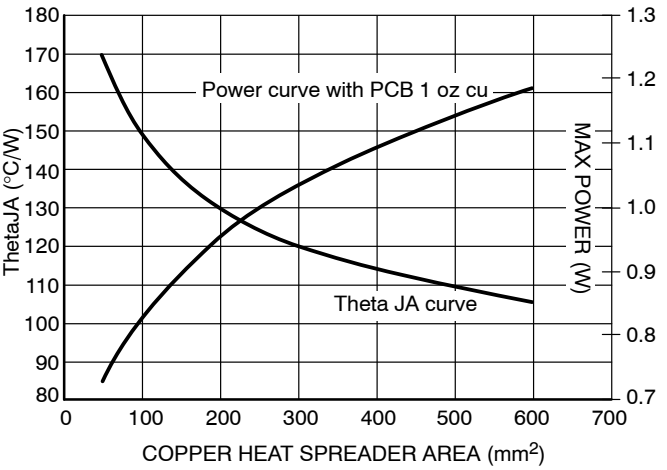


Figure 28. $R_{\theta JA}$ vs. PCB Copper Area (SOIC−8 Fused)

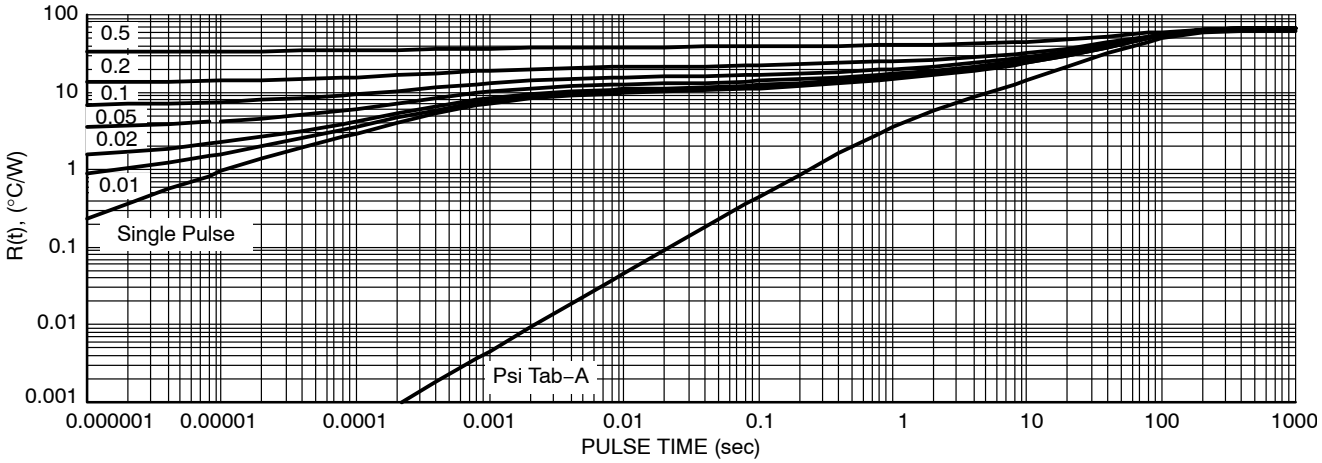


Figure 27. Transient Thermal Response (DPAK)
Cu Area = 645 mm²

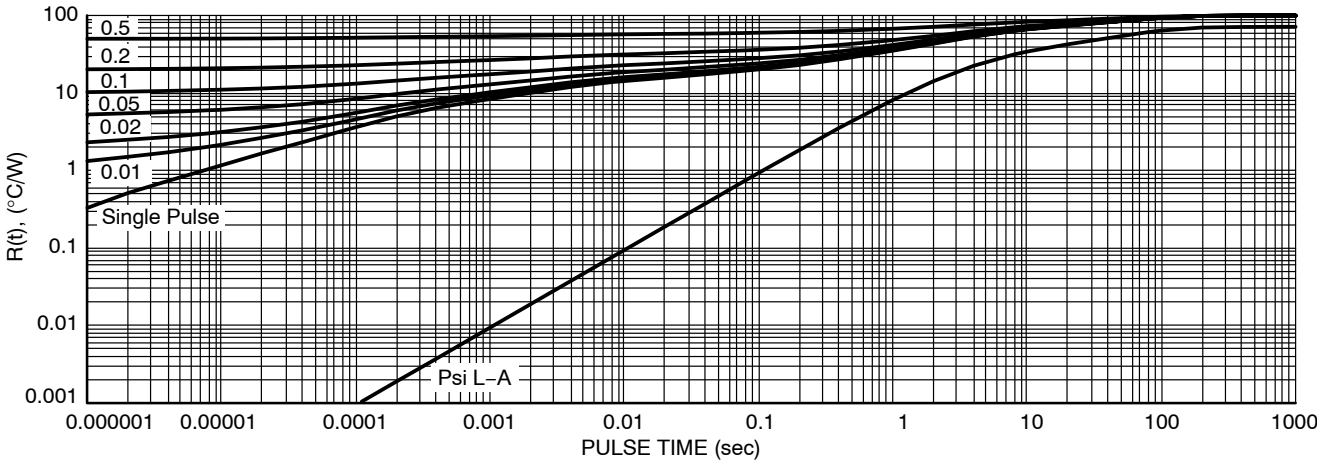


Figure 29. Transient Thermal Response (SOIC−8 Fused)
Cu Area = 645 mm²

ORDERING INFORMATION

Device	Output Voltage	Reset Delay Time, DT to GND	Reset Delay Time, DT to OUT	Package	Shipping†
NCV86601BDT50RKG	5.0 V	8 ms	128 ms	DPAK (Pb−Free)	2500 / Tape & Reel
NCV86602BDT50RKG		8 ms	32 ms		
NCV86603BDT50RKG		16 ms	64 ms		
NCV86604BDT50RKG		32 ms	128 ms		
NCV86601BD50R2G		8 ms	128 ms	SOIC−8 FUSED (Pb−Free)	2500 / Tape & Reel
NCV86602BD50R2G		8 ms	32 ms		
NCV86603BD50R2G		16 ms	64 ms		
NCV86604BD50R2G		32 ms	128 ms		
NCV86601BDT33RKG	3.3 V	8 ms	128 ms	DPAK (Pb−Free)	2500 / Tape & Reel
NCV86602BDT33RKG		8 ms	32 ms		
NCV86603BDT33RKG		16 ms	64 ms		
NCV86604BDT33RKG		32 ms	128 ms		
NCV86601BD33R2G		8 ms	128 ms	SOIC−8 FUSED (Pb−Free)	2500 / Tape & Reel
NCV86602BD33R2G		8 ms	32 ms		
NCV86603BD33R2G		16 ms	64 ms		
NCV86604BD33R2G		32 ms	128 ms		

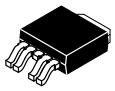
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

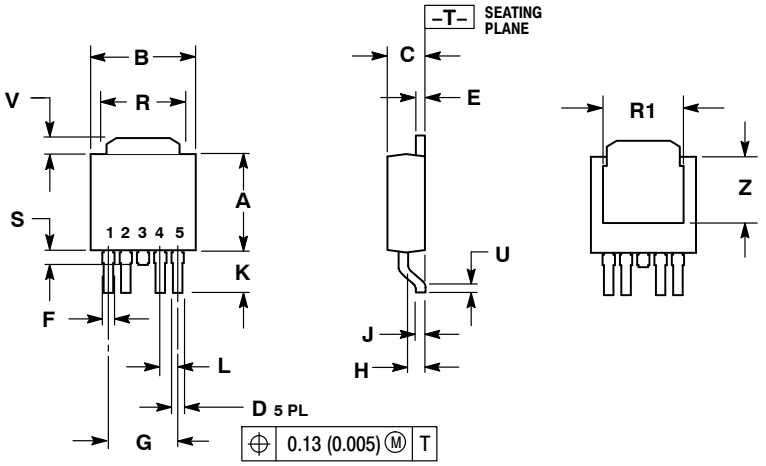
ON Semiconductor®

DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

DATE 15 MAY 2014



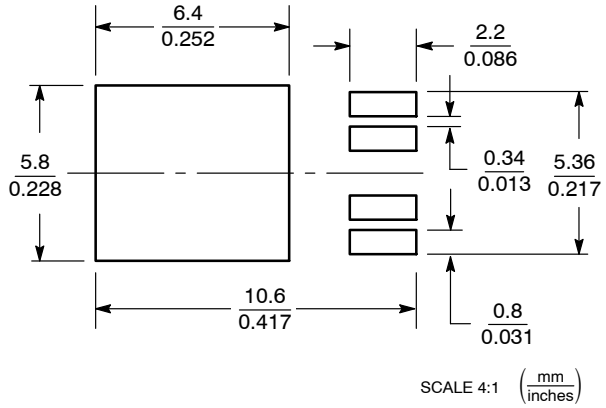
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

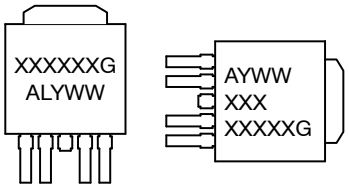
RECOMMENDED SOLDERING FOOTPRINT*



SCALE 4:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON12855D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DPAK−5 CENTER LEAD CROP**	**PAGE 1 OF 1**

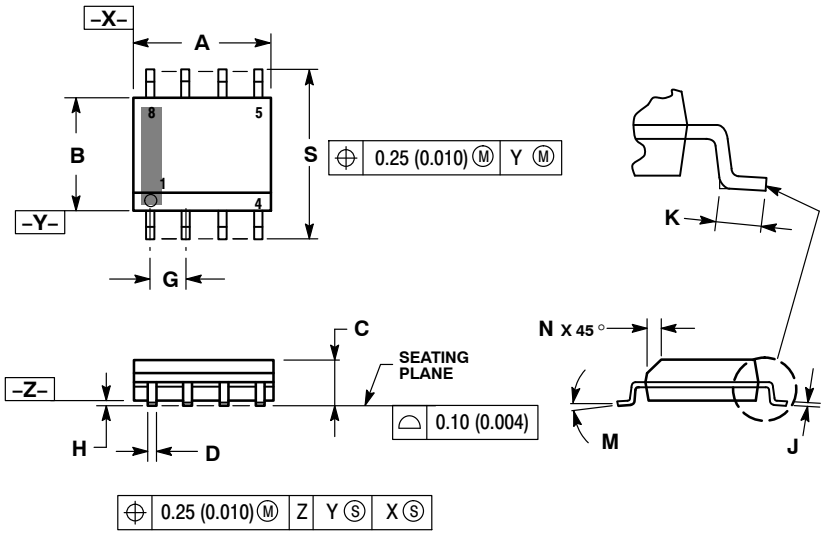
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

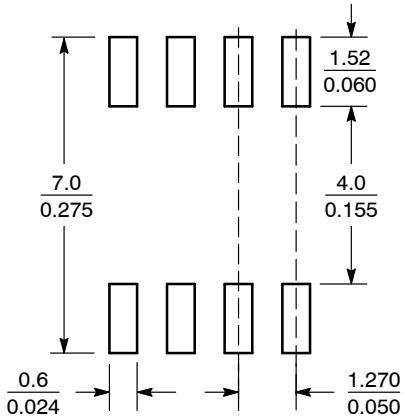
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

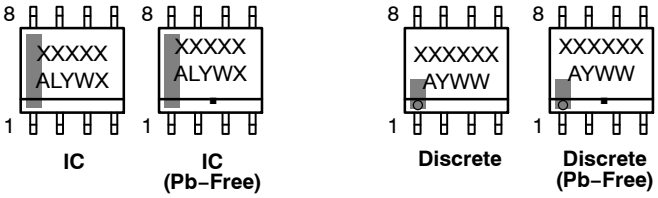
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

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