

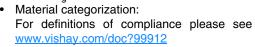
Vishay Siliconix

# N-Channel 75 V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)	
75	0.007 at V <sub>GS</sub> = 10 V	110 <sup>d</sup>	69	

#### **FEATURES**

- TrenchFET® Power MOSFETS
- 100 %  $\rm R_{\rm g}$  and UIS Tested

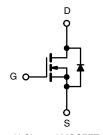






#### **APPLICATIONS**

· Synchronous Rectification



N-Channel MOSFET

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		$\supset$
Н		귄
G	D	S
To	p Vi	ew

Ordering Information: SUM110N08-07P-E3 (Lead (Pb)-free)

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	75	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	\ \ \	
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	T <sub>C</sub> = 25 °C	1-	110 <sup>d</sup>	А	
Continuous Diain Current (1) = 130 °C)	T <sub>C</sub> = 70 °C	-	103		
Pulsed Drain Current		I <sub>DM</sub>	180	_ ^	
Avalanche Current		I <sub>AS</sub>	50		
Single Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AS</sub>	125	mJ	
Mariana Barra Birahadi ad	T <sub>C</sub> = 25 °C	В	208.3 <sup>b</sup>	w	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C <sup>c</sup>	P <sub>D</sub>	3.75		
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.6		

#### Notes:

- a. Duty cycle  $\leq$  1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Package limited.

## SUM110N08-07P

# Vishay Siliconix



<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25	°C, unless o	otherwise noted)					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	75			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.5		4.5		
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA	
Zero Gate Voltage Drain Current		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}$			1	μА	
	I <sub>DSS</sub>	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50		
		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 150 ^{\circ}\text{C}$			250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	70			Α	
Drain-Source On-State Resistance <sup>a</sup>	D	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0057	0.0070	Ω	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C		0.0092	0.0112		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		43		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			4250		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 30 \text{ V}, f = 1 \text{ MHz}$		580			
Reverse Transfer Capacitance	C <sub>rss</sub>			230			
Total Gate Charge <sup>c</sup>	$Q_g$			69	105	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$		23			
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			21			
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.2	2.4	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			17	30		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 30 V, $R_L$ = 0.6 $\Omega$		5	10	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	40		
Fall Time <sup>c</sup>	t <sub>f</sub>		6	15			
Source-Drain Diode Ratings and Ch	aracteristics 7	r <sub>C</sub> = 25 °C <sup>b</sup>					
Continuous Current	Is				110		
Pulsed Current	I <sub>SM</sub>				180	Α	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		0.83	1.5	V	
Reverse Recovery Time	t <sub>rr</sub>			65	100	ns	
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 75 A, dl/dt = 100 A/μs		2.5	5	Α	
Reverse Recovery Charge	Q <sub>rr</sub>			85	150	nC	

#### Notes:

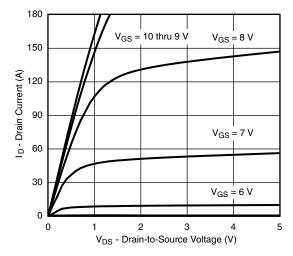
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

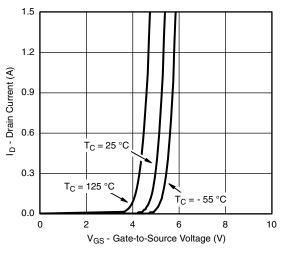




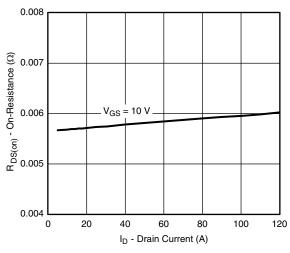
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



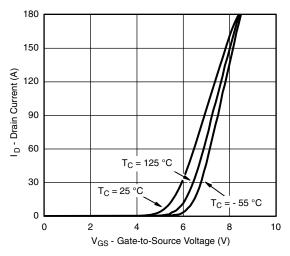
#### **Output Characteristics**



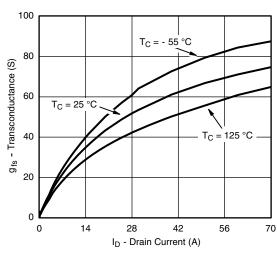
#### **Transfer Characteristics**



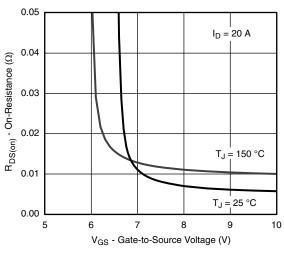
On-Resistance vs. Drain Current



**Transfer Characteristics** 



Transconductance

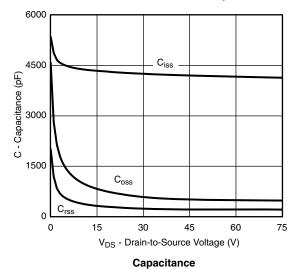


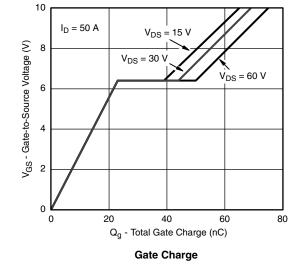
On-Resistance vs. Gate-to-Source Voltage

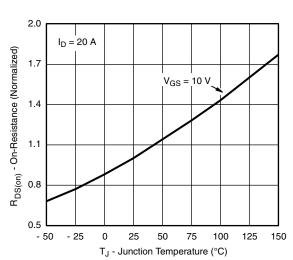
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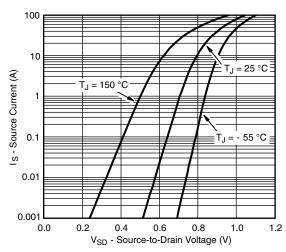
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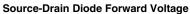


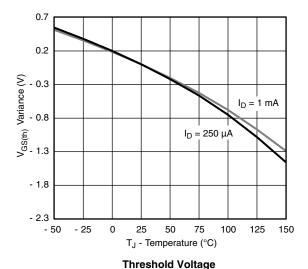


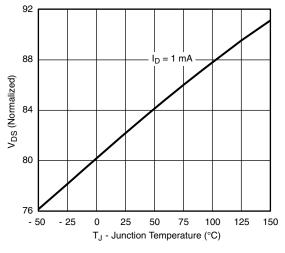




On-Resistance vs. Junction Temperature





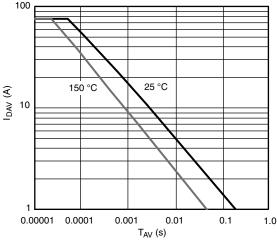


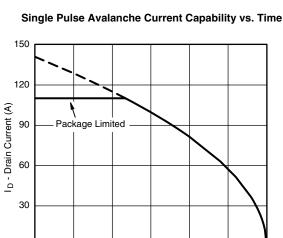
Drain Source Breakdown vs. Junction Temperature



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### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





# 75

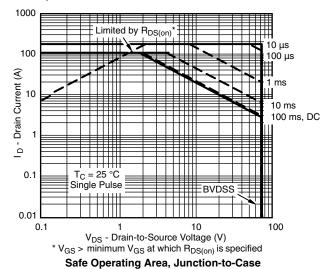
T<sub>C</sub> - Case Temperature (°C)

Current Derating\*, Junction-to-Case

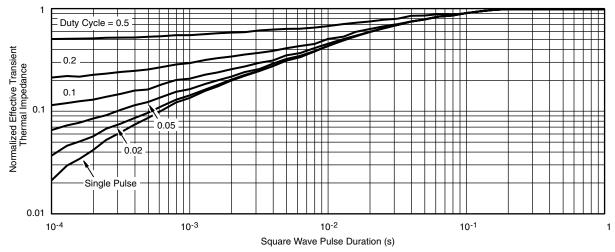
100

125

150



 $^{\star}$  The power dissipation P<sub>D</sub> is based on T<sub>J(max)</sub> = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case

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Document Number: 68637 S12-1616-Rev. B, 09-Jul-12

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