NCP4687

Linear Voltage Regulator, LDO, High PSRR, 500 mA

The NCP4687 is a CMOS 500 mA LDO linear voltage regulator with high output voltage accuracy which features a high ripple rejection, low supply current with low dropout and chip enable with built−in low $R_{DS(on)}$ NMOS transistor for fast output capacitor discharging as option. The device is composed of the voltage reference unit, error amplifier, resistor divider for output voltage sensing or precise output voltage setting. The current limit and thermal shutdown makes the device very suitable for industrial applications and portable communication equipments.

Features

- Operating Input Voltage Range: 2.5 V to 5.25 V
- Output Voltage Range: 0.7 to 3.6 V (available in 0.1 V steps)
- ±0.8% Output Voltage Accuracy @ V_{out} > 1.8 V
- Output noise : 40 μV_{rms}
- Line Regulation: 0.02%/V
- Current Limit Circuit
- High PSRR: 75 dB at 1 kHz, 70 dB at 10 kHz
- Thermal Shutdown
- Available in SOT−23−5, SOT−89−5 and uDFN 1.2 x 1.2 mm Packages
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Home Appliances, Industrial Equipment
- DVB−T and DVB−S Receivers
- Car Audio Equipment, Navigation Systems
- Notebook Adaptors, LCD TVs, Cordless Phones and Private LAN Systems

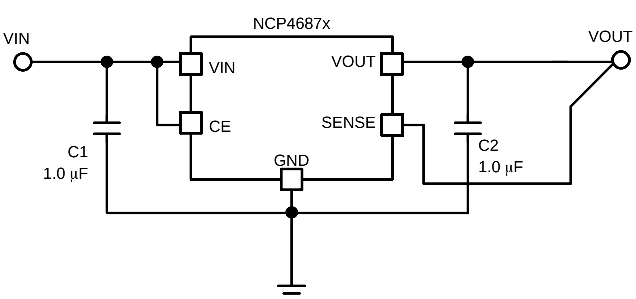
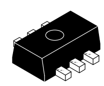


Figure 1. Typical Application Schematic

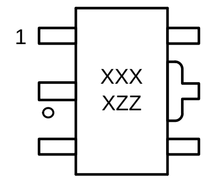
ON Semiconductor™

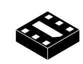
http://onsemi.com

MARKING DIAGRAMS

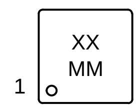


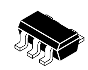
SOT89−5
CASE 528AB



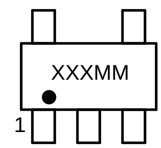


XDFN6
CASE 711AH





SOT−23−5
CASE 1212



XX, XXX = Specific Device Code
ZZ = Lot Code
MM = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

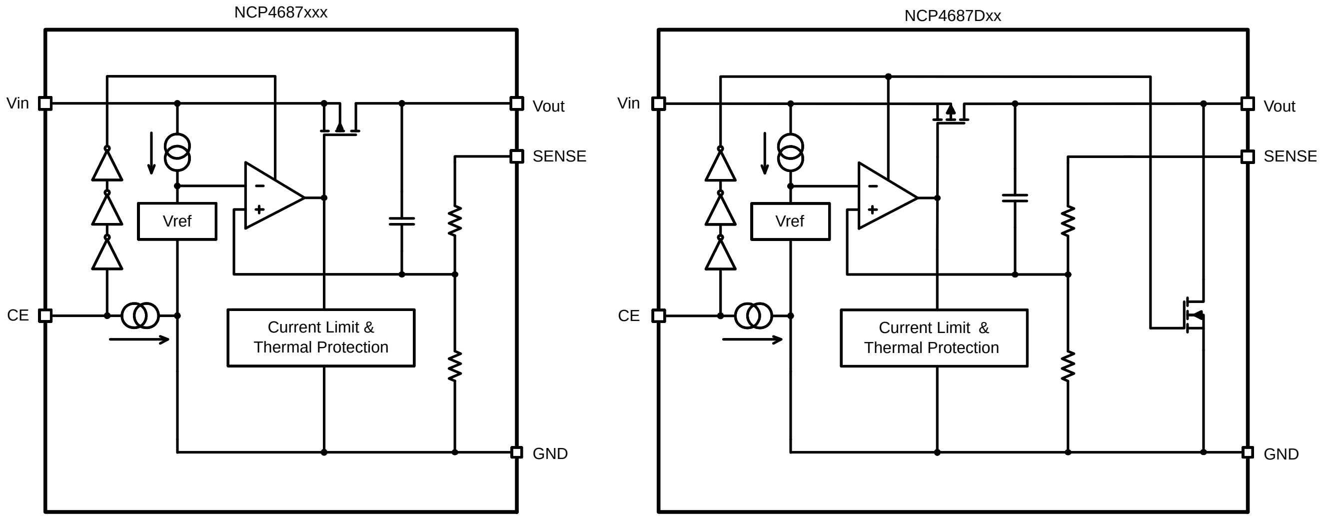


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. SOT−23−5	Pin No. SOT−89−5	Pin No. DFN1212	Pin Name	Description
1	4	6	VIN	Input pin
2	2	3	GND	Ground pin
3	3	4	CE	Chip enable pin (“H” active)
4	1	2	SENSE	Output Voltage Sensing
5	5	1	VOUT	Output pin
		5	NC	Non Connected
		*EP	EP	Exposed Pad (leave floating or connect to GND)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	0 − 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} − 0.3	V
Chip Enable Input	V_{CE}	−0.3 − 6	V
Power Dissipation SOT−23−5	P_D	420	mW
Power Dissipation uDFN 1.2 x 1.2 mm		600	
Power Dissipation SOT−89−5		900	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT−23−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, uDFN 1.2x1.2 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	167	°C/W
Thermal Characteristics, SOT−89−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	111	°C/W

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$; $C_{IN} = C_{OUT} = 1.0\ \mu F$, unless otherwise noted. Typical values are at $T_A = +25°C$.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	$V_{OUT} \le 1.5$ V	V_{IN}	2.5		5.25	V
	$V_{OUT} > 1.5$ V		$V_{OUT} + 1$		5.25	
Output Voltage	Ta = 25°C, $V_{OUT} > 1.8$ V	V_{OUT}	x0.992		x1.008	V
	−40°C < Ta < 85°C, $V_{OUT} > 1.8$ V		x0.985		x1.015	V
	Ta = 25°C, $V_{OUT} \le 1.8$ V		−18		+18	mV
	−40°C < Ta < 85°C, $V_{OUT} \le 1.8$ V		−55		+55	mV
Output Voltage Temp. Coefficient	−40°C < Ta < 85°C, $V_{OUT} > 1.8$ V			±30		ppm/°C
	−40°C < Ta < 85°C, $V_{OUT} \le 1.8$ V			±100		
Load Regulation	1 mA < $I_{OUT} \le$ 500 mA	$Load_{Reg}$		1	20	mV
Line Regulation	Set V_{OUT} + 0.5 V < V_{IN} < 5.25 V	$Line_{Reg}$		0.02	0.1	%/V
Dropout Voltage	I_{OUT} = 500 mA, 0.7 V ≤ V_{OUT} < 0.8 V	V_{DO}		0.58	0.88	V
	0.8 V ≤ V_{OUT} < 0.9 V			0.52	0.80	
	0.9 V ≤ V_{OUT} < 1.0 V			0.45	0.70	
	1.0 V ≤ V_{OUT} < 1.2 V			0.42	0.64	
	1.2 V ≤ V_{OUT} < 1.4 V			0.35	0.53	
	1.4 V ≤ V_{OUT} < 1.8 V			0.31	0.48	
	1.8 V ≤ V_{OUT} < 2.1 V			0.27	0.41	
	2.1 V ≤ V_{OUT} < 2.5 V			0.25	0.38	
	2.5 V ≤ V_{OUT} < 3.0 V			0.23	0.34	
	3.0 V ≤ V_{OUT} < 3.6 V			0.22	0.32	
Output Current		I_{OUT}	500			mA
Short Current Limit	V_{OUT} = 0 V	I_{SC}		50		mA
Quiescent Current	I_{OUT} = 0 mA, V_{OUT} > 1.5 V	I_Q		80	115	μA
	$V_{OUT} \le 1.5$ V			75		
Standby Current	$V_{IN} = V_{IN\ max}$, V_{CE} = 0 V	I_{STB}		0.1	1.0	μA
CE Pin Pull−Down Current		I_{PD}		0.3	0.6	μA
CE Pin Threshold Voltage	CE Input Voltage “H”	V_{CEH}	1.0		V_{IN}	V
	CE Input Voltage “L”	V_{CEL}			0.4	
Power Supply Rejection Ratio	$V_{OUT} \le 2.0$ V @ V_{IN} = 3.0 V, V_{OUT} > 2.0 V @ V_{IN} = = Set V_{OUT} + 1.0 V, ΔV_{IN_PK-PK} = 0.2 V, I_{OUT} = 30 mA; f = 1 kHz	PSRR		75		dB
	f = 10 kHz			70		
Output Noise Voltage	I_{OUT} = 30 mA , f = 10 Hz to 100 kHz, V_{OUT} > 1.8 V	V_{NOISE}		20 x V_{OUT}		μV_{rms}
	I_{OUT} = 30 mA, f = 10 Hz to 100 kHz, $V_{OUT} \le 1.8$ V			40 x V_{OUT}		
Thermal Shutdown / Hysteresis				165/65		°C
Auto−discharge N−MOS Resistance	V_{IN} = 4.0 V, V_{CE} = 0.0 V (Note 2)	$R_{DS(on)}$		60		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2.

TYPICAL CHARACTERISTICS

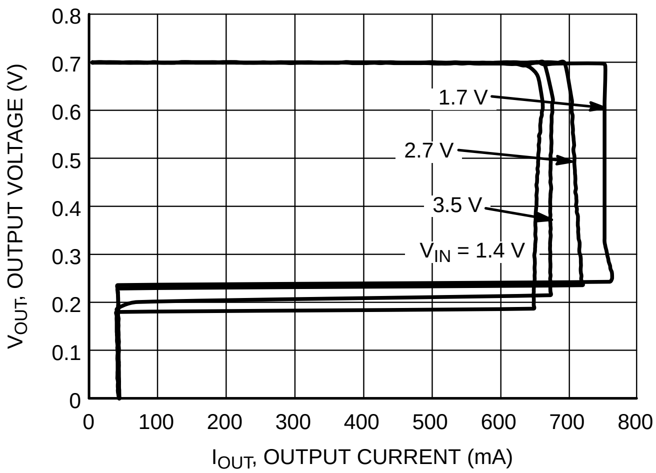


Figure 3. Output Voltage vs. Output Current 0.7 V Version

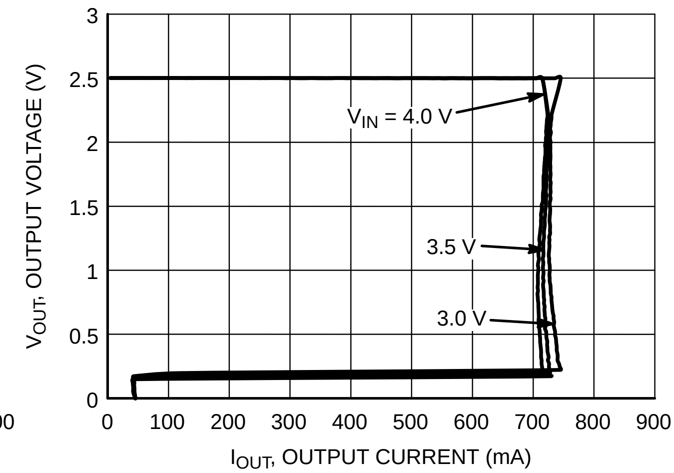


Figure 4. Output Voltage vs. Output Current 2.5 V Version

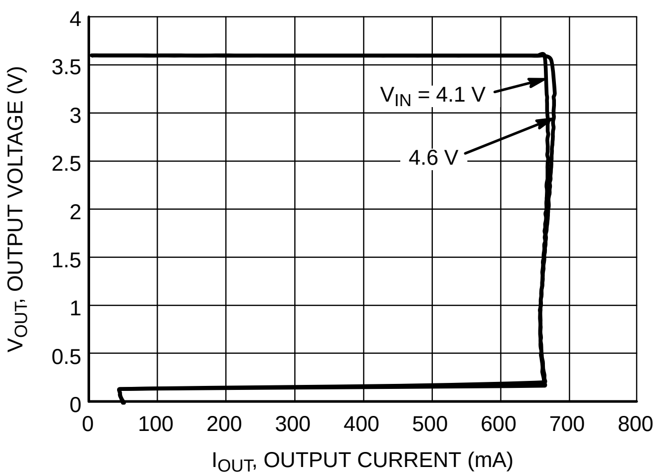


Figure 5. Output Voltage vs. Output Current 3.6 V Version

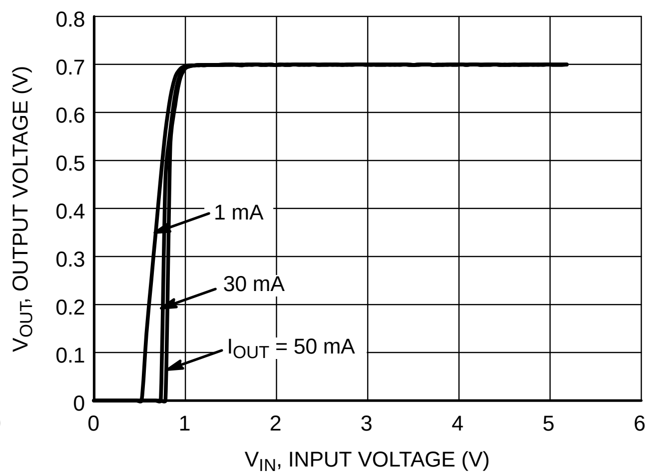


Figure 6. Output Voltage vs. Input Voltage 0.7 V Version

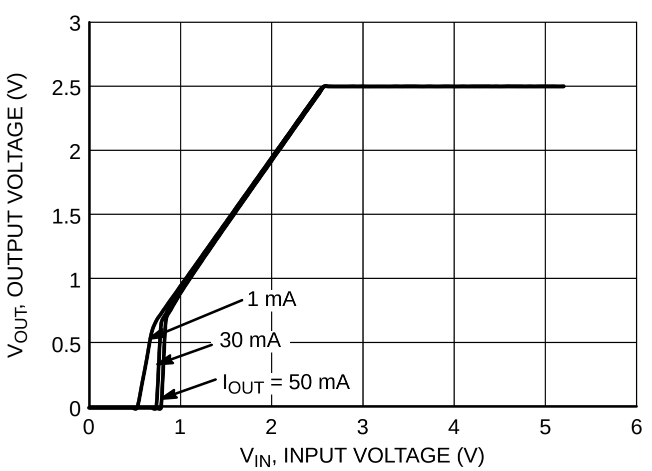


Figure 7. Output Voltage vs. Input Voltage 2.5 V Version

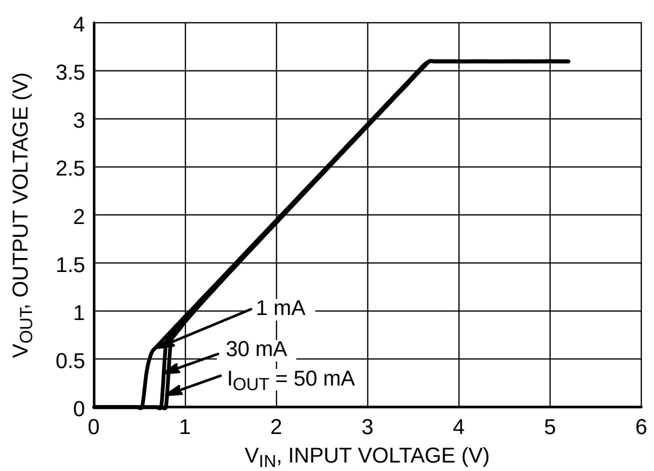


Figure 8. Output Voltage vs. Input Voltage 3.6 V Version

TYPICAL CHARACTERISTICS

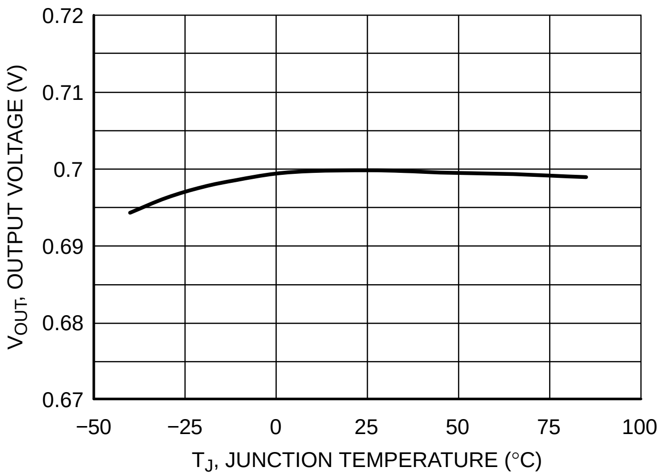


Figure 9. Output Voltage vs. Temperature, 0.7 V Version

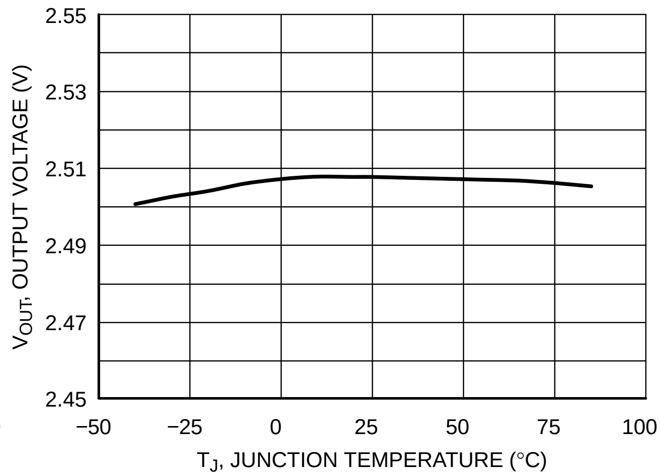


Figure 10. Output Voltage vs. Temperature, 2.5 V Version

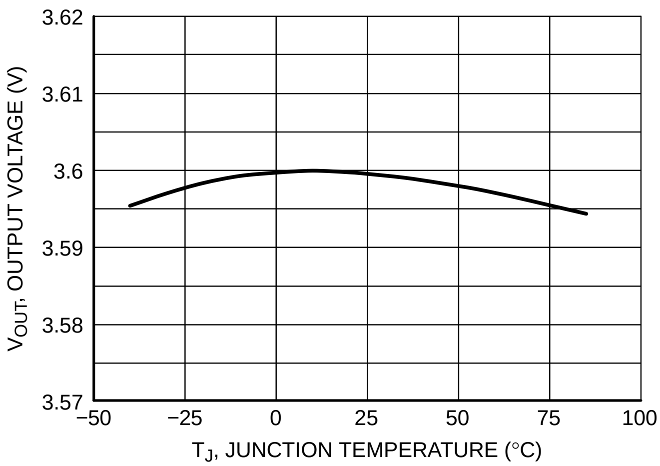


Figure 11. Output Voltage vs. Temperature, 3.6 V Version

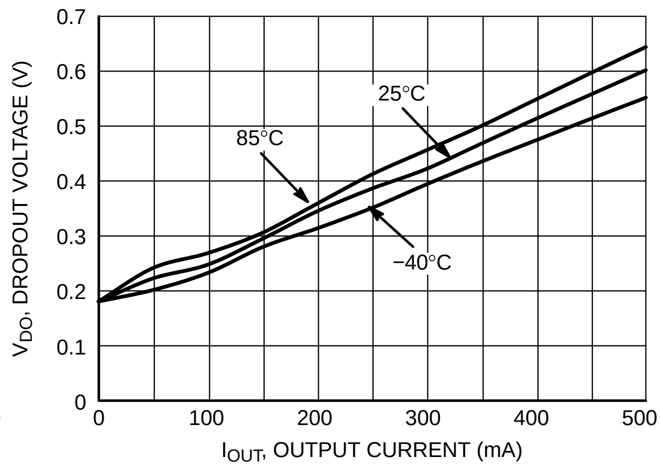


Figure 12. Dropout Voltage vs. Output Current, 0.7 V Version

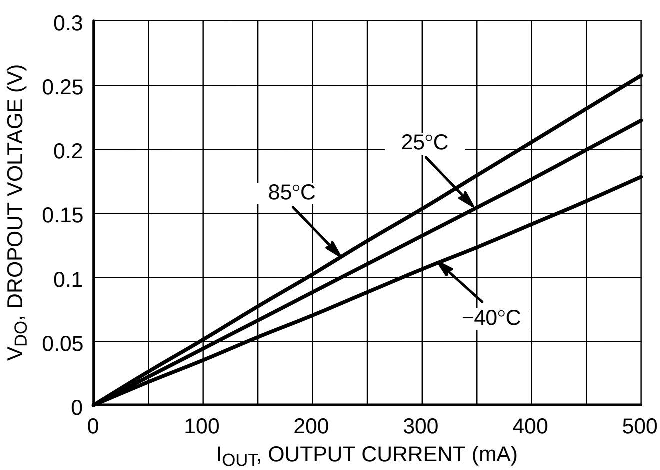


Figure 13. Dropout Voltage vs. Output Current, 2.5 V Version

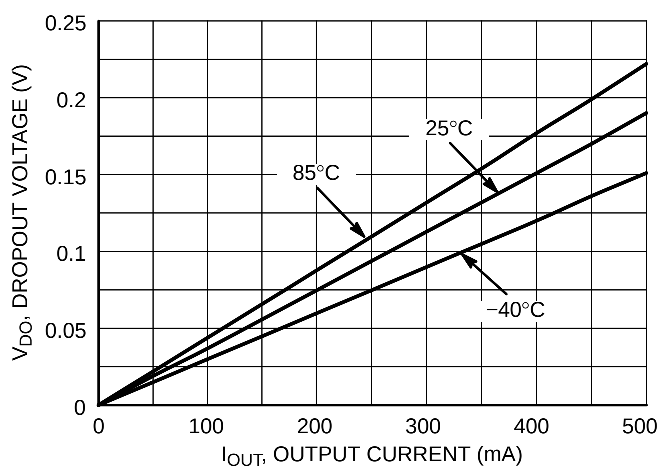


Figure 14. Dropout Voltage vs. Output Current, 3.6 V Version

TYPICAL CHARACTERISTICS

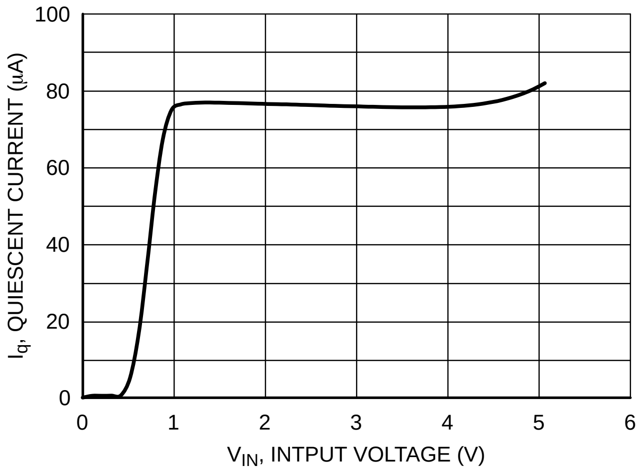


Figure 15. Quiescent Current vs. Input Voltage, 0.7 V Version

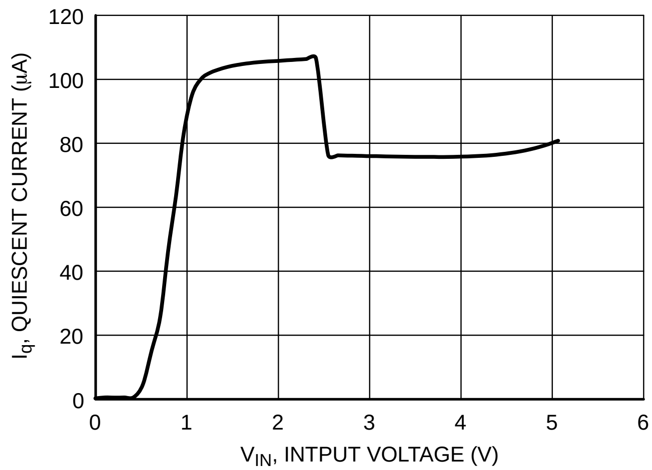


Figure 16. Quiescent Current vs. Input Voltage, 2.5 V Version

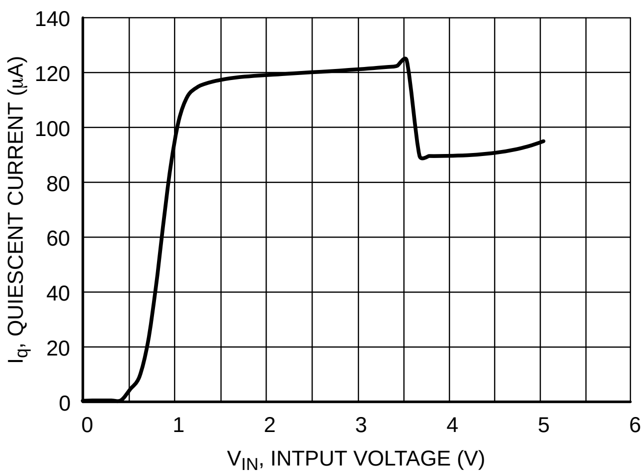


Figure 17. Quiescent Current vs. Input Voltage, 3.6 V Version

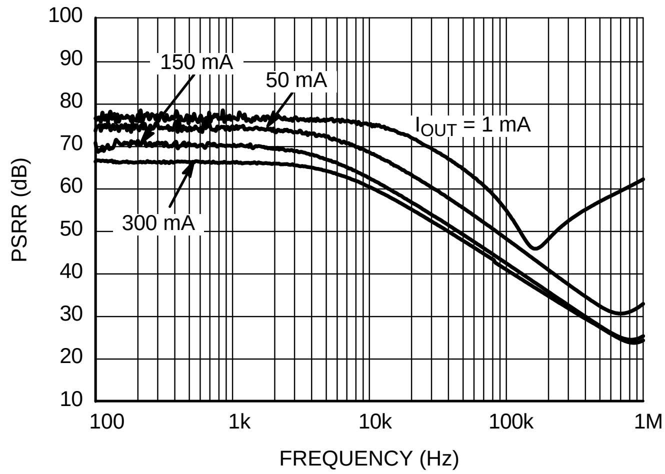


Figure 18. PSRR vs. Frequency, 0.7 V Version

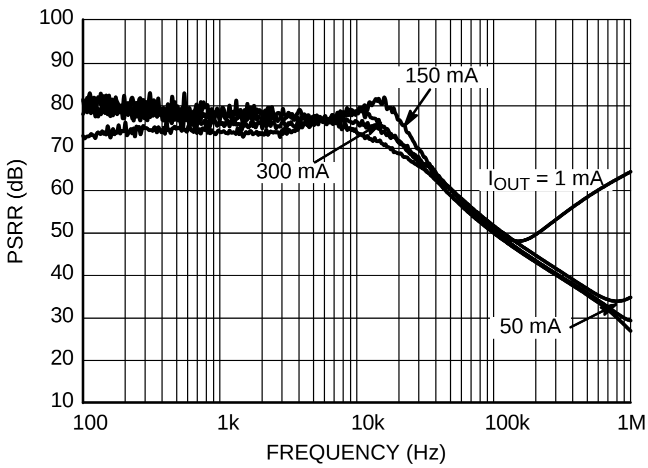


Figure 19. PSRR vs. Frequency, 2.5 V Version

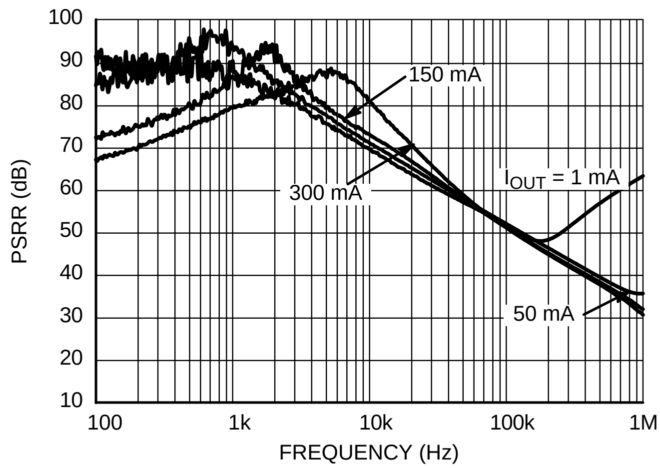


Figure 20. PSRR vs. Frequency, 3.6 V Version

TYPICAL CHARACTERISTICS

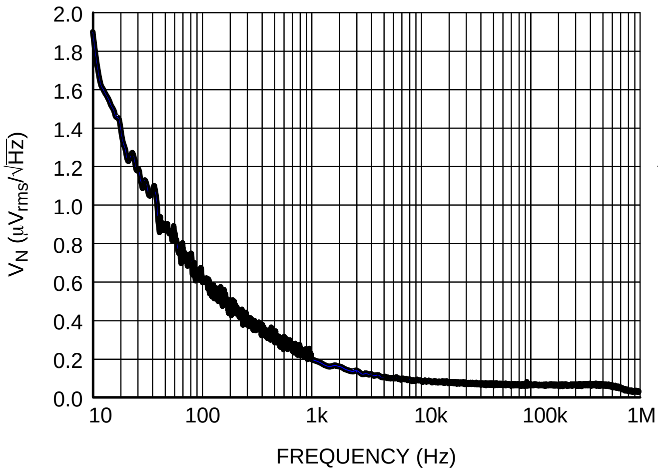


Figure 21. Output Noise vs. Frequency, 0.7 V Version

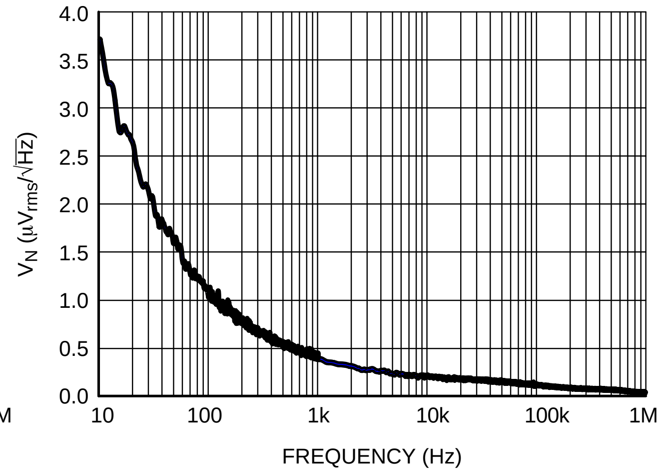


Figure 22. Output Noise vs. Frequency, 2.5 V Version

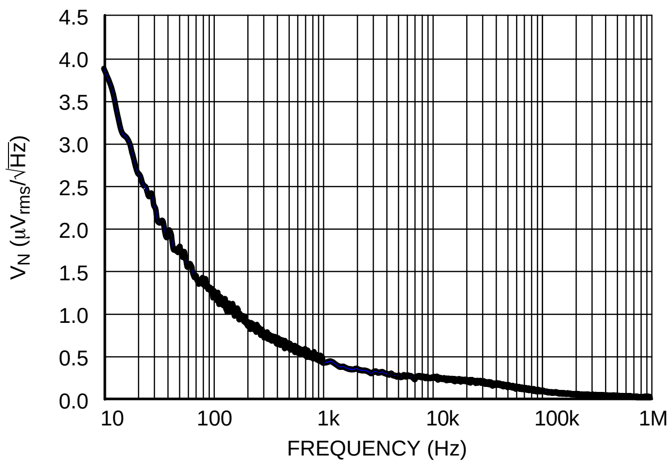


Figure 23. Output Noise vs. Frequency, 3.6 V Version

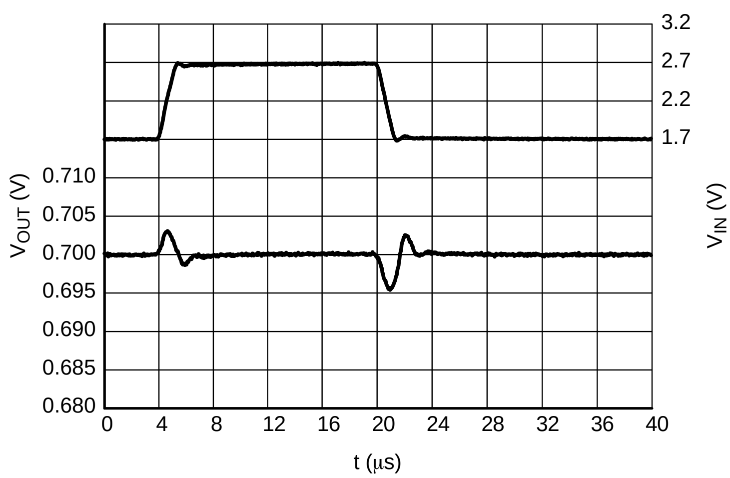


Figure 24. Line Transients, 0.7 V Version

TYPICAL CHARACTERISTICS

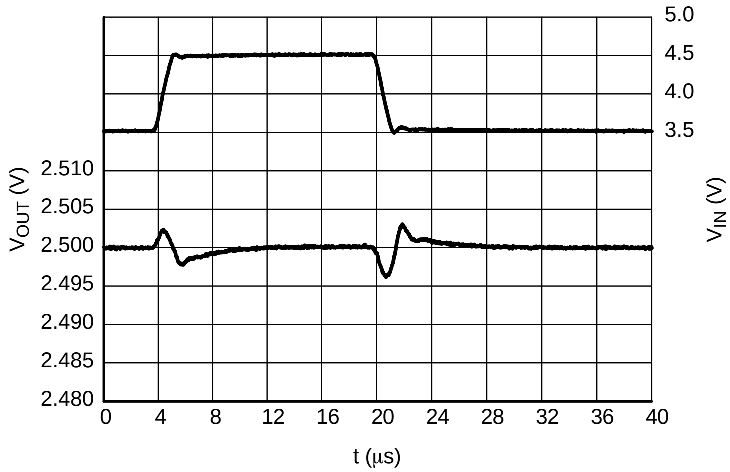


Figure 25. Line Transients, 2.5 V Version

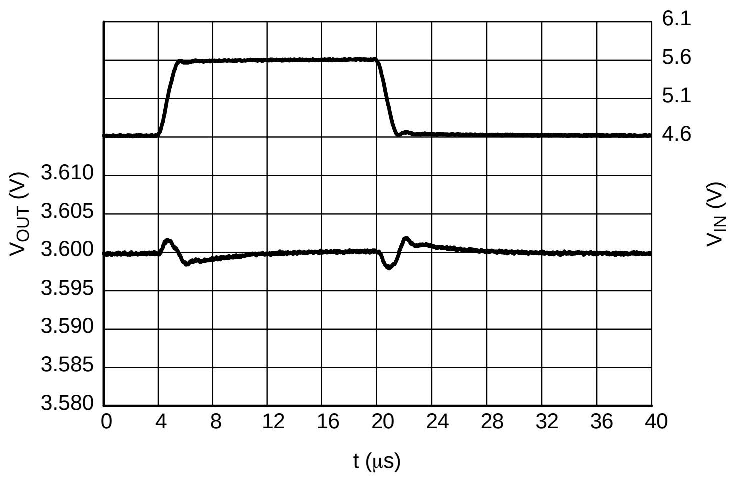


Figure 26. Line Transients, 3.6 V Version

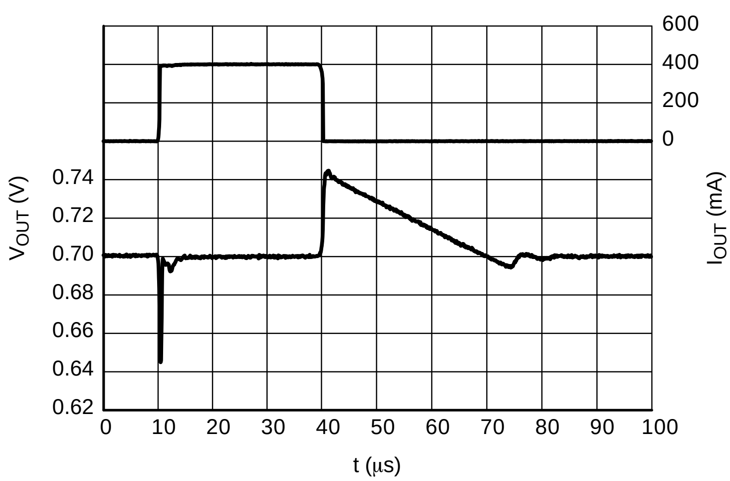


Figure 27. Load Transients, 0.7 V Version, Load Step 1 mA to 400 mA

TYPICAL CHARACTERISTICS

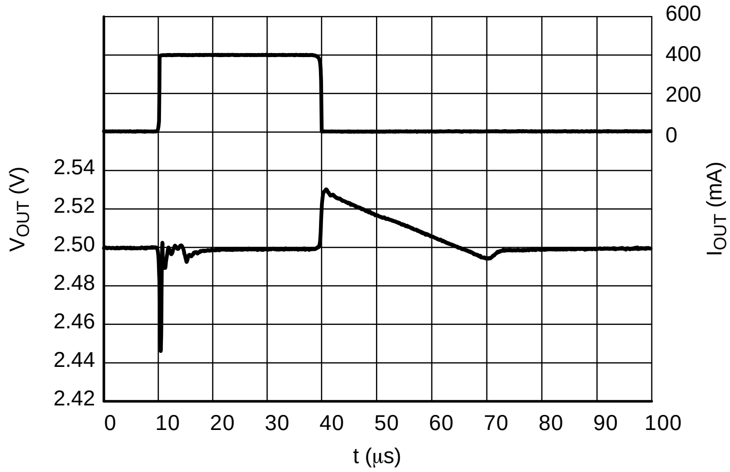


Figure 28. Load Transients, 2.5 V Version, Load Step 1 mA to 400 mA

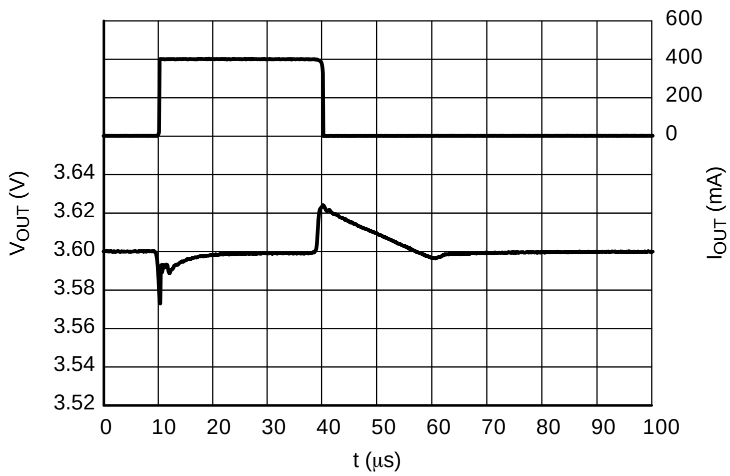


Figure 29. Load Transients, 3.6 V Version, Load Step 1 mA to 400 mA

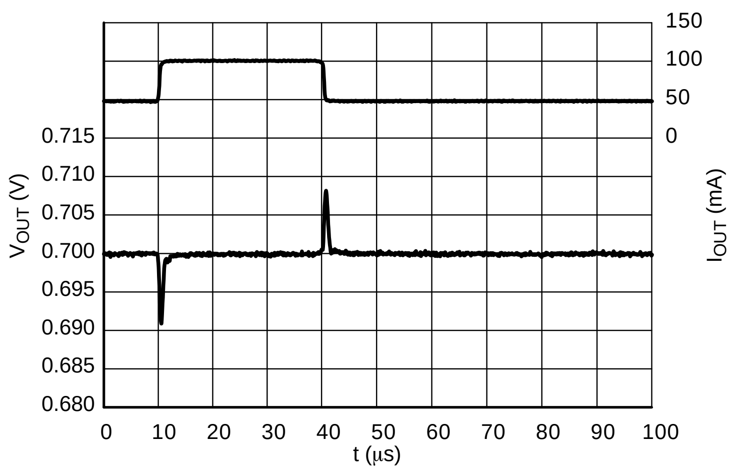


Figure 30. Load Transients, 0.7 V Version, Load Step 50 mA to 100 mA

TYPICAL CHARACTERISTICS

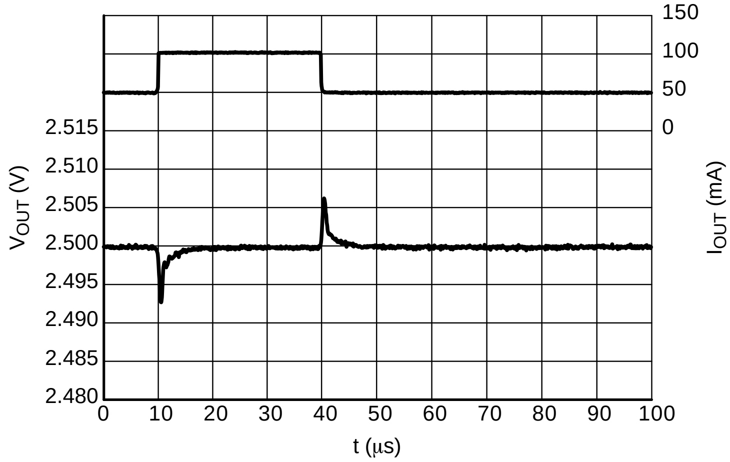


Figure 31. Load Transients, 2.5 V Version, Load Step 50 mA to 100 mA

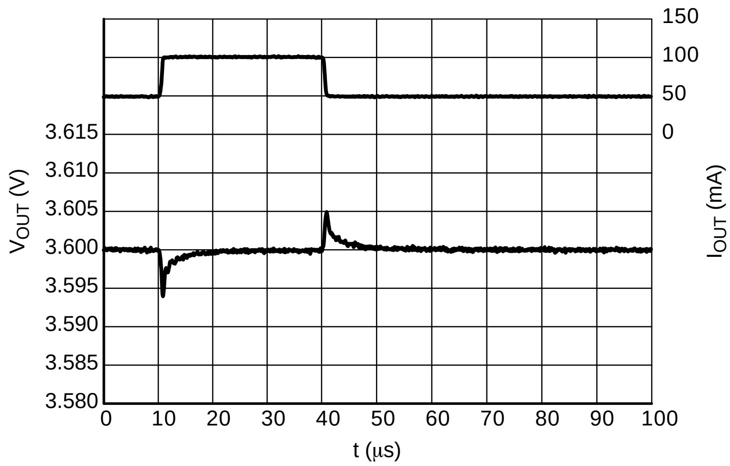


Figure 32. Load Transients, 3.6 V Version, Load Step 50 mA to 100 mA

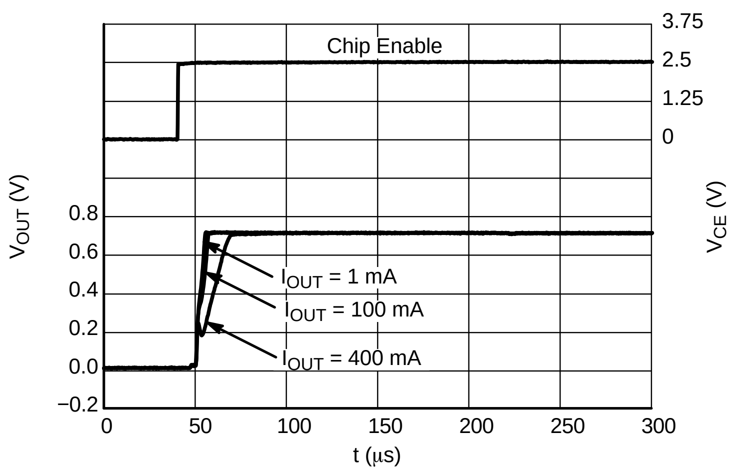


Figure 33. Turn On with CE Behavior, 0.7 V Version

TYPICAL CHARACTERISTICS

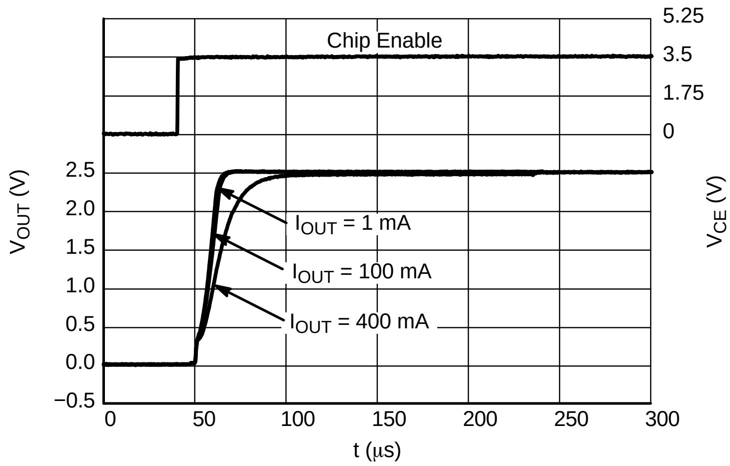


Figure 34. Turn On with CE Behavior, 2.5 V Version

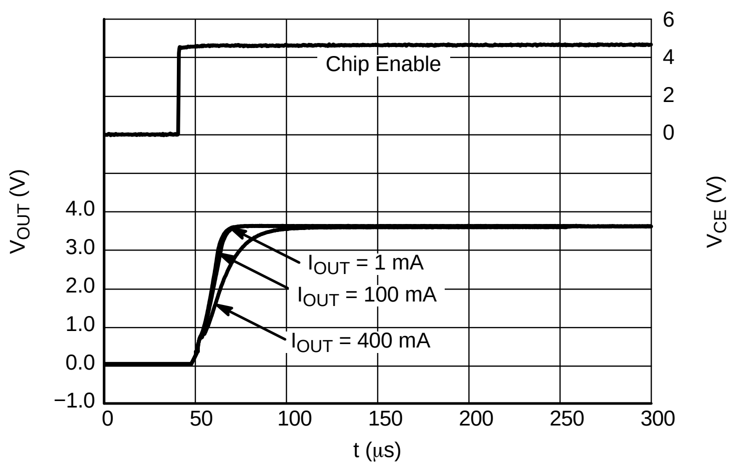


Figure 35. Turn On with CE Behavior, 3.6 V Version

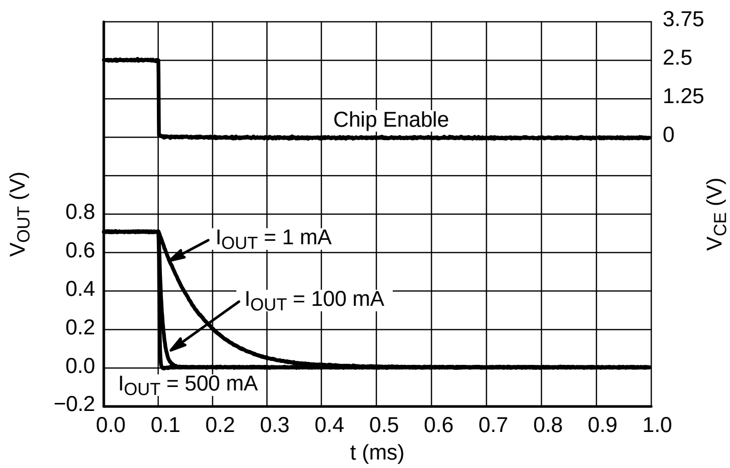


Figure 36. Turn Off with CE Behavior, 0.7 V Version

TYPICAL CHARACTERISTICS

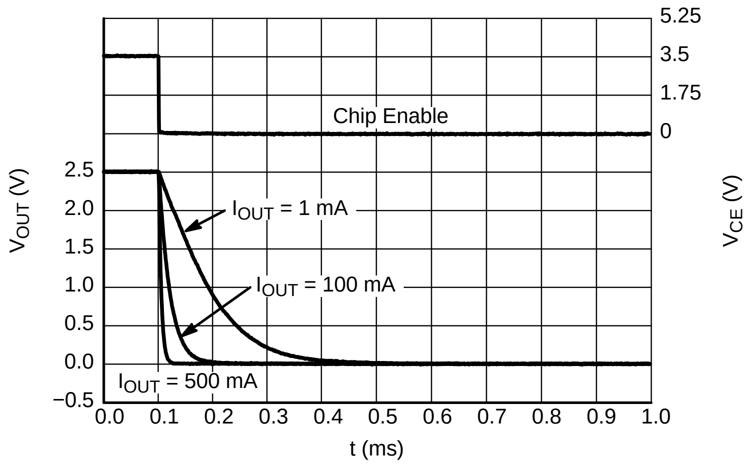


Figure 37. Turn Off with CE Behavior, 2.5 V Version

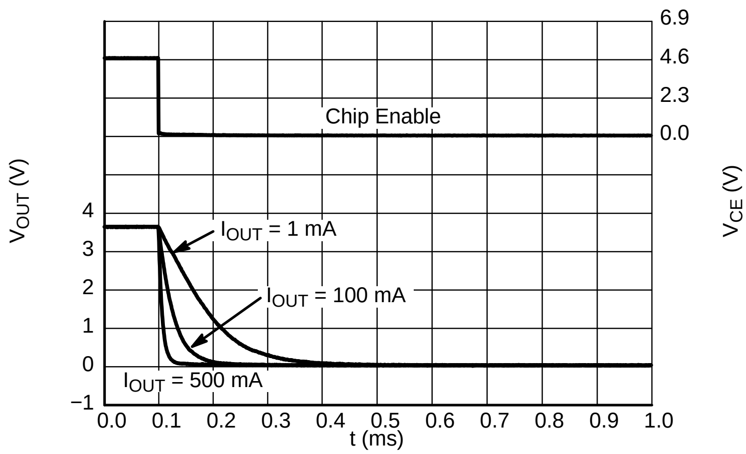


Figure 38. Turn Off with CE Behavior, 3.6 V Version

APPLICATION INFORMATION

A typical application circuit for NCP4687 series is shown in the Figure 39.

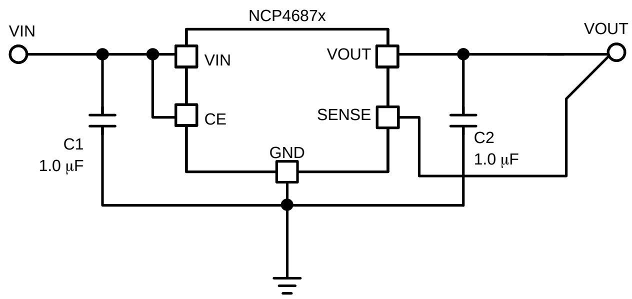


Figure 39. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 1.0 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4687 device. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 1.0 μF ceramic output decoupling capacitor is sufficient to achieve stable operation of the device. If tantalum capacitor is used, and its ESR is high, the loop oscillation may result. The capacitor should be connected as close as possible to the output and ground pin. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source which assure off state of LDO in case the CE pin will stay floating. If the enable function is not needed connect CE pin to V_{IN}.

The D version of the NCP4687 device includes a transistor between V_{OUT} and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal Consideration

As a power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

The IC includes internal thermal shutdown circuit that stops operation of regulator, if junction temperature is higher than 165°C. After that, when junction temperature decreases below 100°C, the operation of voltage regulator would restart. While high power dissipation condition is, the regulator starts and stops repeatedly and protects itself against overheating.

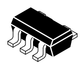
Sense Pin

The SENSE pin improves significantly the load regulation. The connection resistance between the LDO and the load given by PCB parameters has reduced impact to load regulation. If possible, use wide PCB traces as short as possible.

ORDERING INFORMATION

Device	Marking	Nominal Output Voltage	Feature	Package	Shipping†
NCP4687DH12T1G	A12D	1.2 V	Auto discharge	SOT−89 (Pb−Free)	1000 / Tape & Reel
NCP4687DH15T1G	A15D	1.5 V	Auto discharge	SOT−89 (Pb−Free)	1000 / Tape & Reel
NCP4687DH18T1G	A18D	1.8 V	Auto discharge	SOT−89 (Pb−Free)	1000 / Tape & Reel
NCP4687DH25T1G	A25D	2.5 V	Auto discharge	SOT−89 (Pb−Free)	1000 / Tape & Reel
NCP4687DH33T1G	A33D	3.3 V	Auto discharge	SOT−89 (Pb−Free)	1000 / Tape & Reel
NCP4687DMX18TCG	9P	1.8 V	Auto discharge	XDFN6 (Pb−Free)	5000 / Tape & Reel
NCP4687DMX25TCG	9X	2.5 V	Auto discharge	XDFN6 (Pb−Free)	5000 / Tape & Reel
NCP4687DMX33TCG	0G	3.3 V	Auto discharge	XDFN6 (Pb−Free)	5000 / Tape & Reel
NCP4687DSN18T1G	J18	1.8 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4687DSN25T1G	J25	2.5 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4687DSN28T1G	J28	2.8 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel

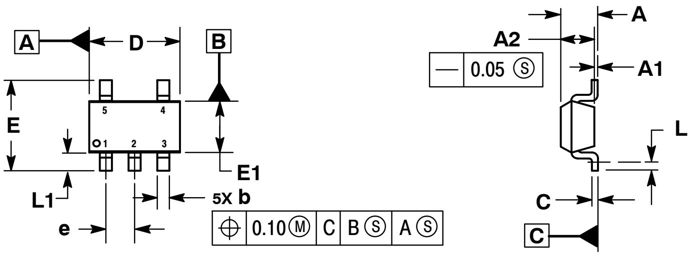
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

SOT−23 5−LEAD
CASE 1212−01
ISSUE A

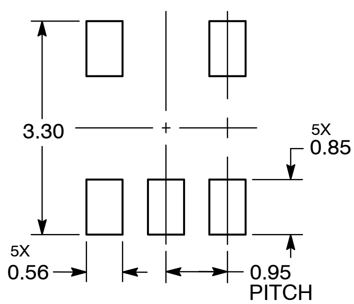
DATE 28 JAN 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

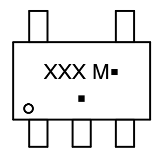
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

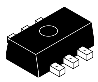
GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

DOCUMENT NUMBER:	98ASH70518A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT−23 5−LEAD	PAGE 1 OF 1

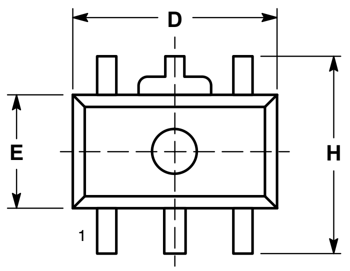


SCALE 2:1

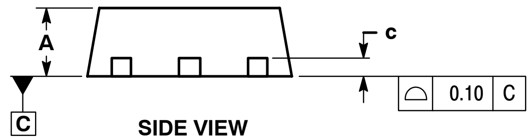
SOT−89, 5 LEAD

CASE 528AB−01
ISSUE O

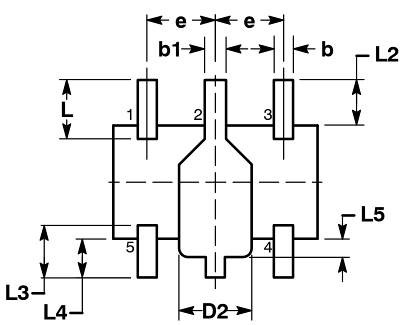
DATE 23 NOV 2009



TOP VIEW



SIDE VIEW

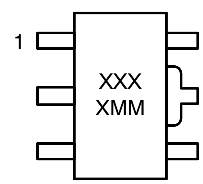


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS INCLUDES LEAD FINISH.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSIONS L, L2, L3, L4, L5, AND H ARE MEASURED AT DATUM PLANE C.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	1.40	1.60
b	0.32	0.52
b1	0.37	0.57
c	0.30	0.50
D	4.40	4.60
D2	1.40	1.80
E	2.40	2.60
e	1.40	1.60
H	4.25	4.45
L	1.10	1.50
L2	0.80	1.20
L3	0.95	1.35
L4	0.65	1.05
L5	0.20	0.60

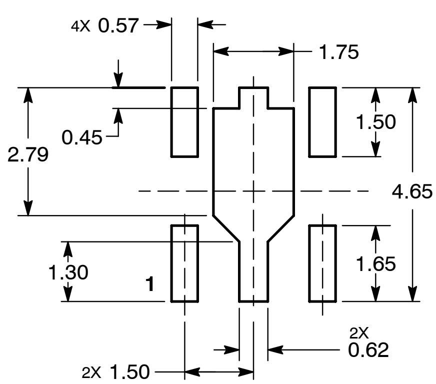
GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
MM = Lot Number
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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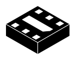
DESCRIPTION:	**SOT−89, 5 LEAD**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

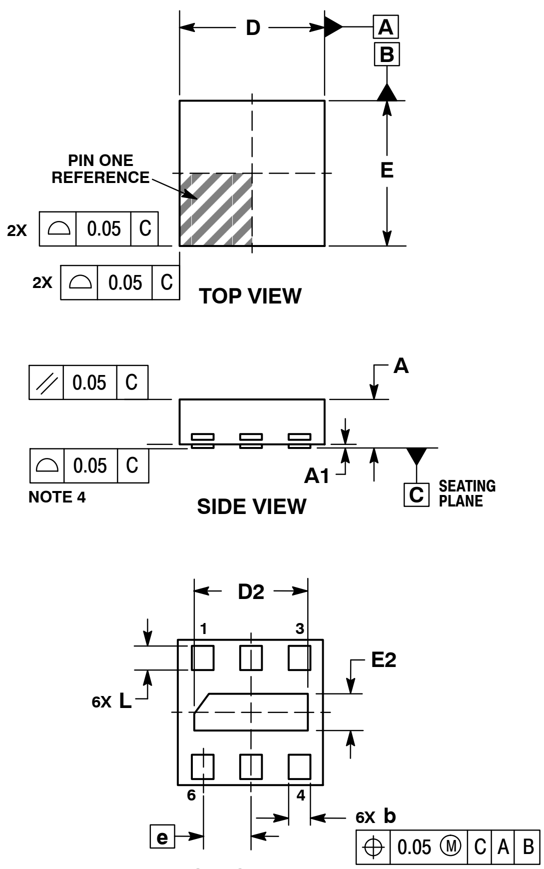
ON Semiconductor®



SCALE 4:1

XDFN6 1.20x1.20, 0.40P
CASE 711AH
ISSUE O

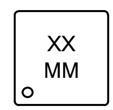
DATE 14 SEP 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25mm FROM TERMINAL TIPS.
4. COPLANARITY APPLIES TO ALL OF THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.13	0.23
D	1.20 BSC	
D2	0.89	0.99
E	1.20 BSC	
E2	0.25	0.35
e	0.40 BSC	
L	0.15	0.25
L1	0.05 BSC	

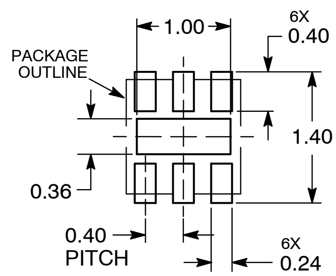
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
MM = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	XDFN6, 1.20 X 1.20, 0.40P	PAGE 1 OF 1

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