



STL60N32N3LL

Dual N-channel 30 V, 0.005 Ω , 15 A PowerFLAT™ 5x6 asymmetrical double island, STripFET™ Power MOSFET

Features

Order code		V _{DSS}	R _{DS(on)}	I _D
STL60N32N3LL	Q ₁	30 V	< 0.0092 Ω	13.6 A
	Q ₂	30 V	< 0.0055 Ω	15 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Application

- Switching applications

Description

This device is a dual N-channel Power MOSFET which utilizes the latest generation of design rules for ST's proprietary STripFET™ V and STripFET™ VI DeepGATE™ technology. The lowest available RDS(on)* Qg in this chip scale package renders the device suitable for the most demanding DC-DC converter applications, where high power density is required.

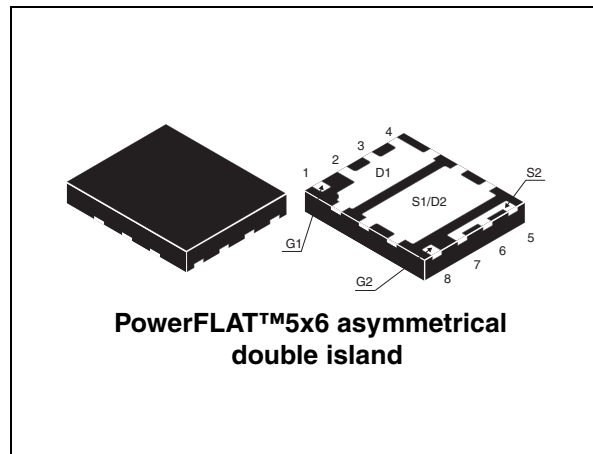


Figure 1. Internal schematic diagram

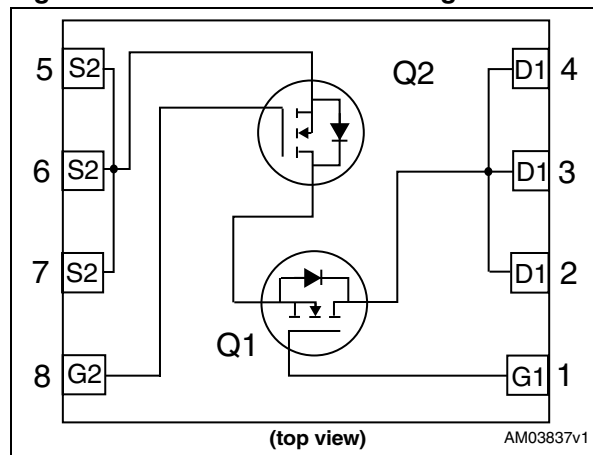


Table 1. Device summary

Order code	Marking	Package	Packaging
STL60N32N3LL	60N32N3LL	PowerFLAT™ 5x6 asymmetrical double island	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Type	Value	Unit
V_{DS}	Drain-source voltage	Q ₁	30	V
		Q ₂	30	V
V_{GS}	Gate- source voltage	Q ₁	± 20	V
		Q ₂	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	Q ₁	32	A
		Q ₂	60	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	Q ₁	23	A
		Q ₂	37	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	Q ₁	13.6	A
		Q ₂	15	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	Q ₁	8.5	A
		Q ₂	9.3	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	Q ₁	54.4	A
		Q ₂	60	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	Q ₁	23	W
		Q ₂	50	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ °C}$	Q ₁	3.12	W
		Q ₂	3.12	W
T_j	Operating junction temperature		-55 to 150	°C
T_{stg}	Storage temperature			

1. This value is according to R_{thj-c}
2. This value is according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Type	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max		40	°C/W
R_{thj-c}	Thermal resistance junction-case	Q ₁	5.5	°C/W
		Q ₂	2.5	

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	Q ₁	30			V
			Q ₂	30			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = 30 V$	Q ₁			1	μA
			Q ₂			1	μA
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = 30 V, T_C = 125^{\circ}C$	Q ₁			10	μA
			Q ₂			10	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$	Q ₁			± 100	nA
			Q ₂			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	Q ₁	1			V
			Q ₂	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 6.8 A$ $V_{GS} = 10 V, I_D = 7.5 A$	Q ₁		0.0085	0.0092	Ω
			Q ₂		0.005	0.0055	Ω
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5 V, I_D = 6.8 A$ $V_{GS} = 4.5 V, I_D = 7.5 A$	Q ₁		0.0109	0.012	Ω
			Q ₂		0.0065	0.0073	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0$	Q ₁	-	950	-	pF
			Q ₂	-	1690	-	pF
C_{OSS}	Output capacitance		Q ₁	-	193	-	pF
			Q ₂	-	291	-	pF
C_{RSS}	Reverse transfer capacitance		Q ₁	-	27.6	-	pF
			Q ₂	-	176	-	pF
Q_g	Total gate charge	$V_{DD} = 15 V, I_D = 15 A, V_{GS} = 4.5 V$ (see Figure 25)	Q ₁	-	6.6	-	nC
Q_{gs}	Gate-source charge		Q ₁	-	3.3	-	nC
			Q ₂	-	8	-	nC
Q_{gd}	Gate-drain charge		Q ₁	-	2.4	-	nC
			Q ₂	-	6	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 29)	Q_1 Q_2	-	10.8 9.5	-	ns ns
t_r	Rise time	$V_{GS}=4.5\text{ V}$ (see Figure 29)	Q_1 Q_2	-	15.6 30	-	ns ns
$t_{d(off)}$	Turn-off delay time	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 29)	Q_1 Q_2	-	14.2 37	-	ns ns
t_f	Fall time	$V_{GS}=4.5\text{ V}$ (see Figure 29)	Q_1 Q_2	-	6 12	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$	Q_1 Q_2	-		13.6 15	A A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$	Q_1 Q_2	-		54.4 60	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=15\text{ A}$, $V_{GS}=0$	Q_1 Q_2	-		1.1 1.1	V V
t_{rr}	Reverse recovery time	$I_{SD}=15\text{ A}$, $V_{DD}=15\text{ V}$	Q_1 Q_2	-	20 24		ns ns
Q_{rr}	Reverse recovery charge	$di/dt=100\text{ A}/\mu\text{s}$, $T_j=150^\circ\text{C}$ (see Figure 29)	Q_1 Q_2	-	10 16.8		nC nC
I_{RRM}	Reverse recovery current	$T_j=150^\circ\text{C}$ (see Figure 29)	Q_1 Q_2	-	1 1.4		A A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

2.1.1 Graphs for Q1

Figure 2. Safe operating area

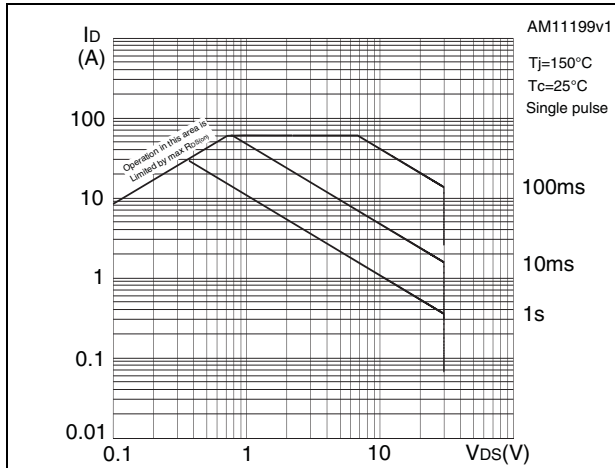


Figure 3. Thermal impedance

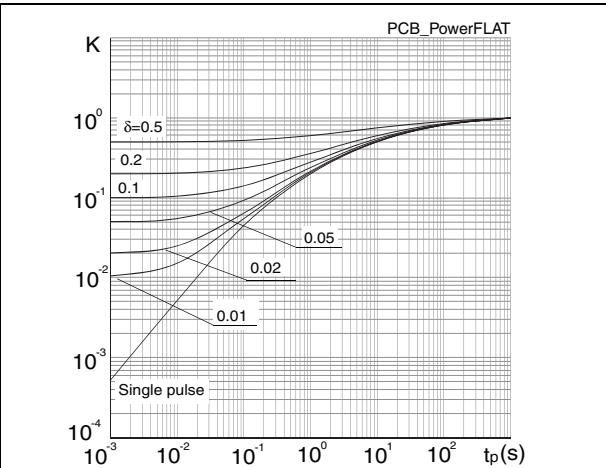


Figure 4. Output characteristics

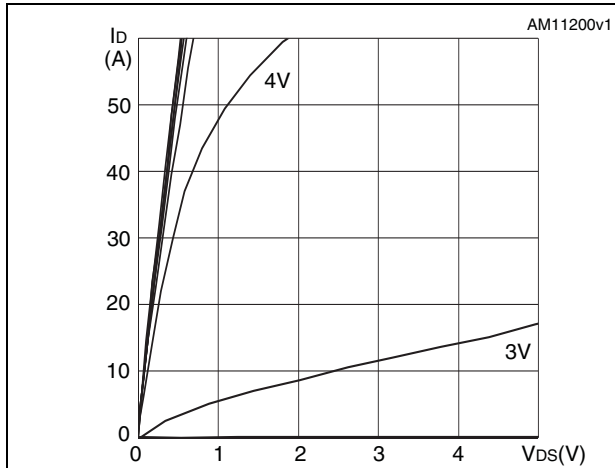


Figure 5. Transfer characteristics

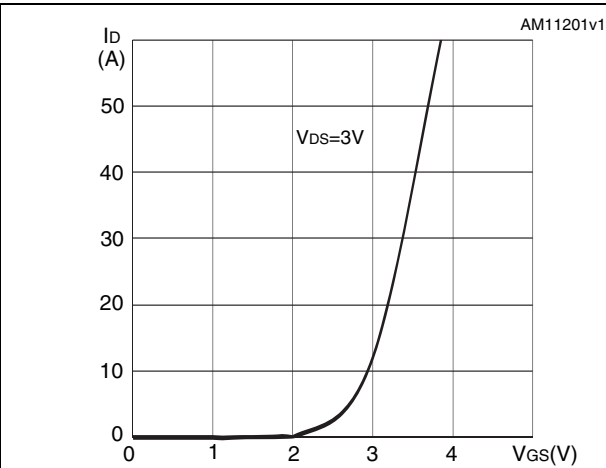


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

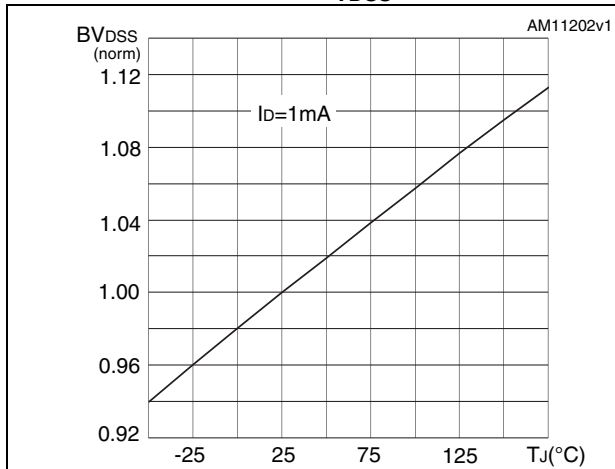


Figure 7. Static drain-source on resistance

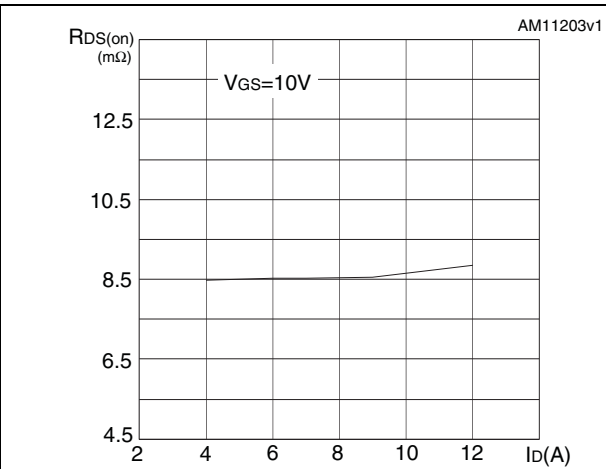


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

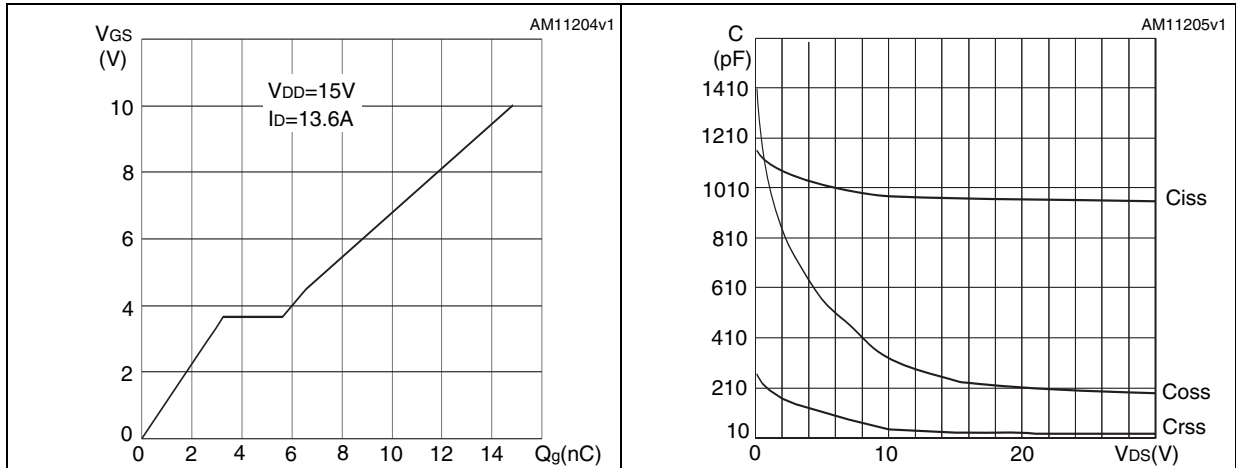


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

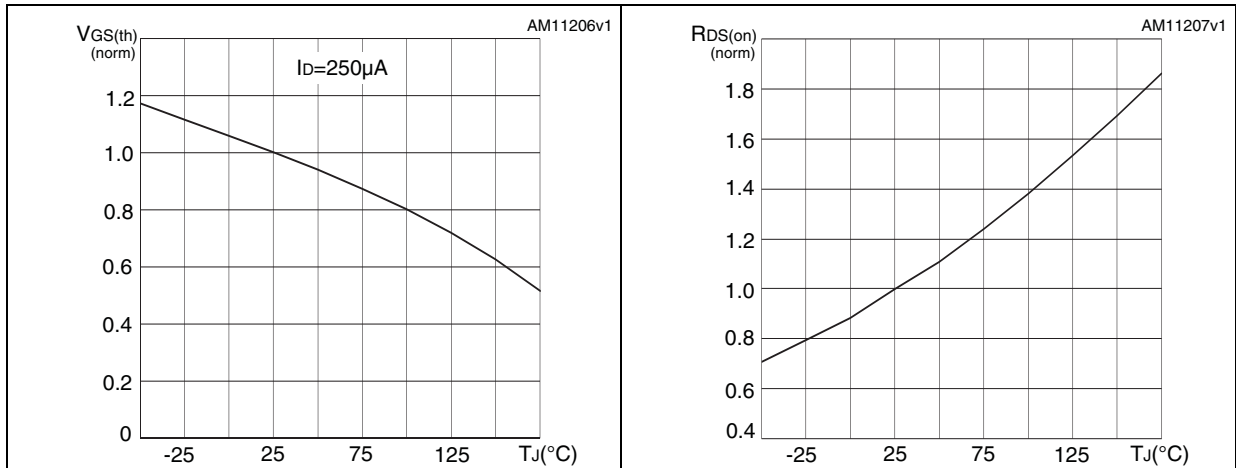
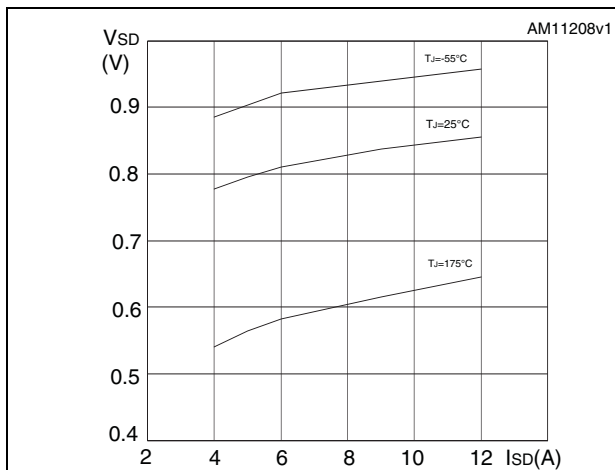


Figure 12. Source-drain diode forward characteristics



2.1.2 Graphs for Q2

Figure 13. Safe operating area

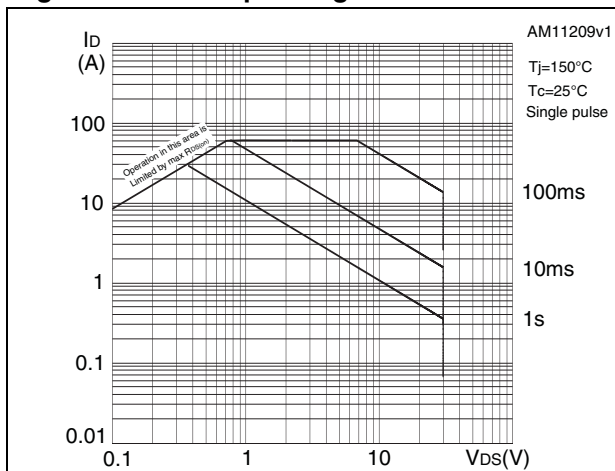


Figure 14. Thermal impedance

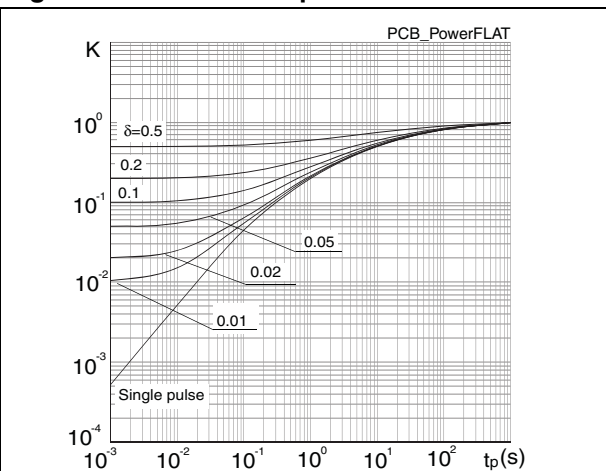


Figure 15. Output characteristics

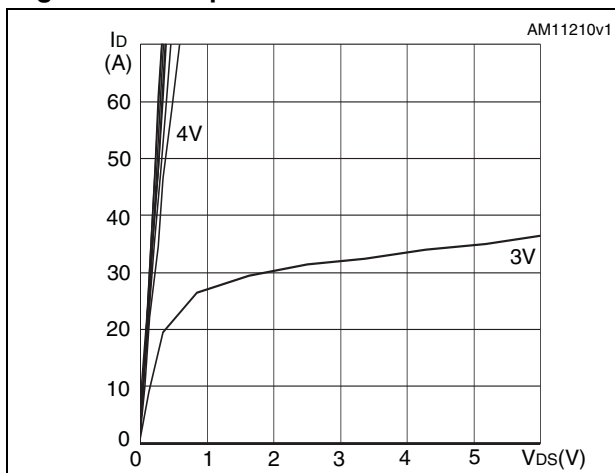


Figure 16. Transfer characteristics

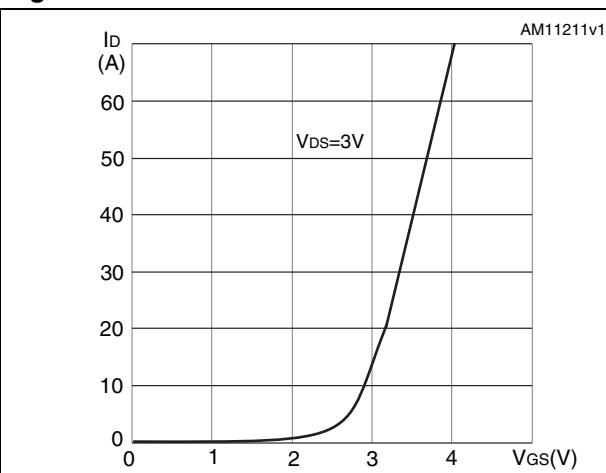


Figure 17. Normalized $B_{V_{DSS}}$ vs temperature

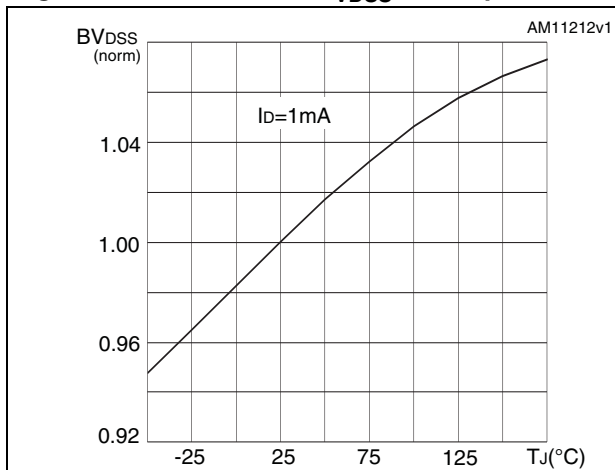


Figure 18. Static drain-source on resistance

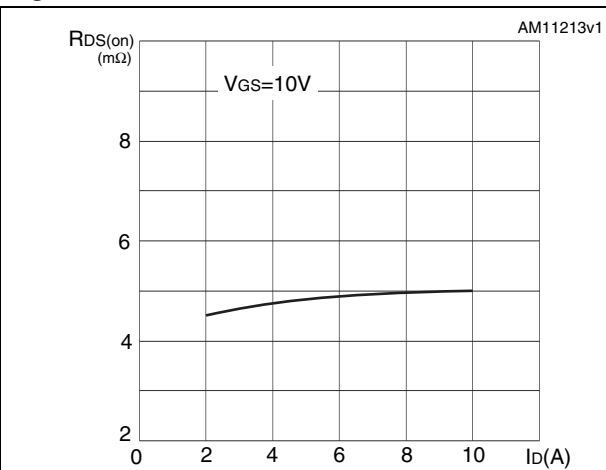


Figure 19. Gate charge vs gate-source voltage Figure 20. Capacitance variations

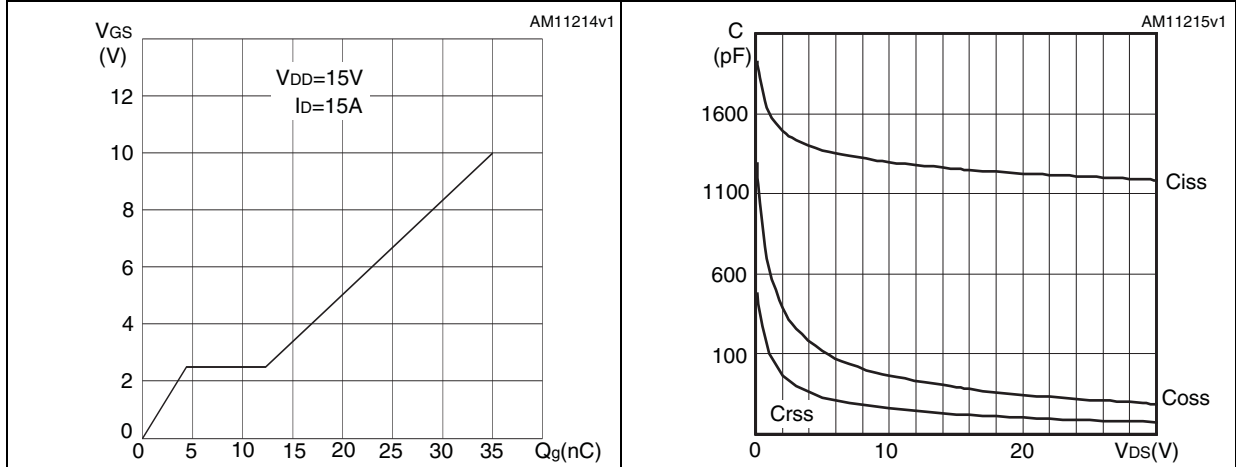


Figure 21. Normalized gate threshold voltage vs temperature Figure 22. Normalized on resistance vs temperature

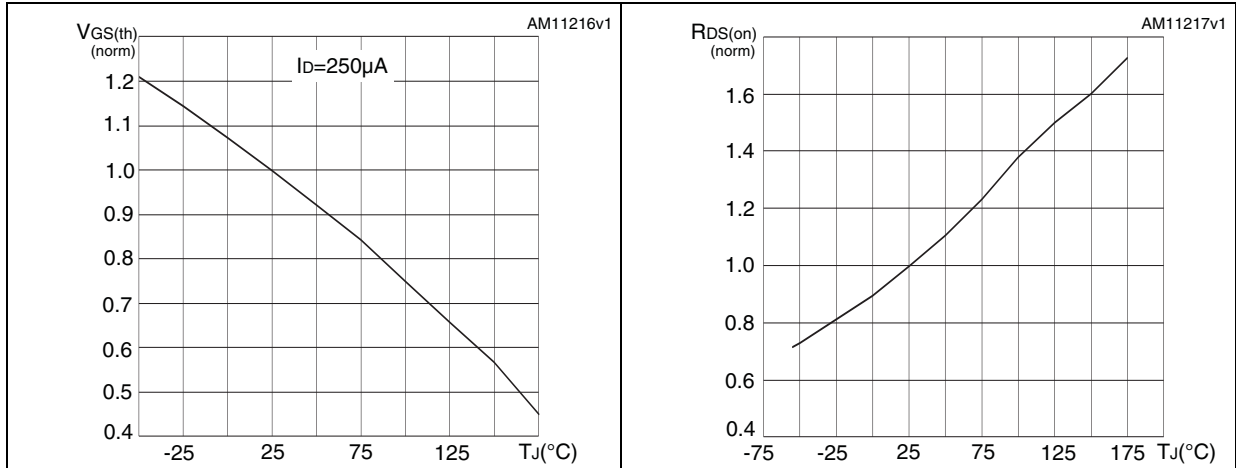
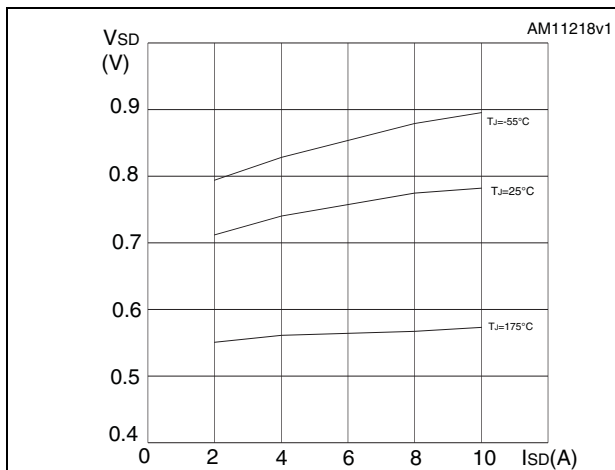


Figure 23. Source-drain diode forward characteristics



3 Test circuits

Figure 24. Switching times test circuit for resistive load

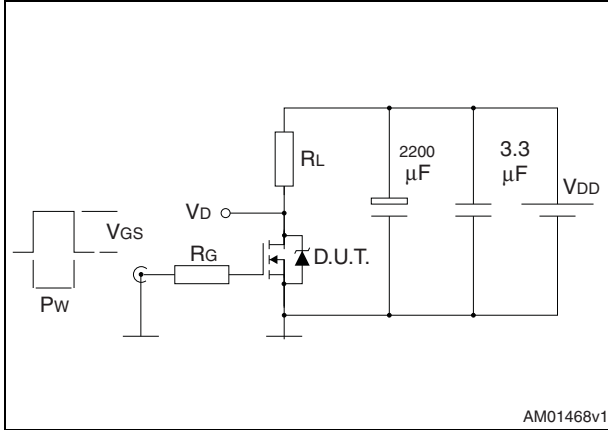


Figure 25. Gate charge test circuit

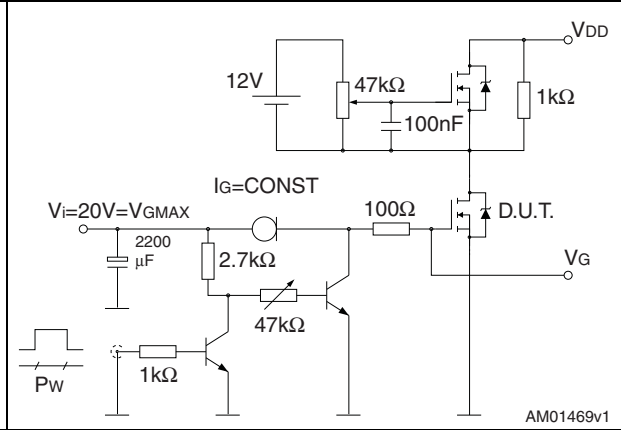


Figure 26. Test circuit for inductive load switching and diode recovery times

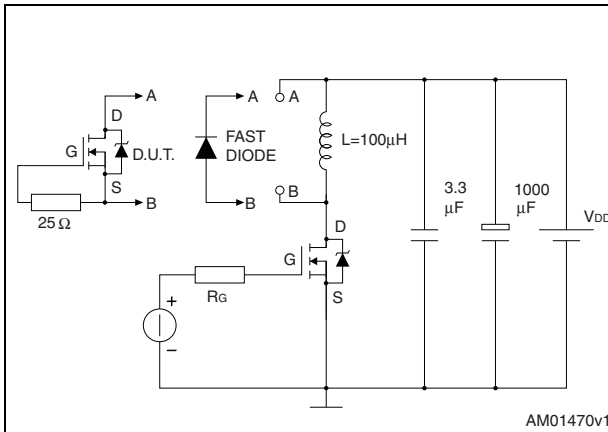


Figure 27. Unclamped inductive load test circuit

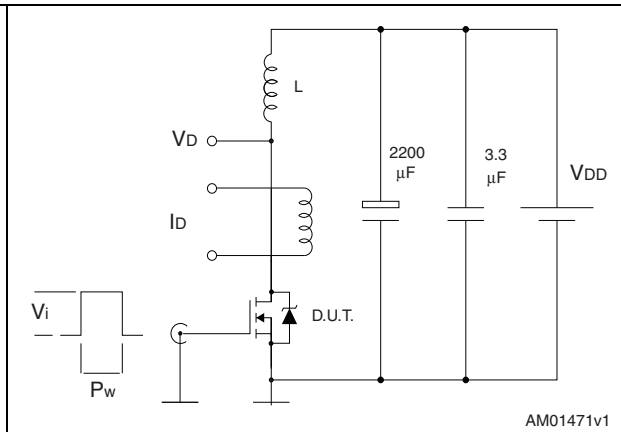


Figure 28. Unclamped inductive waveform

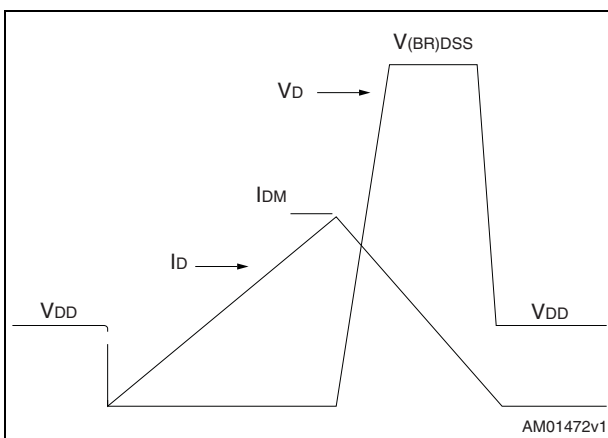
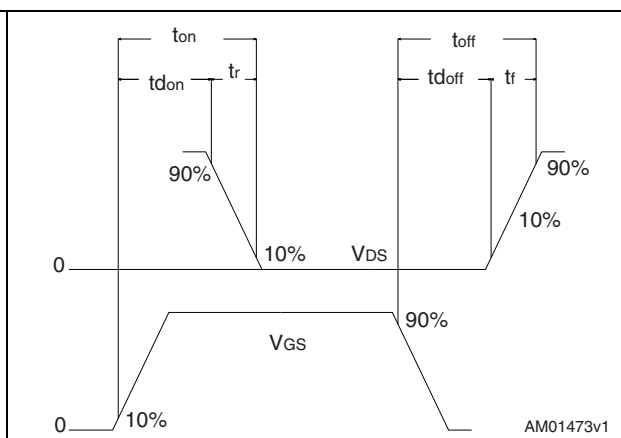


Figure 29. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 asymmetrical double island dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1			0.05
b	0.45		0.55
D	4.90	5.00	5.10
E	5.90	6.00	6.10
e		1.27	
L	0.40		0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 30. Package drawing

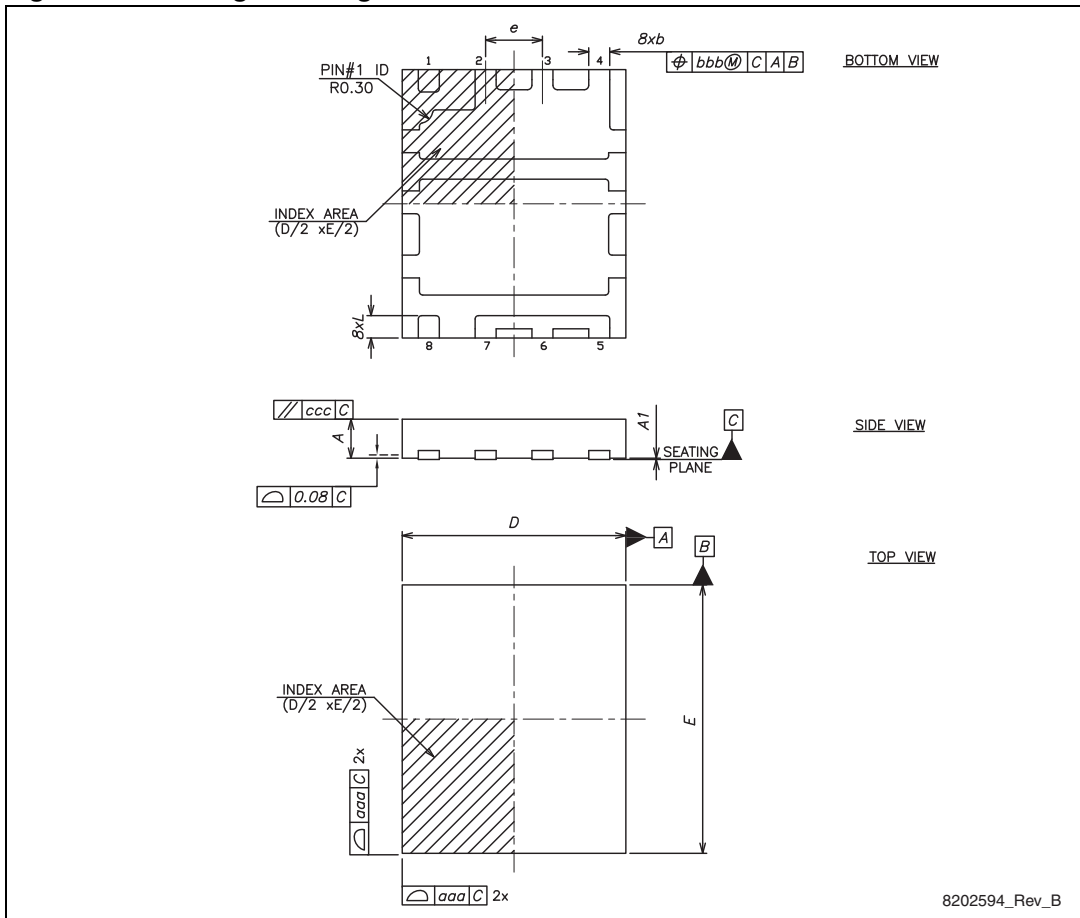
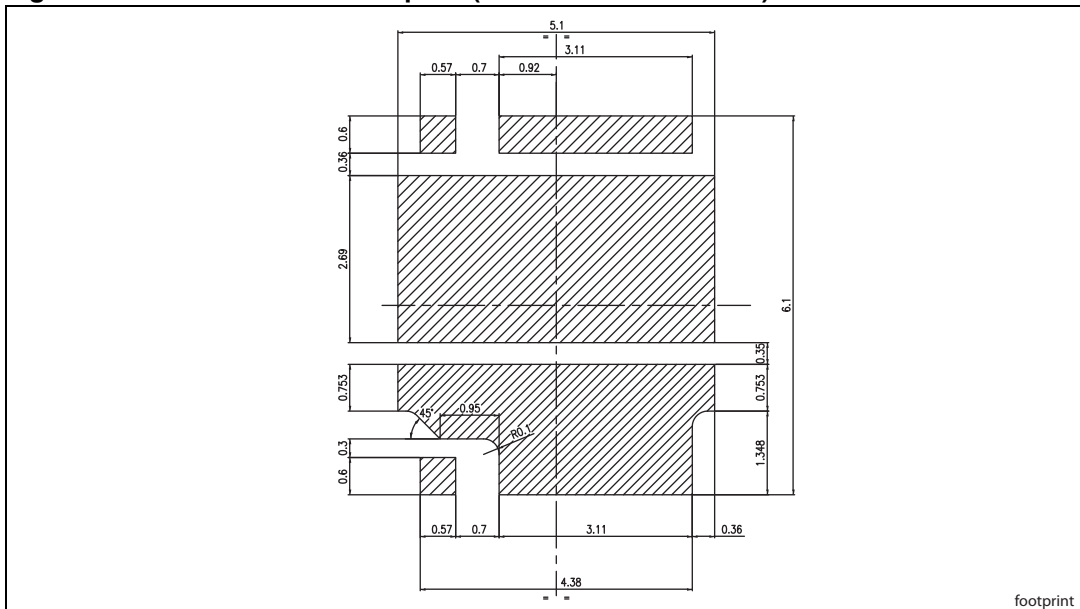


Figure 31. Recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Mar-2010	1	First release
07-Feb-2011	2	Document status promoted from target specification to preliminary data.
21-Feb-2012	3	Document status promoted from preliminary data to datasheet. <i>Section 2.1: Electrical characteristics (curves)</i> has been added. <i>Section 4: Package mechanical data</i> has been updated. Minor text changes.

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