

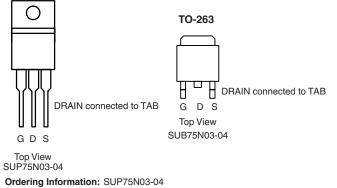
### SUP/SUB75N03-04

### **Vishay Siliconix**

## N-Channel 30-V (D-S), 175 °C MOSFET

PRODUCT SUMMARY			
V <sub>(BR)DSS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	
30	0.004	75 <sup>a</sup>	

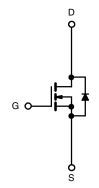
#### **TO-220AB**



**FEATURES** TrenchFET<sup>®</sup> Power MOSFETs

175 °C Rated Maximum Junction • Temperature





SUP75N03-04-E3 (Lead (Pb)-free) SUB75N03-04 SUB75N03-04-E3 (Lead (Pb)-free)

N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATING</b>	<b>S</b> $T_C = 25 \ ^{\circ}C$ , unless otherwis	e noted			
Parameter Gate-Source Voltage		Symbol	Limit ± 20	Unit V	
		V <sub>GS</sub>			
Continuous Drain Current (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	75 <sup>a</sup>		
	T <sub>C</sub> = 125 °C		75 <sup>a</sup>		
Pulsed Drain Current		I <sub>DM</sub>	250	A	
Pulse Diode Forward Current		I <sub>SM</sub>	250		
Continuous Source Current (Diode Conduction)		۱ <sub>S</sub>	75		
Avalanche Current		I <sub>AR</sub>	75		
Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	280		
Repetitive Avalanche Energy <sup>b</sup>	L = 0.05 mH	E <sub>AR</sub>	140	- mJ	
Maximum Power Dissipation	$T_{C}$ = 25 °C (TO-220AB and TO-263)	P <sub>D</sub>	187 <sup>c</sup>	w	
	T <sub>A</sub> = 25 °C (TO-263) <sup>d</sup>		3.7		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175		
Lead Temperature $(^{1}/_{16})^{"}$ from case for 10 sec.)	TO-220AB	Τ <sub>L</sub>	300	- °C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Limit	Unit	
Junction-to-Ambient	PCB Mount (TO-263) <sup>d</sup>	R <sub>thJA</sub>	40	°C/W	
	Free Air (TO-220AB)		62.5		
Junction-to-Case		R <sub>thJC</sub>	0.6		

Notes:

a. Package limited.

b. Duty cycle  $\leq$  1 %.

c. See SOA curve for voltage derating. d. When Mounted on 1" square PCB (FR-4 material).

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

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Parameter	Symbol	Test Conditions	Min	Тур <sup>а</sup>	Max	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1		3	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 500	nA
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μΑ
	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$			50	
		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$			200	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 V, V_{GS} = 10 V$	120			А
Drain-Source On-State Resistance <sup>b</sup>		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 75 A		0.0034	0.004	Ω
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 75 \text{ A}$		0.005	0.006	
	r <sub>DS(on)</sub>	$V_{GS}$ = 10 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 125 °C			0.006	
		$V_{GS}$ = 10 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 175 °C			0.008	
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A	30			S
Dynamic					1	
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		10742		pF
Output Capacitance	C <sub>oss</sub>			1811		
Reverse Transfer Capacitance	C <sub>rss</sub>			775		
Total Gate Charge	Qg	$V_{DS} = 30$ V, $V_{GS} = 10$ V, $I_D = 75$ A		200	250	nC
Gate-Source Charge	Q <sub>gs</sub>			40		
Gate-Drain Charge	Q <sub>gd</sub>			40		
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD}$ = 30 V, R <sub>L</sub> = 0.6 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 2.5 Ω		20	40	- ns
Rise Time	t <sub>r</sub>			40		
Turn-Off Delay Time	t <sub>d(off)</sub>			190		
Fall Time	t <sub>f</sub>			95		
Source-Drain Diode Ratings and Cha	aracteristics					
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V			1.3	V
Reverse Recovery Time	t <sub>rr</sub>			70	120	ns
Peak Reverse Recovery Current	I <sub>RM(rec)</sub>	l <sub>F</sub> = 50 A, di/dt = 100 A/μs		2.8	6	А
Reverse Recovery Charge	Q <sub>rr</sub>			0.1	0.36	μC

Notes:

a. For design aid only; not subject to production testing.

b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

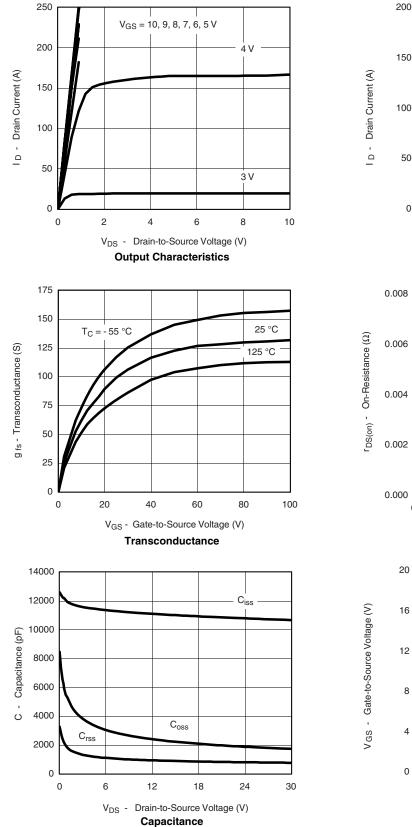
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

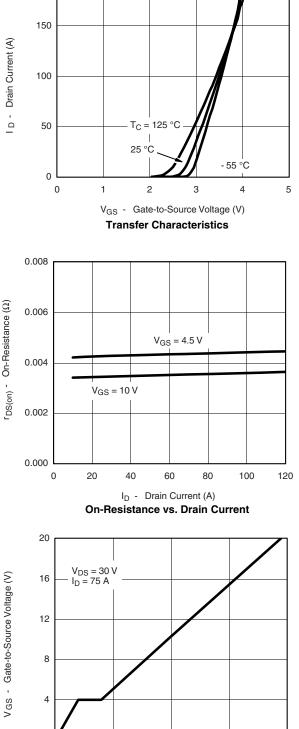


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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





0

100

200

Qg - Total Gate Charge (nC)

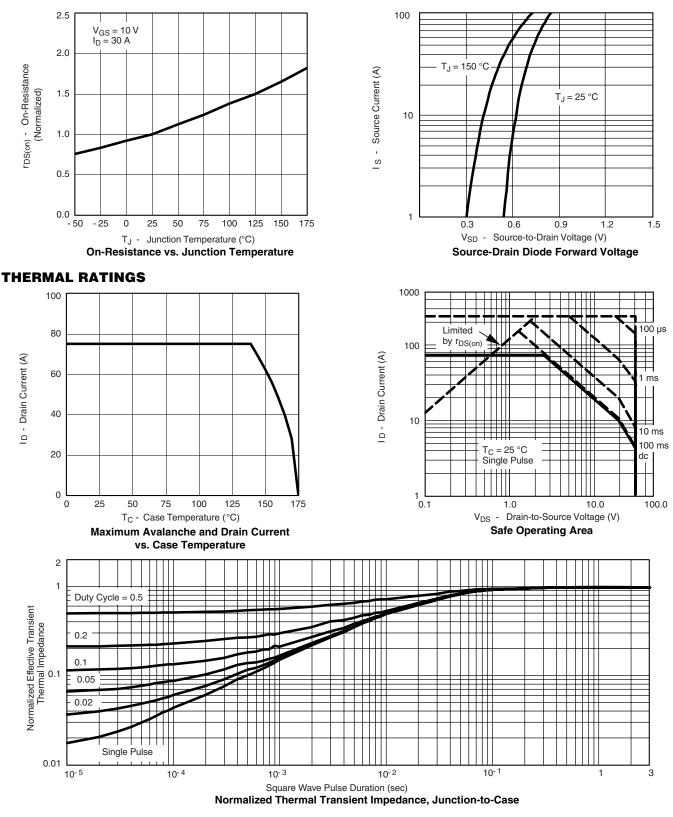
Gate Charge

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300

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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70745.

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