

STS5DNF20V

N-channel 20 V, 0.030 Ω typ, 5 A STripFETTM II Power MOSFET in a SO-8 package

Datasheet - production data

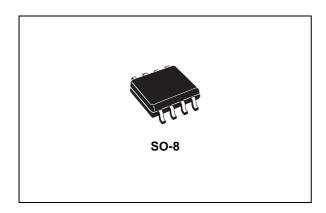
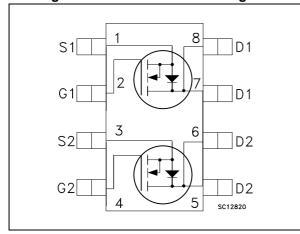


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D
STS5DNF20V	20 V	0.040 Ω @ 4.5 V	5 A
0100DN120V	20 V	0.045 Ω @ 2.7 V	37

- Ultra low threshold gate drive (2.7 V)
- Standard outline for easy automated surface mount assembly

Applications

• Switching application

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1. Device summary

Order code	Marking	Package	Packaging
STS5DNF20V	5DF20V	SO-8	Tape and reel

Contents STS5DNF20V

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STS5DNF20V Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	20	V
V _{GS}	Gate-source voltage	±12	V
I _D	Drain current (continuous) at T _C = 25 °C	5	Α
I _D	Drain current (continuous) at T _C = 100 °C	3	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	20	Α
P _{TOT}	Total dissipation at T _C = 25 °C (dual operation)	1.6	W
P _{TOT}	Total dissipation at T _C = 25 °C (single operation)	2	W
T _J	Max. operating junction temperature -55 to 150		°C
T _{stg}	Storage temperature	-55 (0 150	

^{1.} Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
D	Thermal resistance junction-ambient single operation	62.5	°C/W
R _{thj-a}	Thermal resistance junction-ambient dual operation	78	°C/W

Electrical characteristics STS5DNF20V

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$	20			٧
1	Zero gate voltage	V _{DS} = 20			1	μΑ
I _{DSS}	Drain current (V _{GS} = 0)	V _{DS} = 20 V, T _C =125 °C			10	μΑ
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 12 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6			Ω
R _{DS(on)}	Static drain-source	$V_{GS} = 4.5 \text{ V}, I_D = 2.5 \text{ A}$		0.030	0.040	Ω
	on- resistance	$V_{GS} = 2.7 \text{ V}, I_D = 2.5 \text{ A}$		0.037	0.045	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	V 05.V (4.MI)	-	460		pF
C _{oss}	Output capacitance	$V_{DS} = 25 \text{ V, f} = 1 \text{ MHz,}$ $V_{GS} = 0$	-	200		pF
C _{rss}	Reverse transfer capacitance	VGS = 0	-	50		pF
Qg	Total gate charge	V _{DD} = 16 V, I _D = 5 A,	-	8.5	11.5	nC
Q _{gs}	Gate-source charge	V _{GS} = 4.5 V	-	1.8		nC
Q _{gd}	Gate-drain charge	(see Figure 13)	-	2.4		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time		-	7	-	ns
t _r	Rise time	V_{DD} =10 V, I_{D} =2.5A, R_{G} =4.7 Ω , V_{GS} = 4.5V	-	33	-	ns
t _{d(off)}	Turn-off delay time	(see <i>Figure 12</i>)	-	27	-	ns
t _f	Fall Time		-	10	-	ns

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Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current		-		5	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		20	Α
V _{SD} (2)	Forward on voltage	I _{SD} = 5 A, V _{GS} = 0	-		1.2	V
t _{rr}	Reverse recovery time	$I_{SD} = 5 \text{ A}, V_{DD} = 10 \text{ V},$	-	26		ns
Q _{rr}	Reverse recovery charge	di/dt = 100 A/µs, T _i = 150 °C	-	13		nC
I _{RRM}	Reverse recovery current	(see <i>Figure 14</i>)	-	1		Α

^{1.} Pulse width limited by safe operating area.



^{2.} Pulsed: pulse duration = $300 \mu s$, duty cycle 1.5%

Electrical characteristics STS5DNF20V

Electrical characteristics (curves) 2.1

Figure 2. Safe operating area

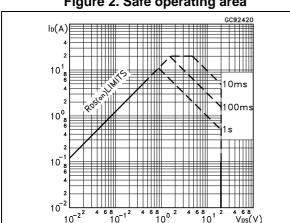


Figure 3. Thermal impedance

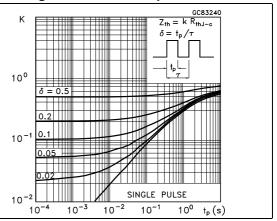


Figure 4. Output characteristics

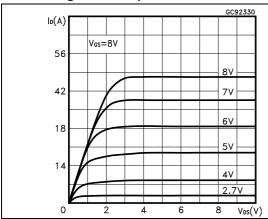


Figure 5. Transfer characteristics

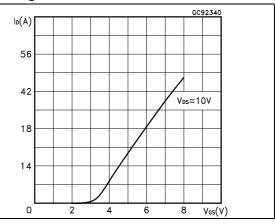
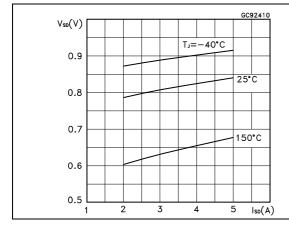
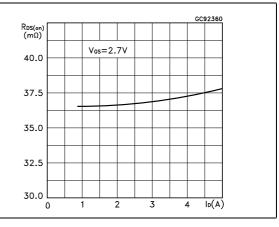


Figure 6. Source-drain diode forward characteristics

Figure 7. Static drain-source on resistance





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Figure 8. Gate charge vs gate-source voltage

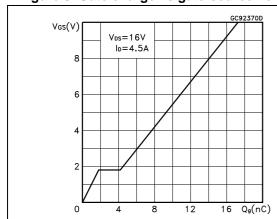


Figure 9. Capacitance variations

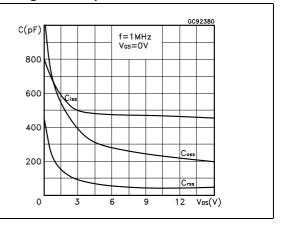


Figure 10. Normalized gate threshold voltage vs temperature

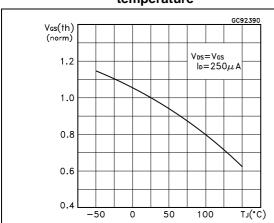
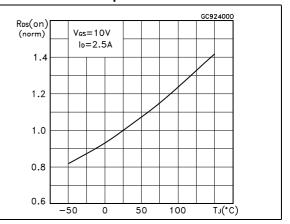


Figure 11. Normalized on-resistance vs temperature



Test circuit STS5DNF20V

3 Test circuit

Figure 12. Switching times test circuit for resistive load

Figure 13. Gate charge test circuit

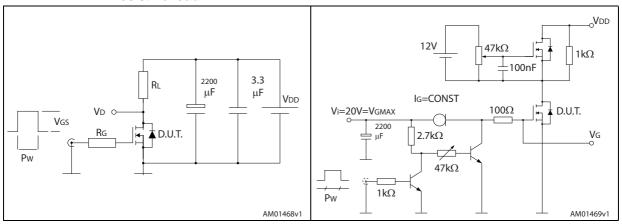


Figure 14. Test circuit for inductive load switching and diode recovery times

Figure 15. Unclamped Inductive load test circuit

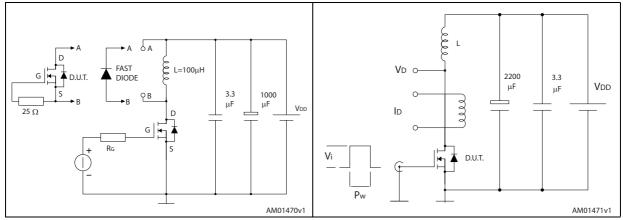
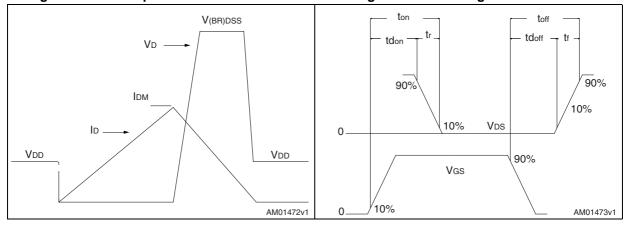


Figure 16. Unclamped inductive waveform

Figure 17. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.



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O016023_G_FU

Figure 18. SO-8 drawing



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Table 8. SO-8 mechanical data

mm Typ.	Max. 1.75 0.25
Тур.	1.75
	0.25
	0.25
	0.51
	0.48
	0.25
	0.23
4.90	5.00
6.00	6.20
3.90	4.00
1.27	
	0.50
	1.27
1.04	
0.25	
	8°
	0.10
	6.00 3.90 1.27



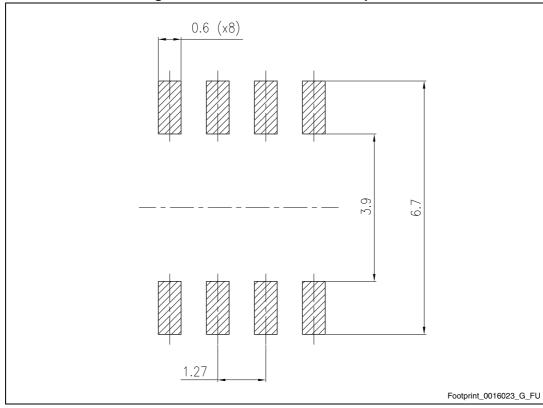


Figure 19. SO-8 recommended footprint^(a)

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a. All dimensions are in millimeters.

STS5DNF20V Revision history

5 Revision history

Table 9. Revision history

Date	Revision	Changes
21-Jun-2004	4	Complete document
13-Nov-2006	5	The document has been reformatted
02-May-2011	6	Table 1: Device summary has been corrected
06-Mar-2014	7	Modified: Marking in Table 1 Updated: Section 4: Package mechanical data, Figure 12: Switching times test circuit for resistive load, Figure 13: Gate charge test circuit, Figure 14: Test circuit for inductive load switching and diode recovery times and Figure 15: Unclamped Inductive load test circuit. Minor text changes.

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