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September 2015

FAN73611
Single-Channel High-Side Gate Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- 250 mA/500 mA Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise-Canceling Circuit
- 3.3 V and 5 V Input Logic Compatible
- Output In Phase with Input Signal
- Under-Voltage Lockout for V_{DD} and V_{BS}
- 8-Lead Small Outline Package (SOP)

The FAN73611 is a monolithic high-side gate drive IC that can drive MOSFETs and IGBTs operating up to +600 V. Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to V_S=-9.8 V (typical) for V_{BS}=15 V. The UVLO circuits prevents malfunction when V_{DD} or V_{BS} is lower than the specified threshold voltage. The output drivers typically source/sink 250 mA/500 mA; respectively, which is suitable for Plasma Display Panel (PDP) application, motor drive inverter, and switching mode power supply applications.

Applications

- Electronic Ballast
- Switching-Mode Power Supply (SMPS)

8-SOP

Related Application Notes

- *AN-6076 — Design and Applicaiton Guide of Boostrap Circuit for High-Voltage Gate-Drive IC*
- *AN-9052 — Design Guide for Selection of Bootstrap Components*
- *AN-8102 — Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications*

Description

Ordering Information

Part Number	Package	Operating Temperature	Packing Method	Description
FAN73611MX(1)	8 SOP	-40°C ~ 125°C	Tape & Reel	Lighting Application

Note:

1. This device passed wave soldering test by JESD22A-111.

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Typical Application Diagrams

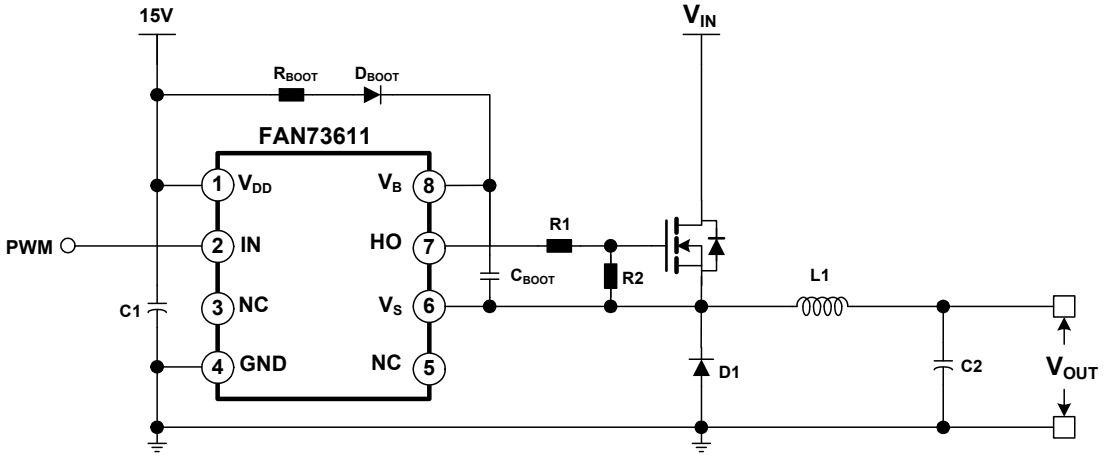

Figure 1. Step-Down (Buck) DC-DC Converter Application

Internal Block Diagram

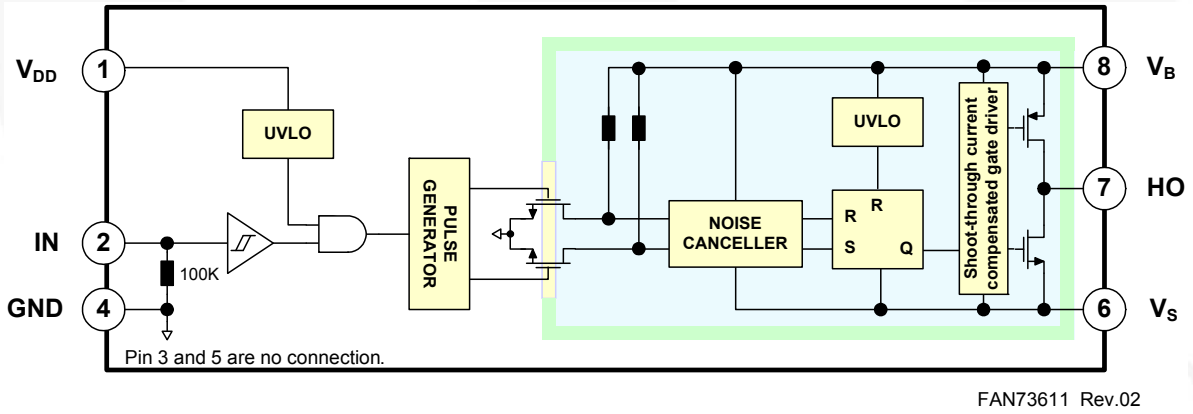

Figure 2. Functional Block Diagram

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Pin Configuration

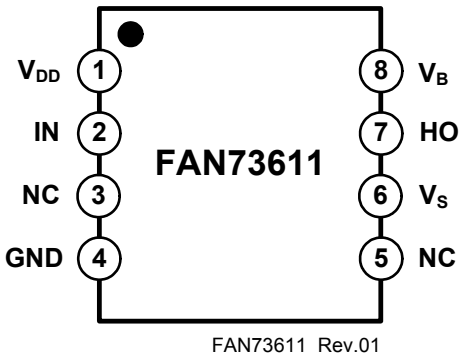

Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	V_{DD}	Supply Voltage
2	IN	Logic Input for High-Side Gate Driver Output
3	NC	No Connection
4	GND	Ground
5	NC	No Connection
6	V_S	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	V_B	High-Side Floating Supply

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V_S	High-Side Floating Offset Voltage	V_B-25	V_B+0.3	V
V_B	High-Side Floating Supply Voltage	-0.3	625.0	V
V_{HO}	High-Side Floating Output Voltage	V_S-0.3	V_B+0.3	V
V_{DD}	Low-Side and Logic Supply Voltage	-0.3	25.0	V
V_{IN}	Logic Input Voltage	-0.3	V_{DD}+0.3	V
dV_S/dt	Allowable Offset Voltage Slew Rate		± 50	V/ns
P_D	Power Dissipation[2, 3, 4]		0.625	W
θ_{JA}	Thermal Resistance		200	°C/W
T_J	Junction Temperature	-55	+150	°C
T_{STG}	Storage Temperature	-55	+150	°C

Notes:

2. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
3. *Refer to the following standards:*
   JESD51-2: Integrated circuits thermal test method environmental conditions, natural convection, and
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
4. Do not exceed power dissipation (P_D) under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	V_S+10	V_S+20	V
V_S	High-Side Floating Supply Offset Voltage	6-V_{DD}	600	V
V_{HO}	High-Side Output Voltage	V_S	V_B	V
V_{IN}	Logic Input Voltage	GND	V_{DD}	V
V_{DD}	Supply Voltage	10	20	V
T_A	Operating Ambient Temperature	-40	+125	°C

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Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})$ = 15.0 V and T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are relative to V_S and are applicable to the respective output HO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Power Supply Section						
I_{QDD}	Quiescent V_{DD} Supply Current	V_{IN}=0 V or 5 V, C_{LOAD}=1000 pF		80	140	µA
I_{PDD}	Operating V_{DD} Supply Current	C_{LOAD}=1000 pF, f_{IN}=20 KHz, RMS value		80	160	µA
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} Supply Under-Voltage Positive Going Threshold Voltage	V_{DD}=Sweep, V_{BS}=Sweep	7.8	8.8	9.8	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} Supply Under-Voltage Negative Going Threshold Voltage	V_{DD}=Sweep, V_{BS}=Sweep	7.3	8.3	9.3	V
V_{DDHYS} V_{BSHYS}	V_{DD} and V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage	V_{DD}=Sweep, V_{BS}=Sweep		0.5		V
I_{LK}	Offset Supply Leakage Current	V_B=V_S=600 V			10	µA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN}=0 V or 5 V, C_{LOAD}=1000 pF		60	100	µA
I_{PBS}	Operating V_{BS} Supply Current	C_{LOAD}=1000 pF, f_{IN}=20 KHz, RMS Value		420	600	µA
Input Logic Section						
V_{IH}	Logic “1” Input Voltage		2.5			V
V_{IL}	Logic “0” Input Voltage				0.8	V
I_{IN+}	Logic Input High Bias Current	V_{IN}=5 V		50	75	µA
I_{IN-}	Logic Input Low Bias Current	V_{IN}=0 V			2	µA
R_{IN}	Input Pull-Down Resistance		60	100		KΩ
Gate Driver Output Section						
V_{OH}	High Level Output Voltage (V_{BIAS} - V_O)	No Load			0.1	V
V_{OL}	Low Level Output Voltage	No Load			0.1	V
I_{O+}	Output High, Short-Circuit Pulsed Current	V_{HO}=0 V, V_{IN}=5 V, PW ≤10 µs	200	250		mA
I_{O-}	Output Low, Short-Circuit Pulsed Current	V_{HO}=15 V,V_{IN}=0 V, PW ≤10 µs	400	500		mA
V_S	Allowable Negative V_S Pin Voltage for IN Signal Propagation to HO	V_{BS}=15 V		-9.8	-7.0	V

Dynamic Electrical Characteristics

V_{DD}=V_{BS}=15 V, C_{LOAD}=1000 pF, and T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-On Propagation Delay Time	V_S=0 V	70	120	170	ns
t_{off}	Turn-Off Propagation Delay Time	V_S=0 V	70	120	170	ns
t_r	Turn-On Rise Time			70	140	ns
t_f	Turn-Off Fall Time			30	60	ns

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Typical Characteristics

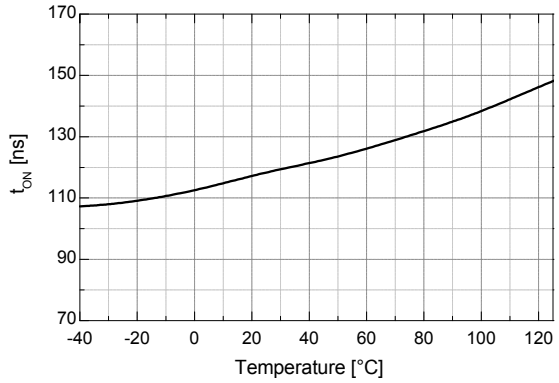

Figure 5. Turn-On Propagation Delay vs. Temperature

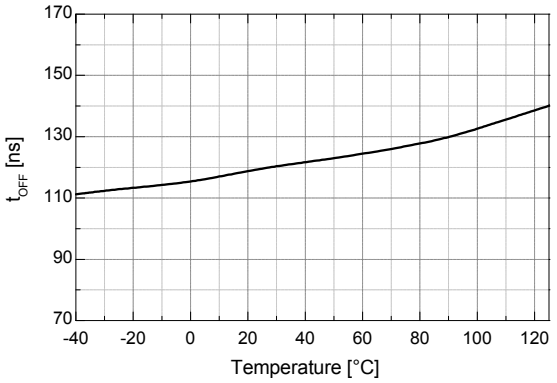

Figure 6. Turn-Off Propagation Delay vs. Temperature

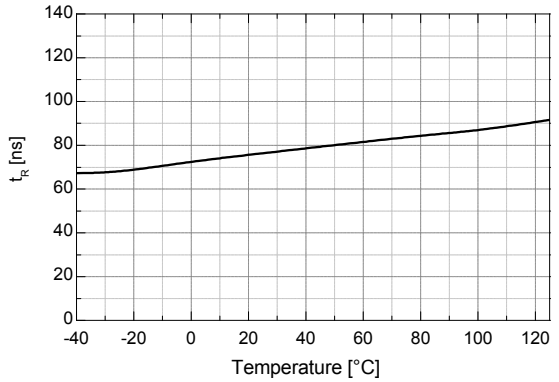

Figure 7. Turn-On Rise Time vs. Temperature

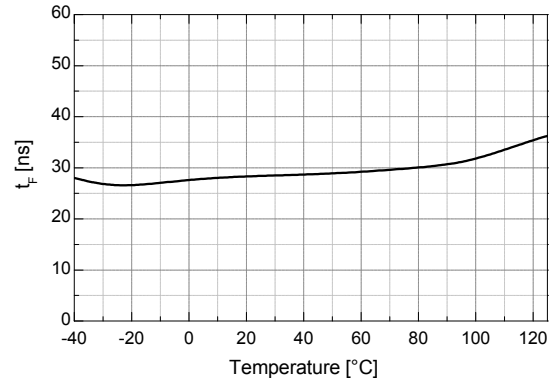

Figure 8. Turn-Off Fall Time vs. Temperature

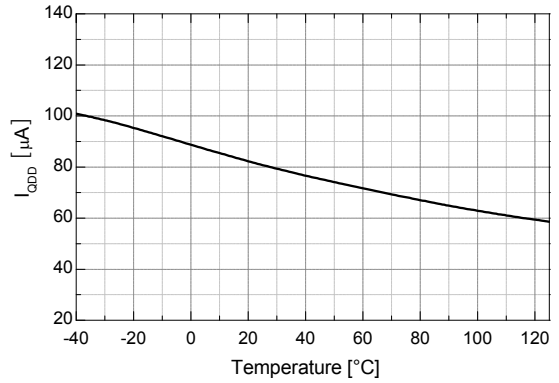

Figure 9. Quiescent V_{DD} Supply Current vs. Temperature

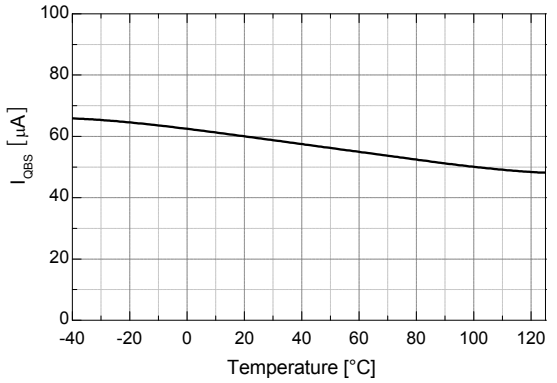

Figure 10. Quiescent V_{BS} Supply Current vs. Temperature

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Typical Characteristics (Continued)

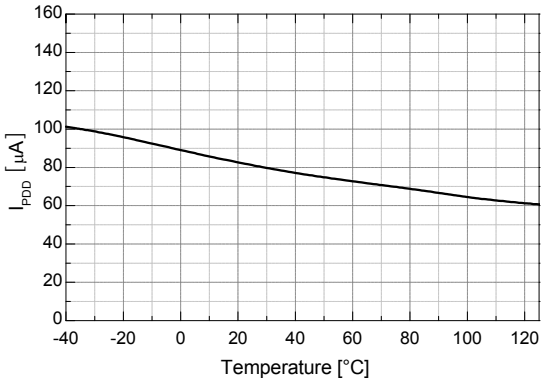

Figure 11. Operating V_{DD} Supply Current vs. Temperature

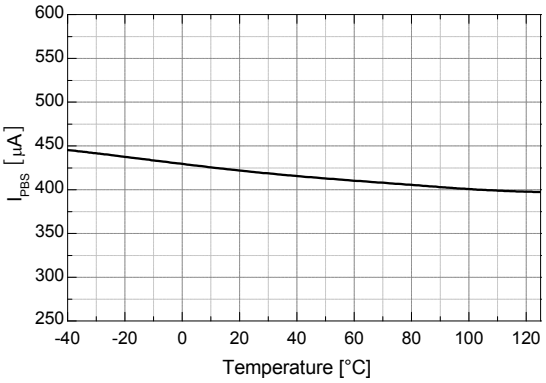

Figure 12. Operating V_{BS} Supply Current vs. Temperature

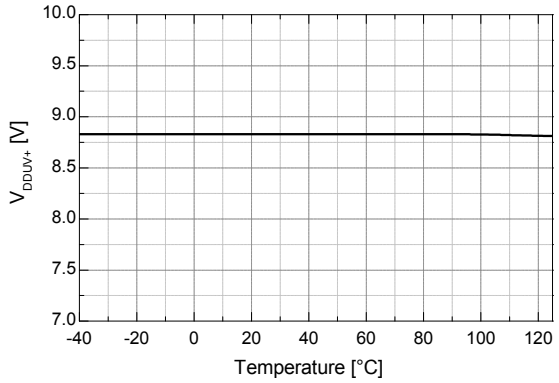

Figure 13. V_{DD} UVLO+ vs. Temperature

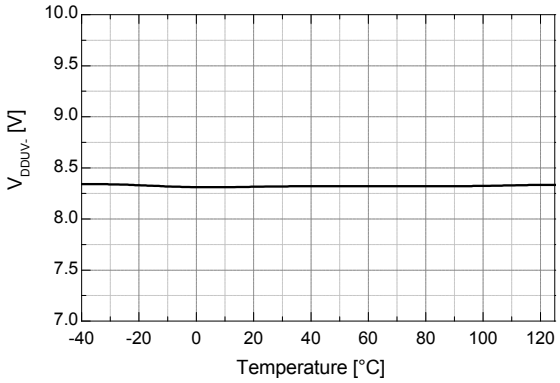

Figure 14. V_{DD} UVLO- vs. Temperature

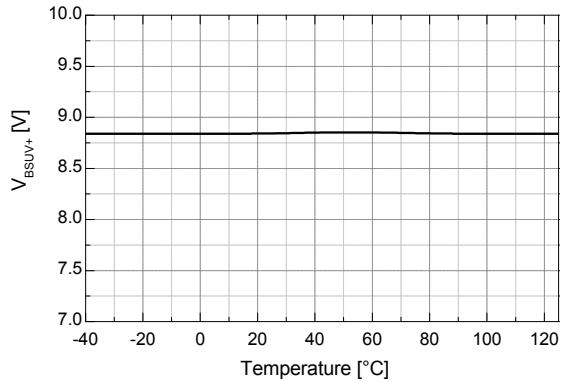

Figure 15. V_{BS} UVLO+ vs. Temperature

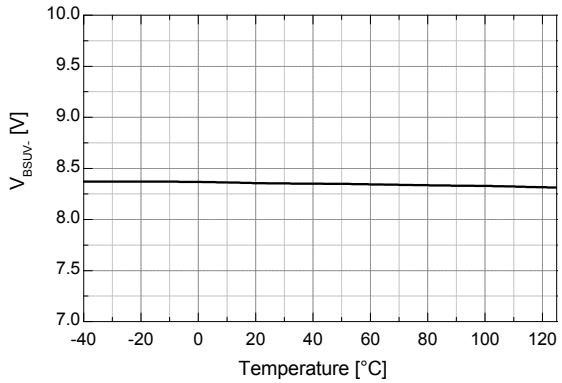

Figure 16. V_{BS} UVLO- vs. Temperature

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Typical Characteristics (Continued)

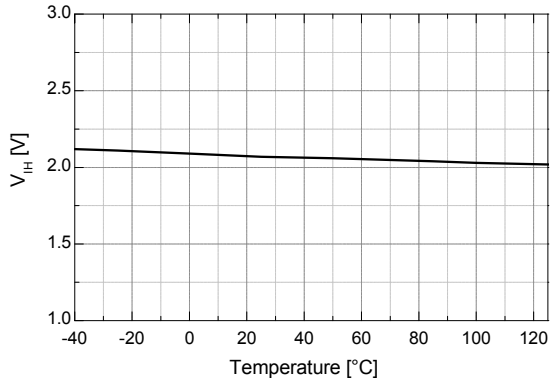

Figure 17. Logic HIGH Input Voltage vs. Temperature

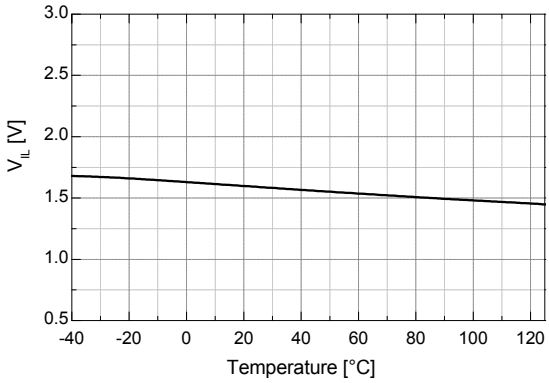

Figure 18. Logic LOW Input Voltage vs. Temperature

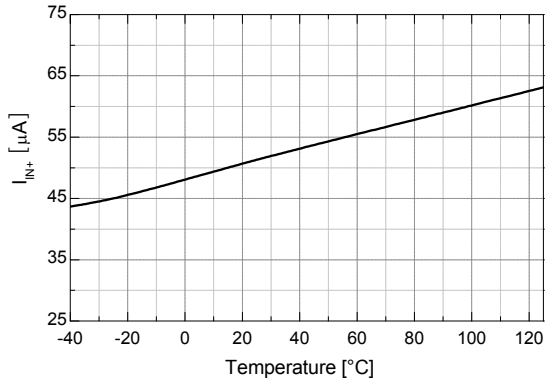

Figure 19. Logic HIGH Input Bias Current vs. Temperature

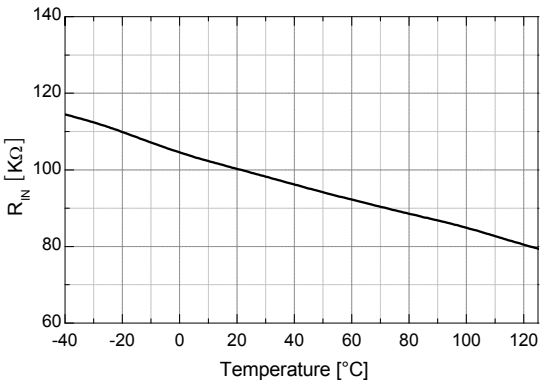

Figure 20. Input Pull-Down Resistance vs. Temperature

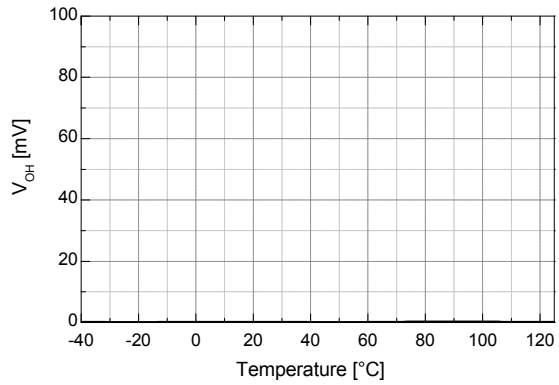

Figure 21. High-Level Output Voltage vs. Temperature

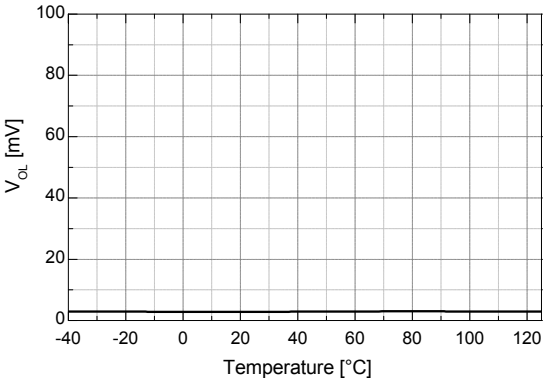

Figure 22. Low-Level Output Voltage vs. Temperature

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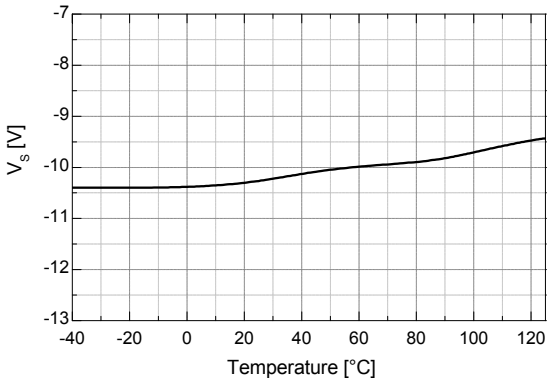

Figure 23. Allowable Negative V_S Voltage vs. Temperature

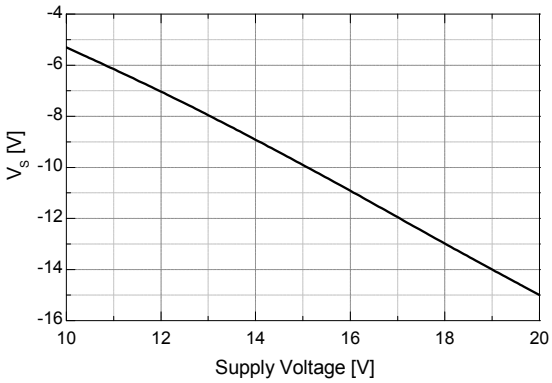

Figure 24. Allowable Negative V_S Voltage vs. Supply Voltage

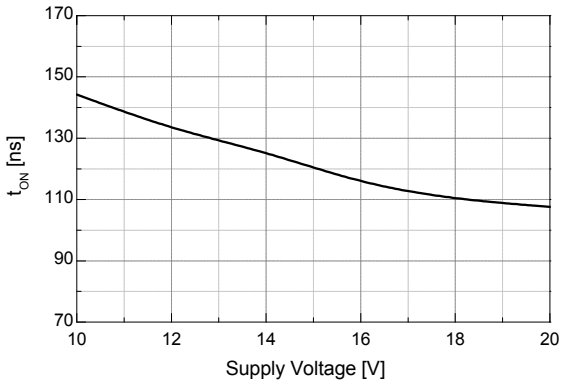

Figure 25. Turn-On Propagation Delay vs. Supply Voltage

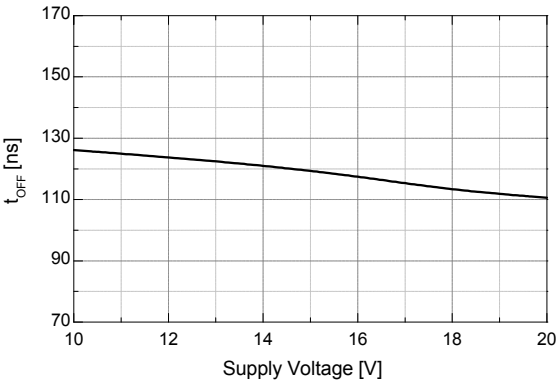

Figure 26. Turn-Off Propagation Delay vs. Supply Voltage

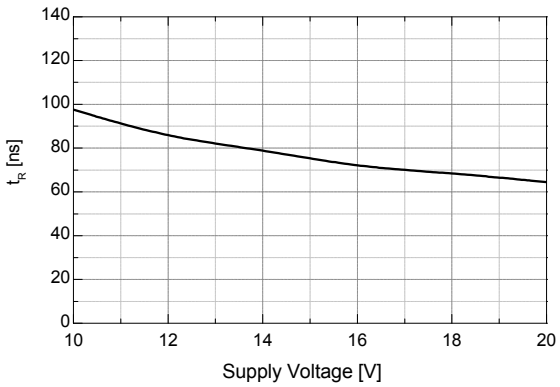

Figure 27. Turn-On Rise Time vs. Supply Voltage

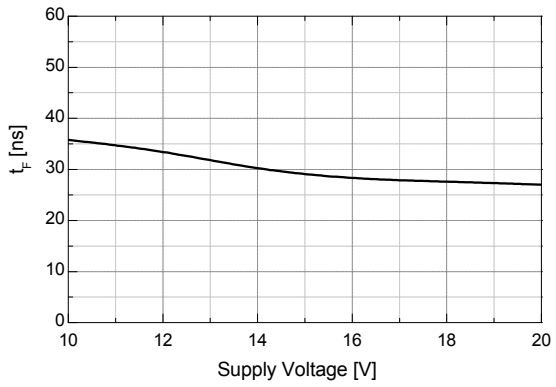

Figure 28. Turn-Off Fall Time vs. Supply Voltage

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Typical Characteristics (Continued)

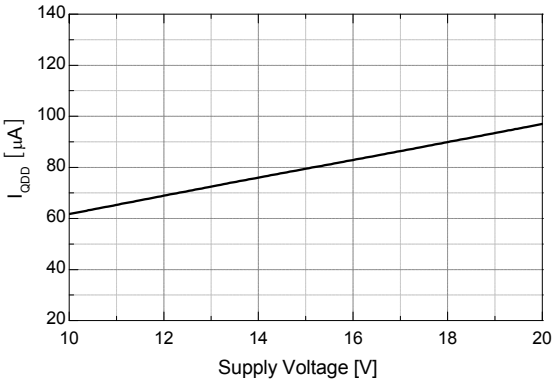

Figure 29. Quiescent V_{DD} Supply Current vs. Supply Voltage

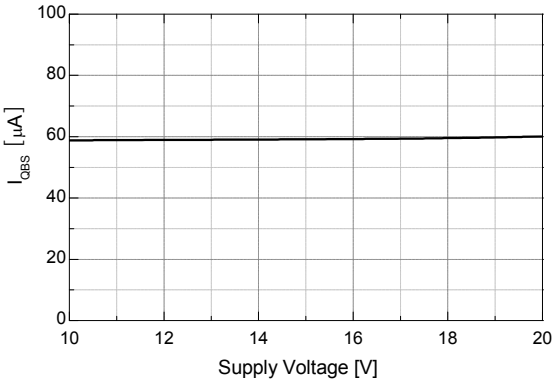

Figure 30. Quiescent V_{BS} Supply Current vs. Supply Voltage

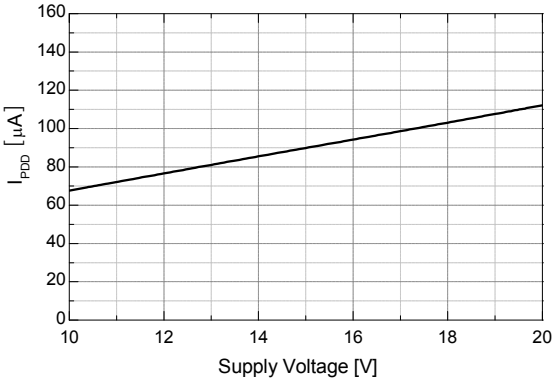

Figure 31. Operating V_{DD} Supply Current vs. Supply Voltage

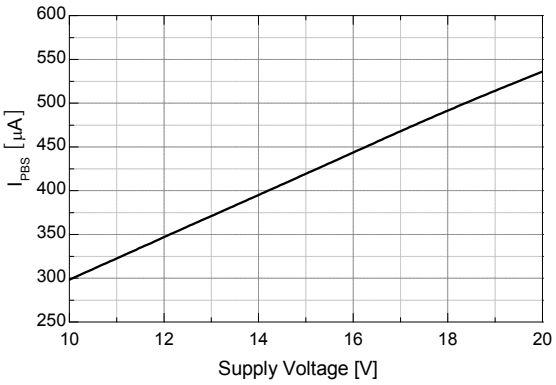

Figure 32. Operating V_{BS} Supply Current vs. Supply Voltage

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Switching Time Definitions

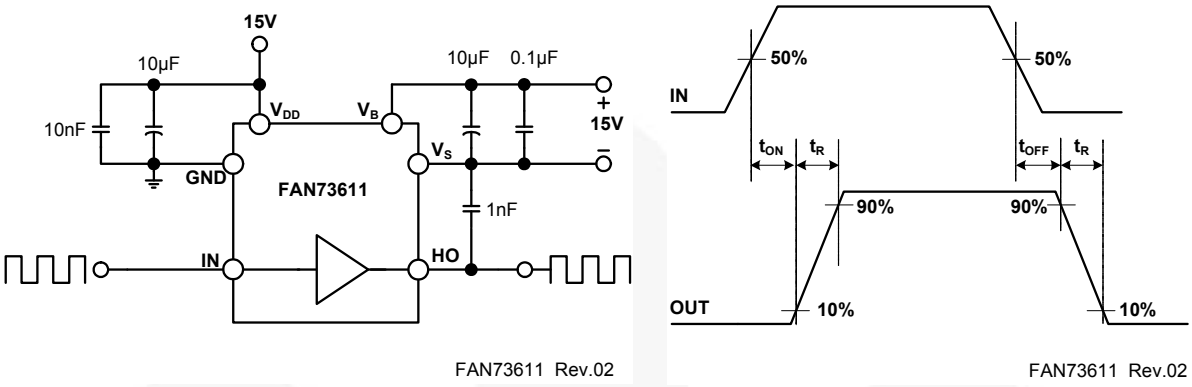

Figure 33. Switching Time Test Circuit and Waveform Definitions

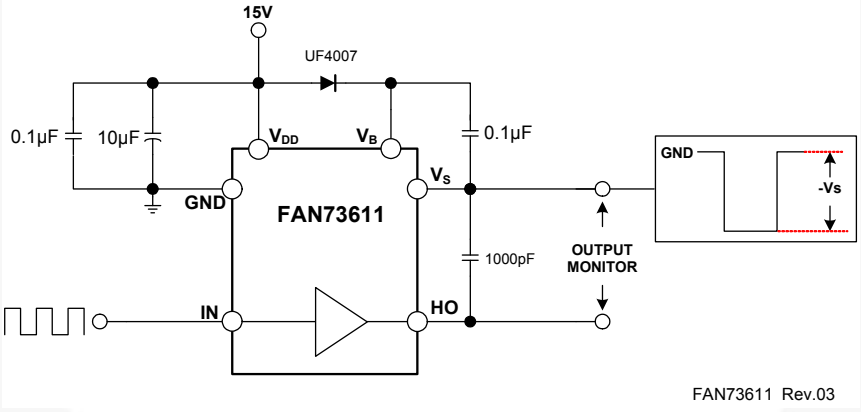

Figure 34. Floating Supply Voltage Transient Test

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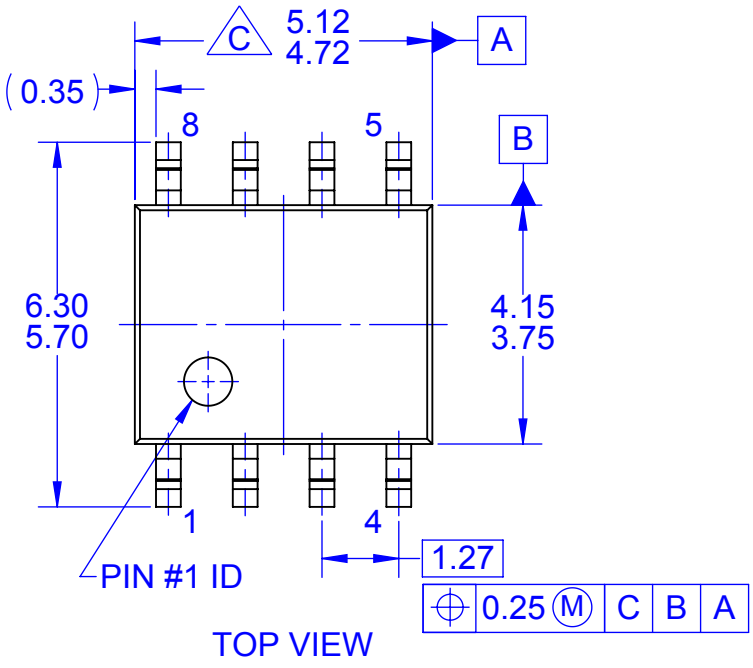
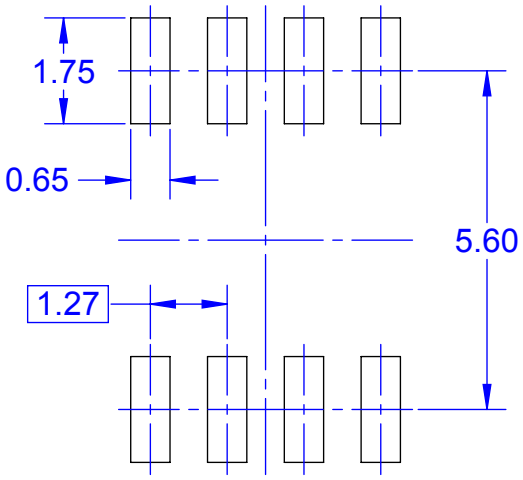
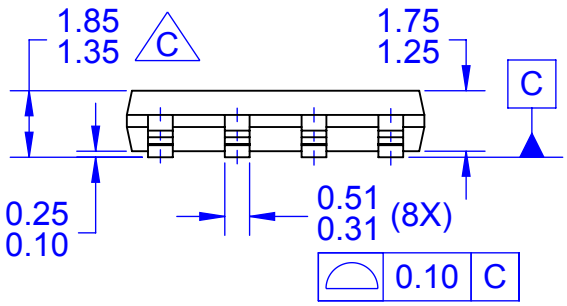


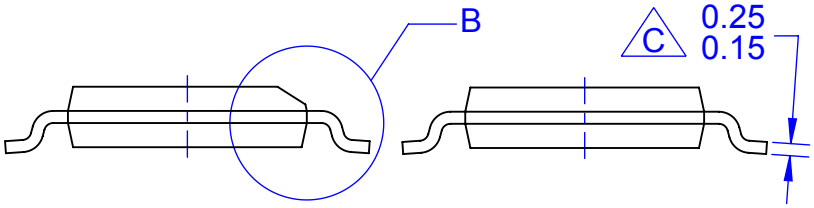
TOP VIEW



LAND PATTERN RECOMMENDATION



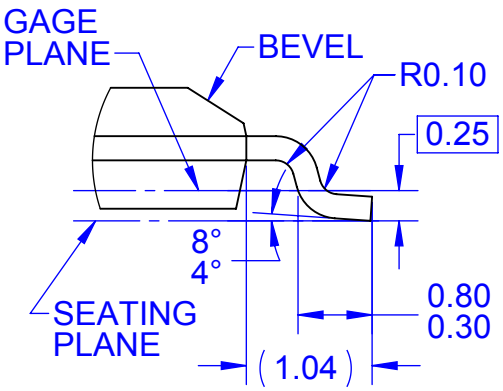
FRONT VIEW



OPTION A
BEVEL EDGE

OPTION B
NON-BEVEL EDGE

SIDE VIEW



DETAIL "B"
SCALE 2:1

NOTES: UNLESS OTHERWISED SPECIFIED

A. THIS PACKAGE CONFORMS TO JEDEC MS-012 VARIATION A EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS
C OUT OF JEDEC STANDARD VALUE
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
E. LAND PATTERN AS PER IPC SOIC127P600X175-8M
F. DRAWING FILENAME: MKT-M08Brev2

FAIRCHILD ™

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