

STP2NK90Z - STD2NK90Z STD2NK90Z-1

N-channel 900V - 5Ω - 2.1A - TO-220 /DPAK/IPAK Zener-Protected SuperMESH™ MOSFET

General features

Туре	V _{DSS} (@Tjmax)	R _{DS(on)}	I _D	P _W
STD2NK90Z	900V	<6.5Ω	2.1A	70W
STD2NK90Z-1	900V	<6.5Ω	2.1A	70W
STP2NK90Z	900V	<6.5Ω	2.1A	70W

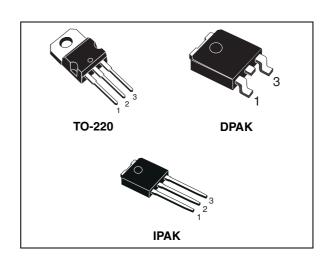
- Extremely high dv/dt capability
- Improved esd capability
- 100% avalanche rated
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatibility



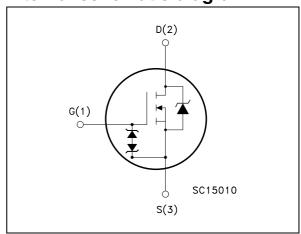
The SuperMESH™ series is obtained through an extreme optimization of ST's well established stripbased PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Applications

Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD2NK90ZT4	D2NK90Z	DPAK	Tape & reel
STD2NK90Z-1	D2NK90Z	IPAK	Tube
STP2NK90Z	P2NK90Z	TO-220	Tube

July 2006 Rev 4 1/18

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Val	Unit			
		STP2NK90Z	STD2NK90Z STD2NK90Z-1			
V_{DS}	Drain-source voltage (V _{GS} = 0)	90	0	٧		
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	90	0	٧		
V_{GS}	Gate- source Voltage	± 30		V		
I _D	Drain current (continuous) at T _C = 25°C	2.1		Α		
I _D	Drain current (continuous) at T _C = 100°C	1.3		Α		
I _{DM} ⁽¹⁾	Drain current (pulsed)	8.	4	Α		
P _{TOT}	Total dissipation at T _C = 25°C	70)	W		
	Derating factor	0.5	66	W/°C		
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000		V		
dv/dt (2)	Peak diode recovery voltage slope	4.5		V/ns		
Tj	Operating junction temperature	-55 to 150		-55 to 150		°C
T _{stg}	Storage temperature	-55 to	150	°C		

^{1.} Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	1.78	°C/W
Rthj-amb T _l	Thermal resistance junction-ambient max Maximum lead temperature for soldering purpose	62.5 300	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.1	Α
E _{AS}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	150	mJ

 $^{2. \}quad I_{SD} \leq \hspace{-0.1cm} 2.1A, \ di/dt \leq \hspace{-0.1cm} 200A/\mu s, \ V_{DD} \leq \hspace{-0.1cm} V_{(BR)DSS}, \ T_j \leq \hspace{-0.1cm} T_{JMAX}.$

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
BV _{GSO}	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30			V

1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test condictions		Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown Voltage	I _D = 1 mA, V _{GS} = 0	900			V
I _{DSS}	Zero gate voltage Drain current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_{C} = 125°C			1 50	μ Α μ Α
I _{GSS}	Gate-body Leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			± 10	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50 \mu A$	3	3.75	4.5	٧
R _{DS(on}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 1.05 A		5	6.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test condictions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15 V , I _D = 1.05 A		2.3		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V, f} = 1 \text{ MHz,}$ $V_{GS} = 0$		485 50 10		pF pF pF
Coss eq ⁽²⁾ .	Equivalent output capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ to } 720 \text{ V}$		24		pF
$egin{array}{c} Q_{ m g} \ Q_{ m gd} \end{array}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 720 \text{ V}, I_{D} = 2 \text{ A},$ $V_{GS} = 10 \text{ V}$ (see Figure 22)		19.5 3.4 10.8	27	nC nC nC

^{1.} Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test condictions	Min.	Тур.	Max.	Unit
$t_{ m d(on)}$ $t_{ m r}$ $t_{ m d(off)}$ $t_{ m f}$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 450 \text{ V}, I_{D} = 1 \text{ A},$ $R_{G} = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 19)		21 11 43 40		ns ns ns ns

^{2.} $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Table 8. Source drain diode

Symbol	Parameter	Test condictions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				2.1	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				8.4	Α
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 2.1 \text{ A}, V_{GS} = 0$			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 2$ A, di/dt = 100 A/ μ s $V_{DD} = 50$ V (see Figure 20)		415 1.5 7.2		ns μC A
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 2 \text{ A, di/dt} = 100 \text{ A/µs}$ $V_{DD} = 50\text{V, T}_{j} = 150^{\circ}\text{C}$ (see Figure 20)		515 1.9 7.5		ns μC A

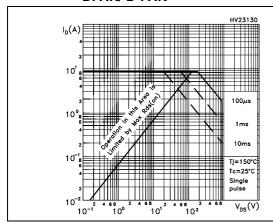
^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/ DPAK/ D²PAK

Figure 2. Thermal impedance for TO-220/ DPAK/ D²PAK



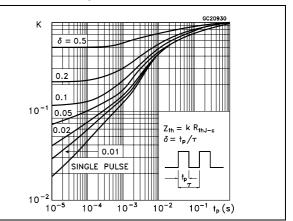
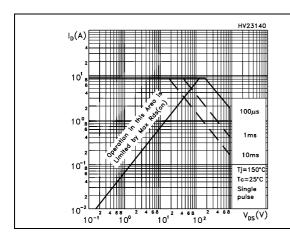


Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP



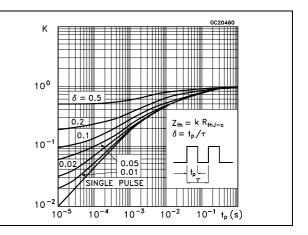
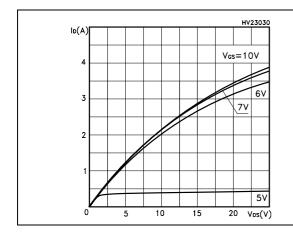


Figure 5. Output characterisics

Figure 6. Transfer characteristics



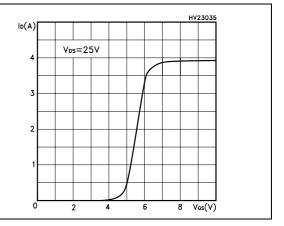


Figure 7. Transconductance

Figure 8. Static drain-source on resistance

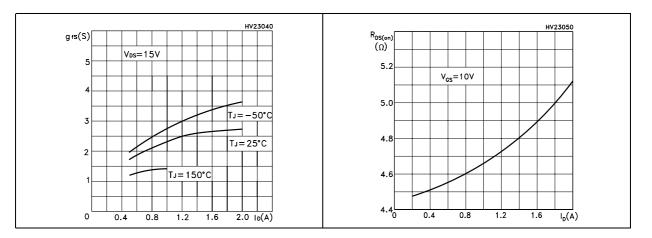


Figure 9. Gate charge vs gate-source voltage Figure 10. Capacitance variations

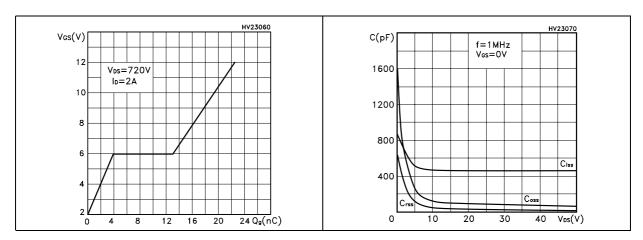


Figure 11. Normalized gate threshold voltage Figure 12. Normalized on resistance vs vs temperature temperature

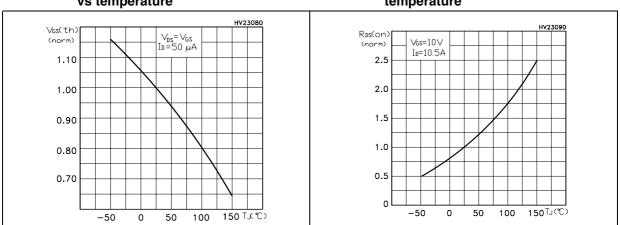
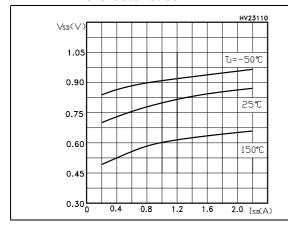


Figure 13. Source-drain diode forward characteristics

Figure 14. Normalized B_{VDSS} vs temperature



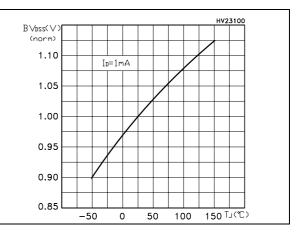
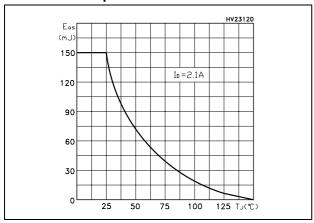


Figure 15. Maximum avalanche energy vs temperature



 V_{DD}

SC05980

3 Test circuit

Figure 16. Switching times test circuit for resistive load

Figure 17. Gate charge test circuit

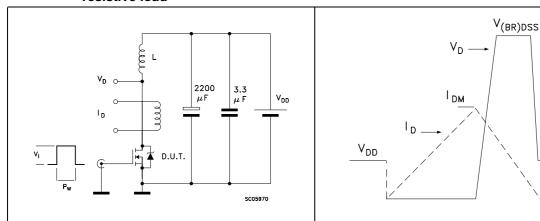


Figure 18. Test circuit for inductive load switching and diode recovery times

Figure 19. Unclamped Inductive load test circuit

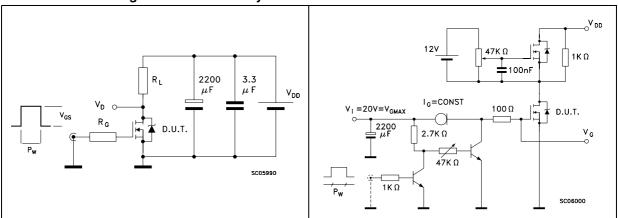
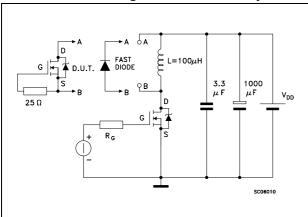


Figure 20. Test circuit for inductive load switching and diode recovery times



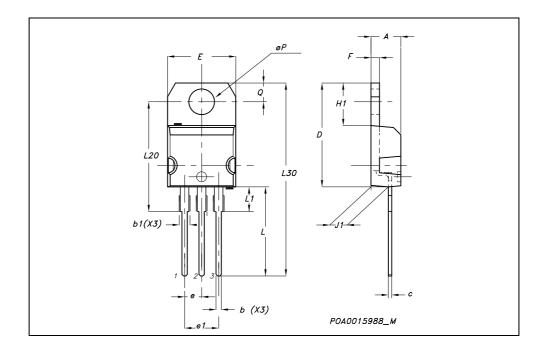
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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

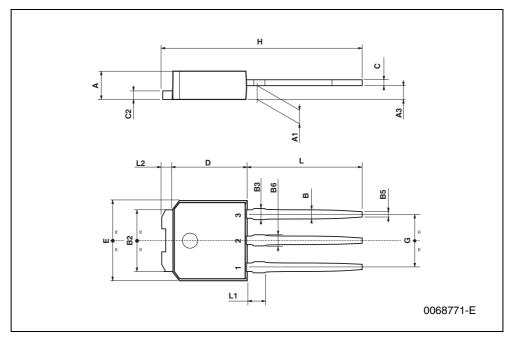
TO-220 MECHANICAL DATA

DIM.		mm.			inch		
DINI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
Α	4.40		4.60	0.173		0.181	
b	0.61		0.88	0.024		0.034	
b1	1.15		1.70	0.045		0.066	
С	0.49		0.70	0.019		0.027	
D	15.25		15.75	0.60		0.620	
E	10		10.40	0.393		0.409	
е	2.40		2.70	0.094		0.106	
e1	4.95		5.15	0.194		0.202	
F	1.23		1.32	0.048		0.052	
H1	6.20		6.60	0.244		0.256	
J1	2.40		2.72	0.094		0.107	
L	13		14	0.511		0.551	
L1	3.50		3.93	0.137		0.154	
L20		16.40			0.645		
L30		28.90			1.137		
øΡ	3.75		3.85	0.147		0.151	
Q	2.65		2.95	0.104		0.116	



TO-251 (IPAK) MECHANICAL DATA

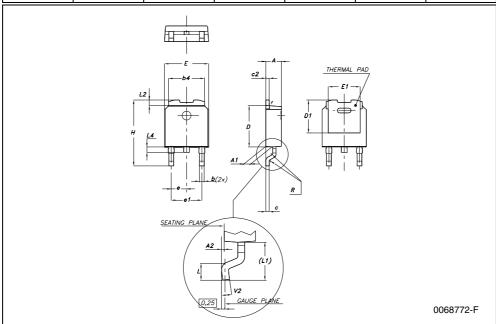
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
А3	0.7		1.3	0.027		0.051
В	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
В3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
Е	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
Н	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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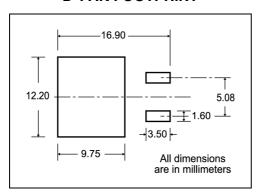
DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
В	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
е		2.28			0.090	
e1	4.4		4.6	0.173		0.181
Н	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

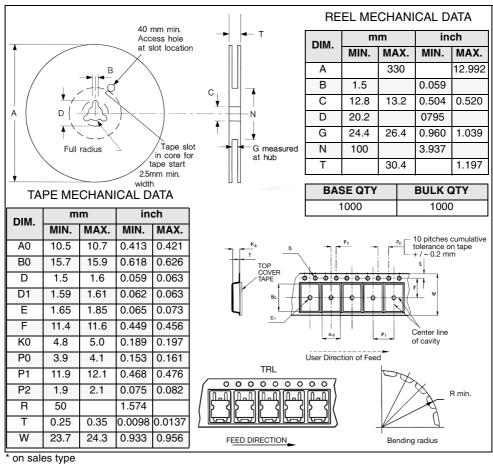


Packing mechanical data 5

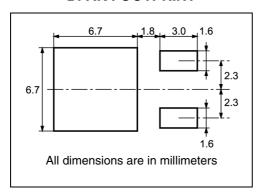
D²PAK FOOTPRINT



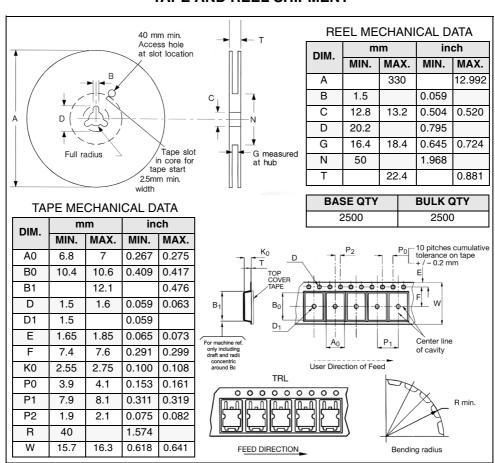
TAPE AND REEL SHIPMENT



DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 9. Revision history

Date	Revision	Changes
06-Oct-2004	1	First version
08-Sep-2005	2	Complete version
05-Mar-2006	3	Inserted Ecopack indication
27-Jul-2006	4	New template, no content change

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