

Automotive-grade N-channel 600 V, 0.097  $\Omega$  typ., 29 A FDmesh™ II Power MOSFETs (with fast diode) in D<sup>2</sup>PAK and TO-247 packages

Datasheet - production data

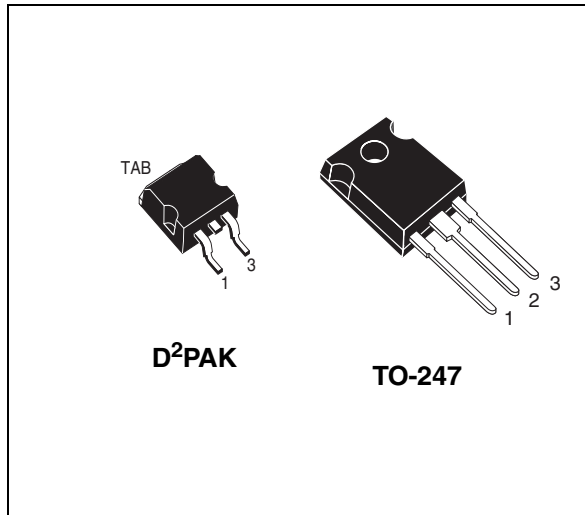
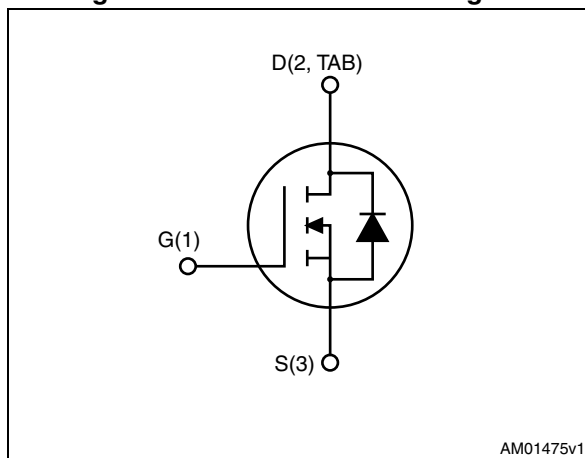


Figure 1. Internal schematic diagram



## Features

Order codes	V <sub>DSS</sub> @T <sub>J</sub> max.	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB36NM60ND	650 V	0.110 $\Omega$	29 A
STW36NM60ND			

- Designed for automotive applications and AEC-Q101 qualified
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities

## Applications

- Automotive switching applications

## Description

These FDmesh™ II Power MOSFETs with intrinsic fast-recovery body diode are produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, these revolutionary devices feature extremely low on-resistance and superior switching performance. They are ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB36NM60ND	36NM60ND	D <sup>2</sup> PAK	Tape and reel
STW36NM60ND	36NM60ND	TO-247	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate- source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	29	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	18	A
$I_{DM}^{(1)}$	Drain current (pulsed)	116	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	°C
$T_J$	Max. operating junction temperature	150	

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 29\text{ A}$ ,  $di/dt \leq 600\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ ,  $V_{DSPeak} < V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK	TO-247	
$R_{thj-case}$	Thermal resistance junction-case max	0.66		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		50	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	30		°C/W

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu.

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	110	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 600 V V <sub>DS</sub> = 600 V, T <sub>C</sub> = 125 °C			1 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 25 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14.5 A		0.097	0.110	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	2785	-	pF
C <sub>oss</sub>	Output capacitance		-	168	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	5	-	pF
C <sub>oss eq. (1)</sub>	Equivalent output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 480 V	-	438	-	pF
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 14.5 A R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 16</a> and <a href="#">21</a> )	-	30	-	ns
t <sub>r</sub>	Rise time		-	53.4	-	ns
t <sub>d(off)</sub>	Turn-off delay time		-	111	-	ns
t <sub>f</sub>	Fall time		-	61.8	-	ns
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 29 A, V <sub>GS</sub> = 10 V, (see <a href="#">Figure 17</a> )	-	80.4	-	nC
Q <sub>gs</sub>	Gate-source charge		-	16	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	41.4	-	nC
R <sub>g</sub>	Gate input resistance	f = 1 MHz, open drain	-	2.87	-	Ω

1. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		29	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		116	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 29\text{ A}, V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 29\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ (see <a href="#">Figure 18</a> )	-	175		ns
$Q_{rr}$	Reverse recovery charge		-	1.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	16		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 29\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 18</a> )	-	255		ns
$Q_{rr}$	Reverse recovery charge		-	2.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK

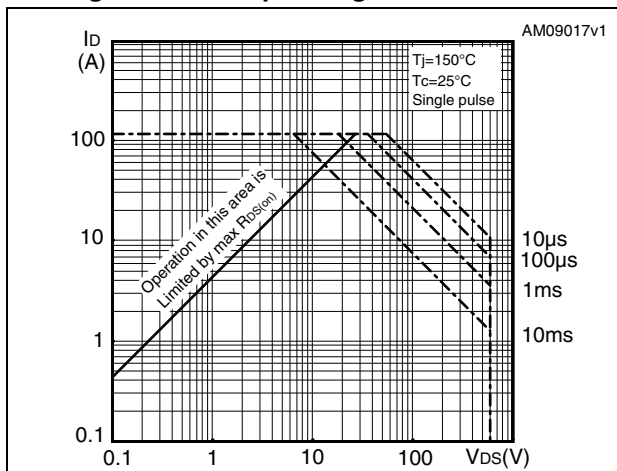


Figure 3. Thermal impedance for D<sup>2</sup>PAK

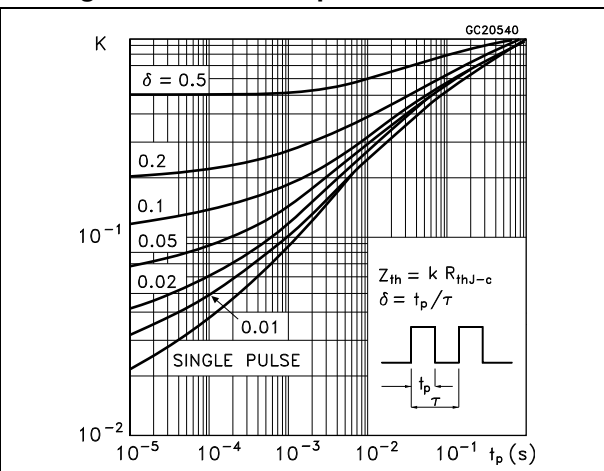


Figure 4. Safe operating area for TO-247

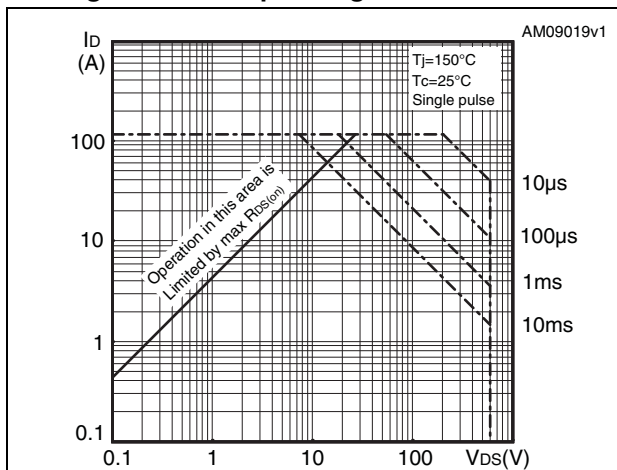


Figure 5. Thermal impedance for TO-247

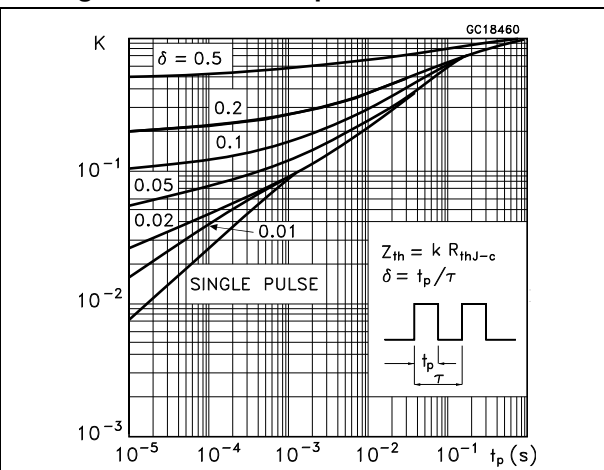


Figure 6. Output characteristics

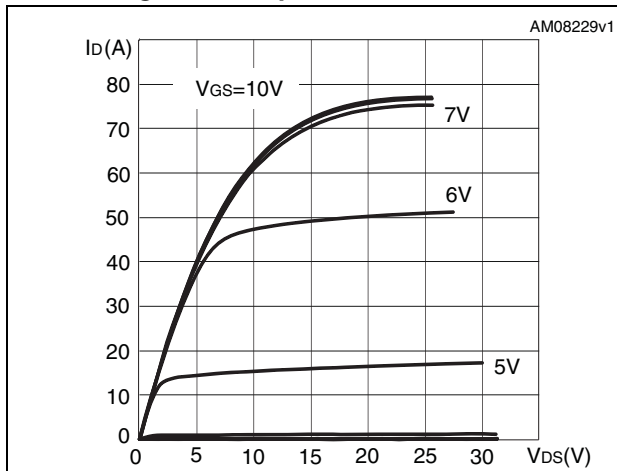


Figure 7. Transfer characteristics

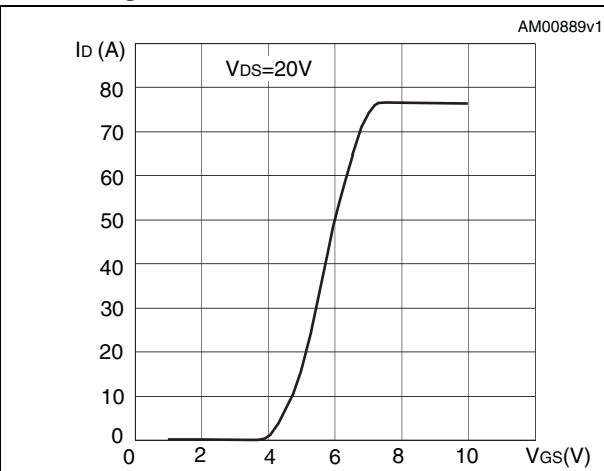


Figure 8. Gate charge vs gate-source voltage

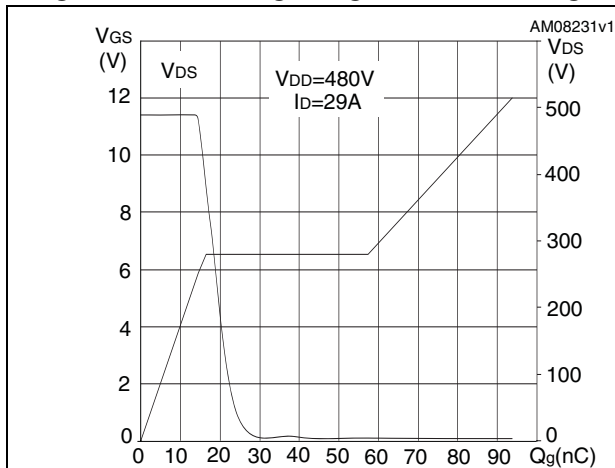


Figure 9. Static drain-source on-resistance

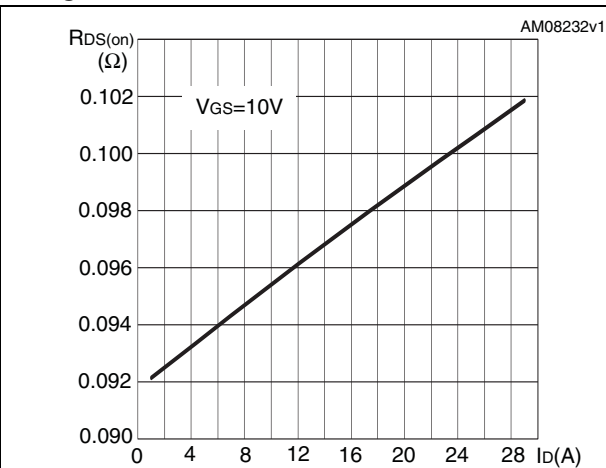


Figure 10. Capacitance variations

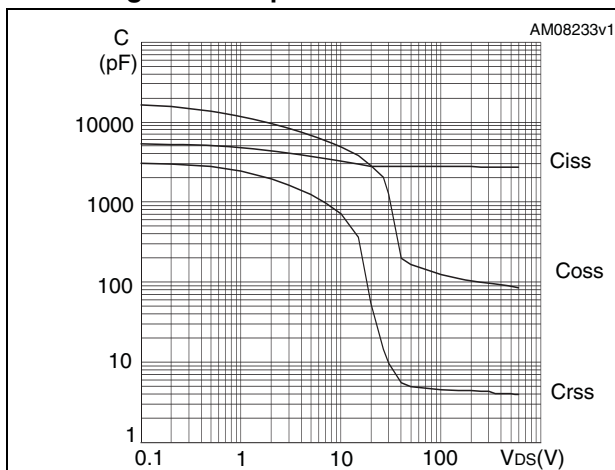


Figure 11. Output capacitance stored energy

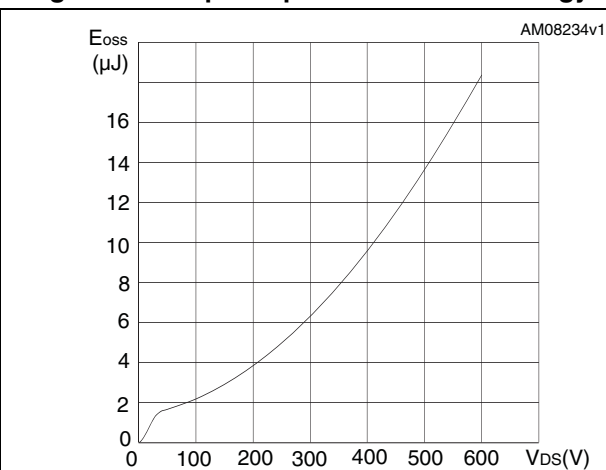


Figure 12. Normalized gate threshold voltage vs temperature

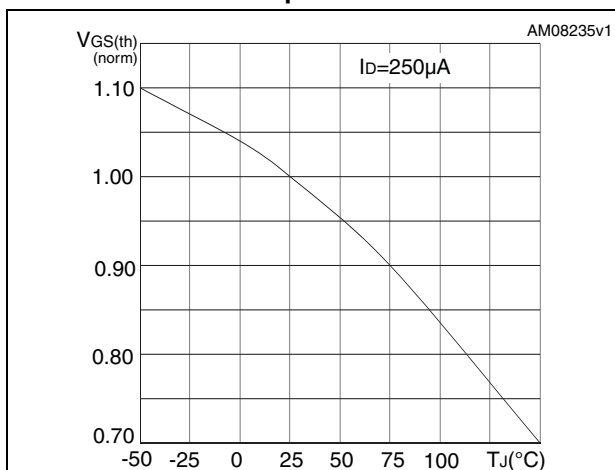


Figure 13. Normalized on-resistance vs temperature

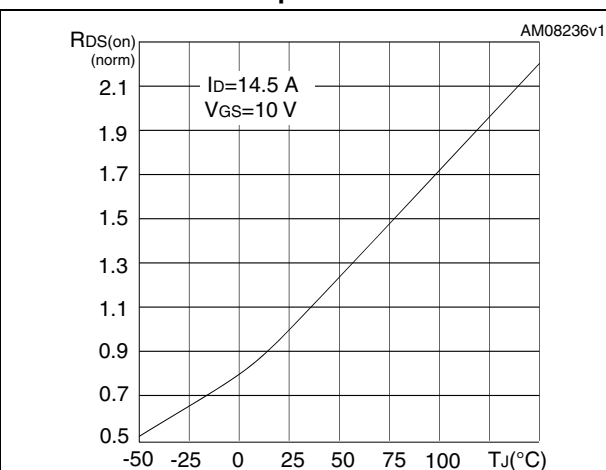


Figure 14. Normalized  $V_{DS}$  vs temperature

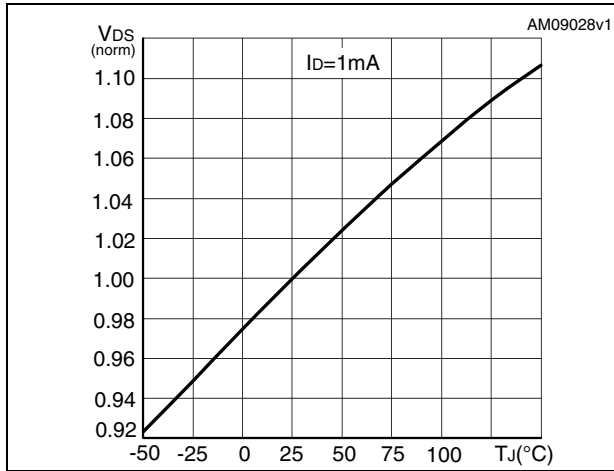
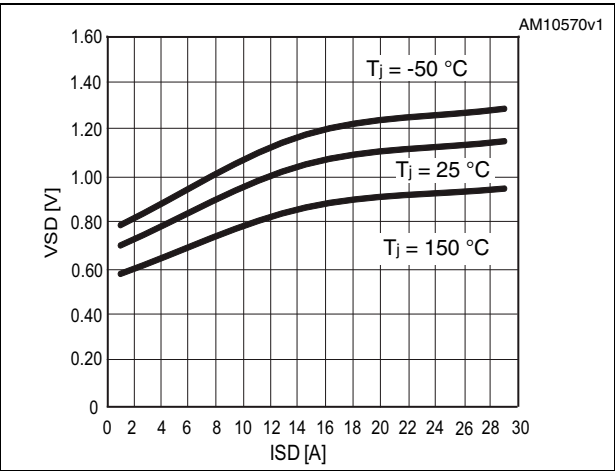


Figure 15. Source-drain diode forward vs temperature





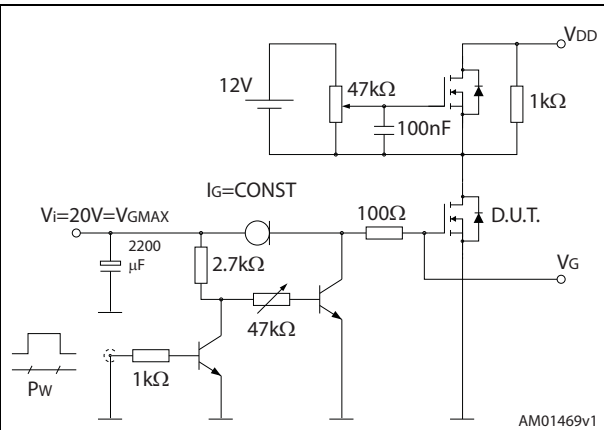
### 3 Test circuits

Figure 16. Switching times test circuit for resistive load



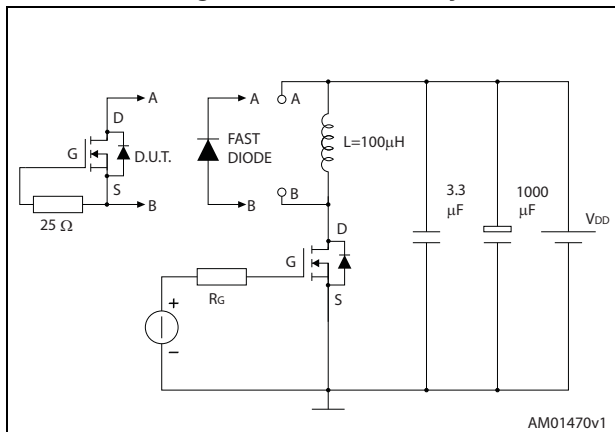
AM01468v1

Figure 17. Gate charge test circuit



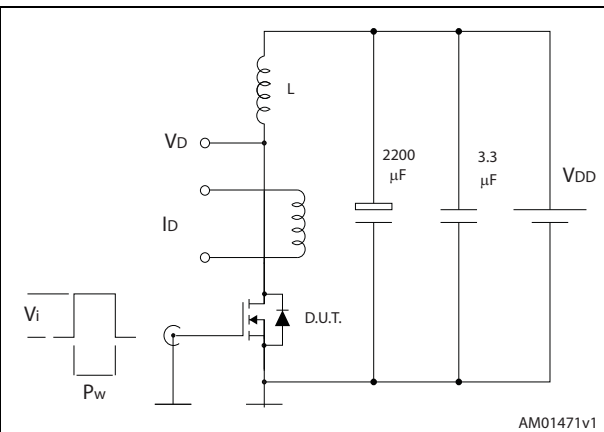
AM01469v1

Figure 18. Test circuit for inductive load switching and diode recovery times



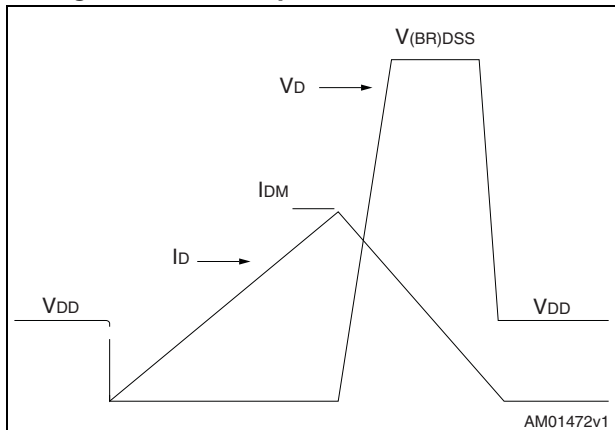
AM01470v1

Figure 19. Unclamped inductive load test circuit



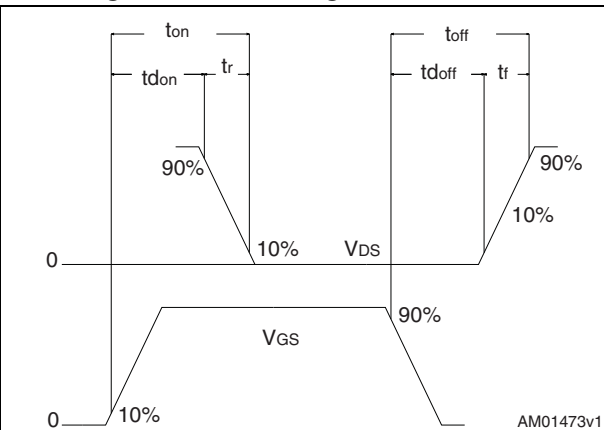
AM01471v1

Figure 20. Unclamped inductive waveform



AM01472v1

Figure 21. Switching time waveform



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 22. D<sup>2</sup>PAK (TO-263) drawing

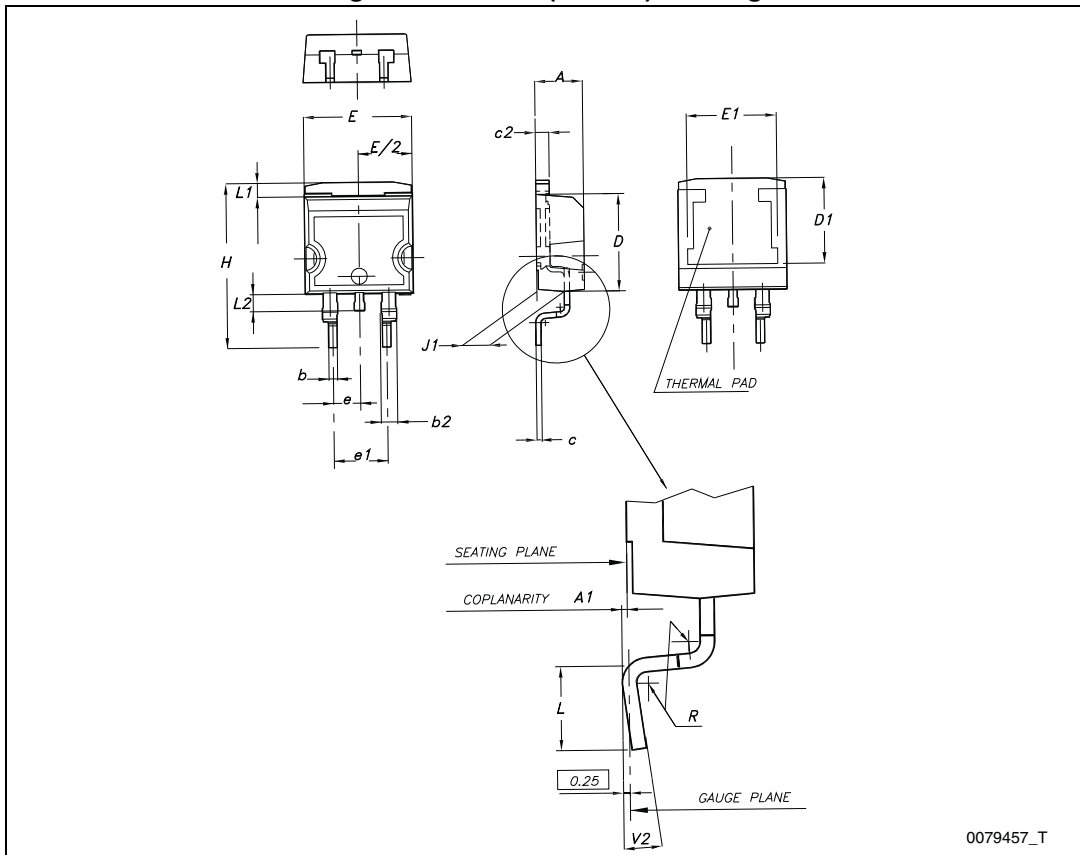
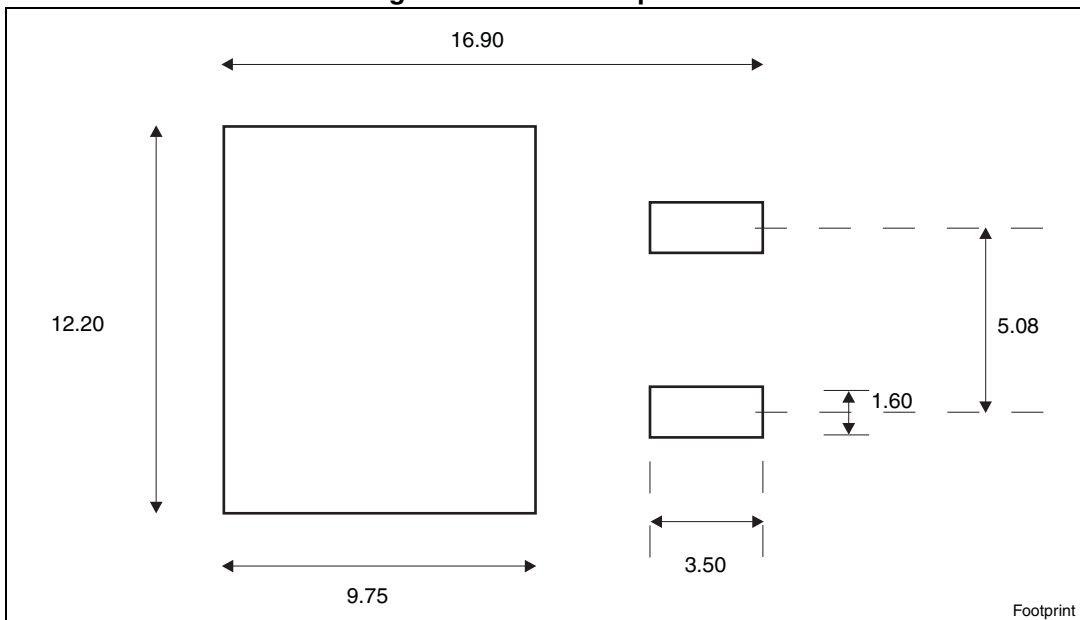


Figure 23. D<sup>2</sup>PAK footprint<sup>(a)</sup>

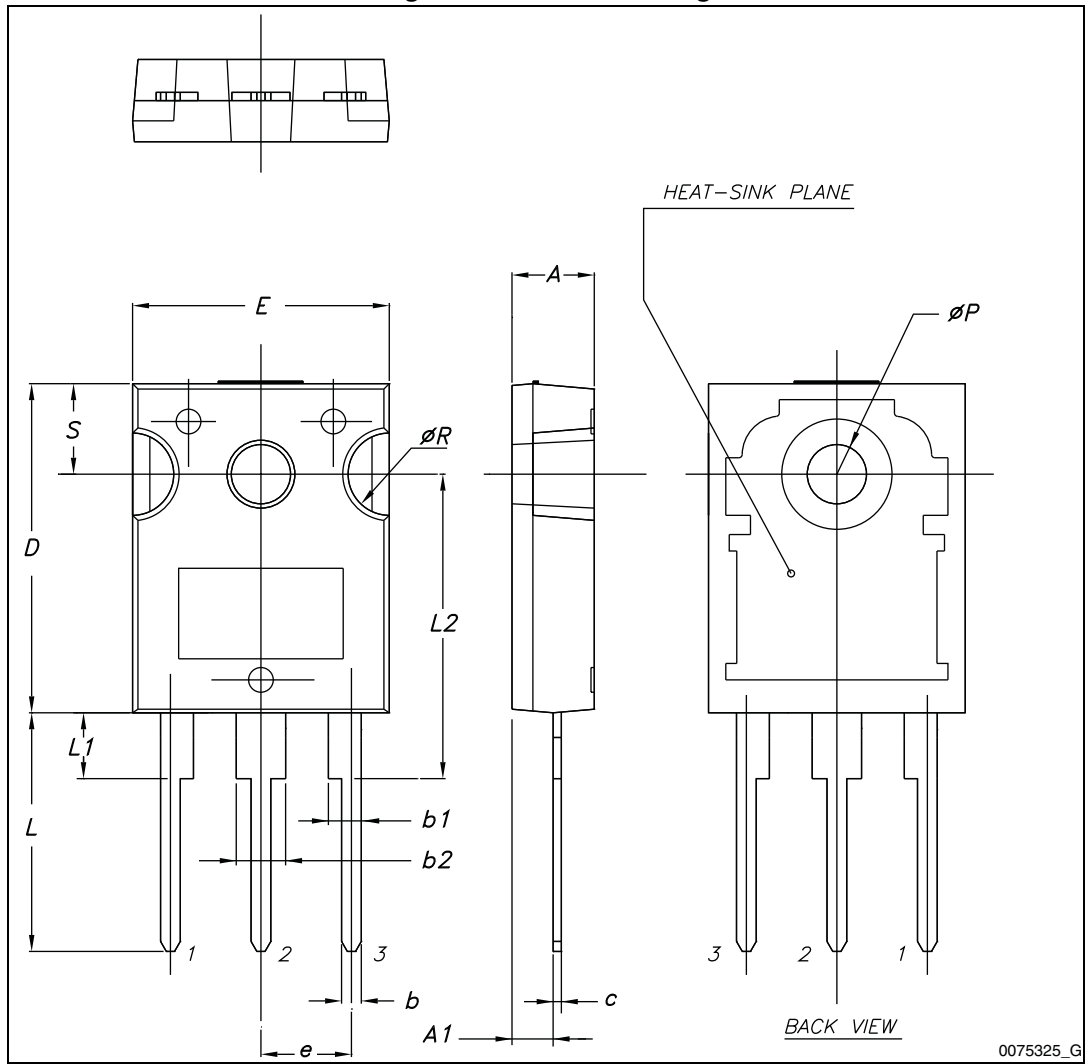


a. All dimensions are in millimeters

Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 24. TO-247 drawing



## 5 Packaging mechanical data

Table 10. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 25. Tape

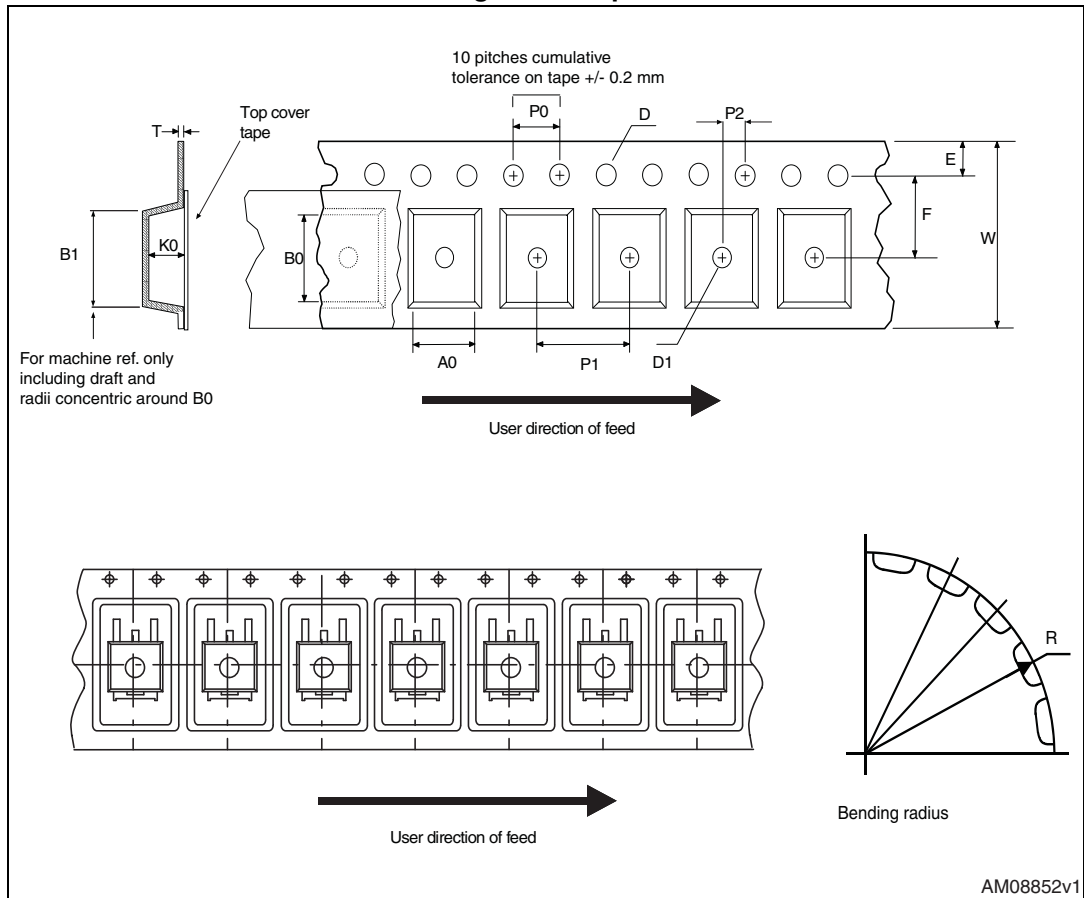
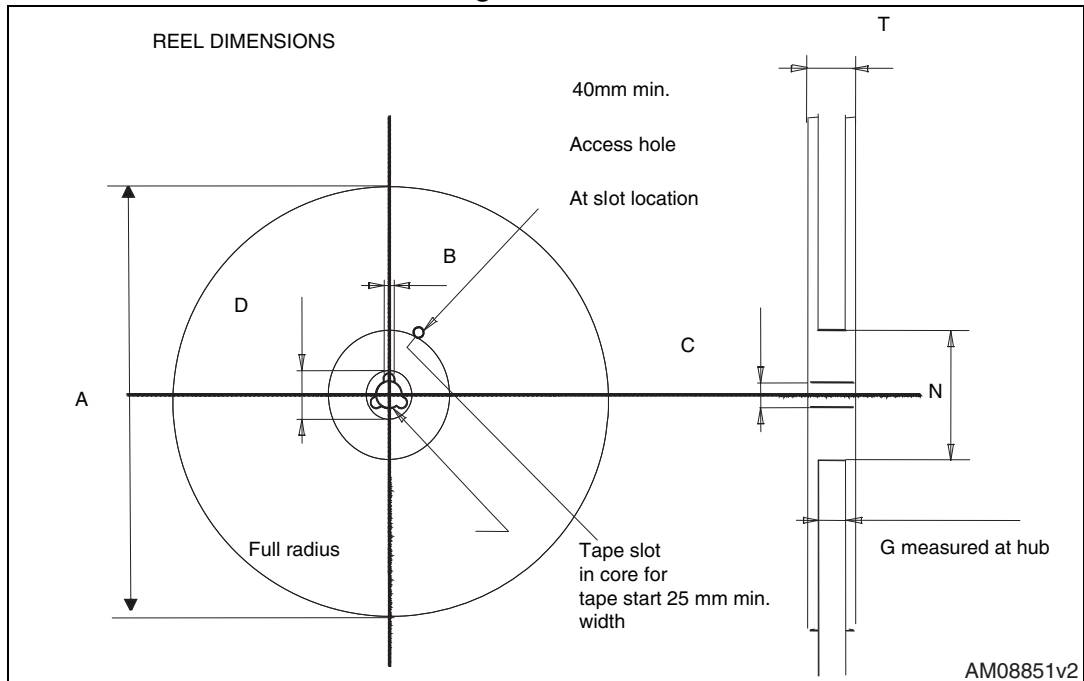


Figure 26. Reel





## 6 Revision history

Table 11. Document revision history

Date	Revision	Changes
24-Oct-2012	1	Initial release.
01-Jul-2013	2	– Updated <a href="#">Figure 1: Internal schematic diagram</a> . – Added <a href="#">Section 2.1: Electrical characteristics (curves)</a> .
02-Oct-2013	3	– Modified: $E_{AS}$ in <a href="#">Table 4</a> , $C_{oss\ eq.}$ typical value in <a href="#">Table 6</a> , <a href="#">Figure 13</a> – Minor text changes

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