

N-channel 120 V, 6.3 mΩ typ., 100 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

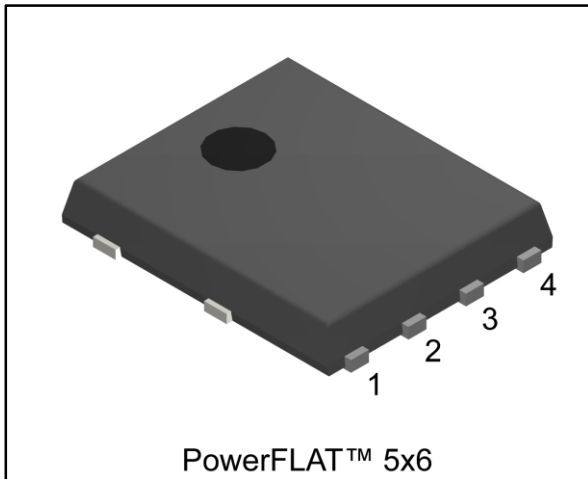


Figure 1: Internal schematic diagram

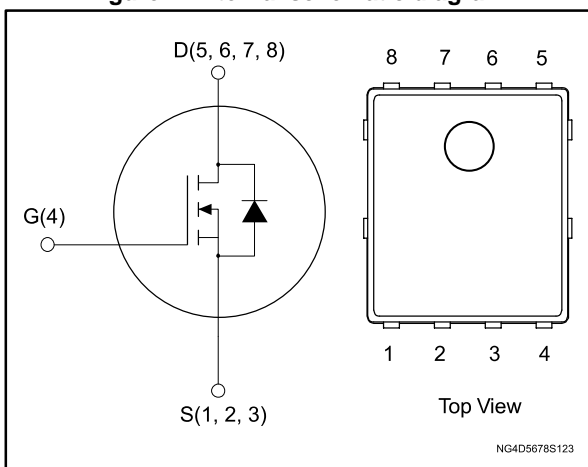


Table 1: Device summary

Order code	Marking	Package	Packing
STL100N12F7	100N12F7	PowerFLAT™ 5x6	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)max}	I _D	P _{TOT}
STL100N12F7	120 V	7.5 mΩ	100 A	136 W

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	120	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	100	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	71	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	400	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	18	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	13	A
$I_{DM}^{(3)(2)}$	Drain current (pulsed)	72	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	136	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_J	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		$^\circ\text{C}$

Notes:

- (1) This value is rated according to R_{thj-c} .
 (2) Pulse width limited by safe operating area.
 (3) This value is rated according to $R_{thj-pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.1	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.5	$^\circ\text{C}/\text{W}$

Notes:

- (1) When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	120			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 120\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 120\text{ V}, T_C = 125\text{ °C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$		6.3	7.5	m Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 60\text{ V}, f = 1\text{ MHz}$	-	3300	-	pF
C_{oss}	Output capacitance		-	1380	-	pF
C_{riss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	$V_{DD} = 60\text{ V}, I_D = 18\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	46	-	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain charge		-	10	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 60\text{ V}, I_D = 9\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	25	-	ns
t_r	Rise time		-	12.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	38	-	ns
t_f	Fall time		-	20	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 18 \text{ A}$	-	-	1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 18 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 96 \text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	73		ns
Q_{rr}	Reverse recovery charge		-	142		nC
I_{RRM}	Reverse recovery current		-	3.9		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curves)

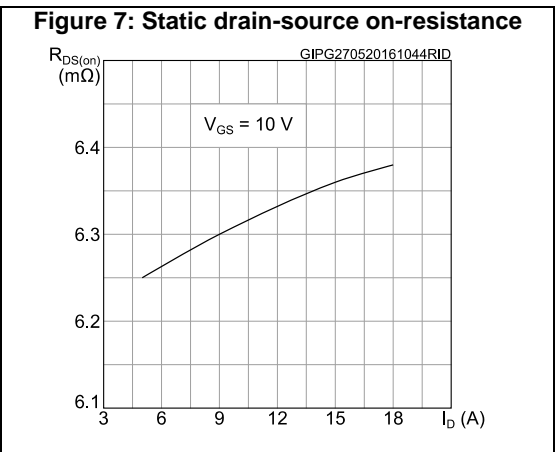
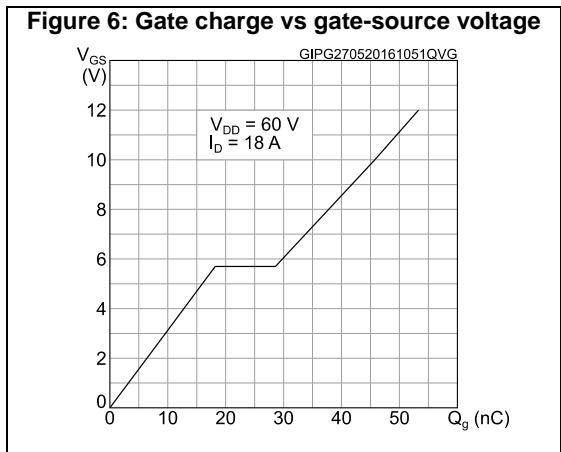
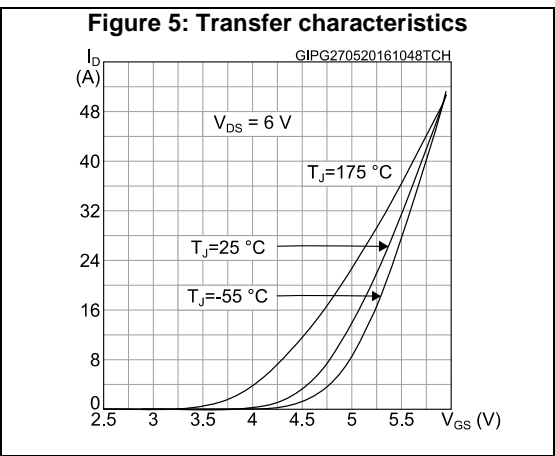
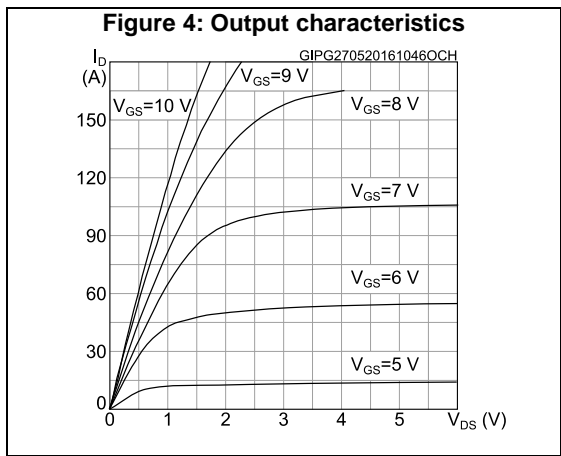
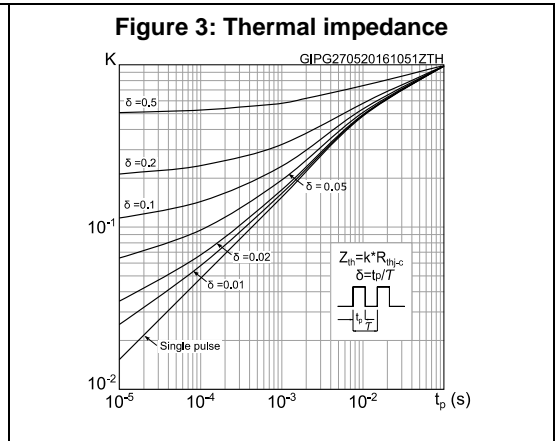
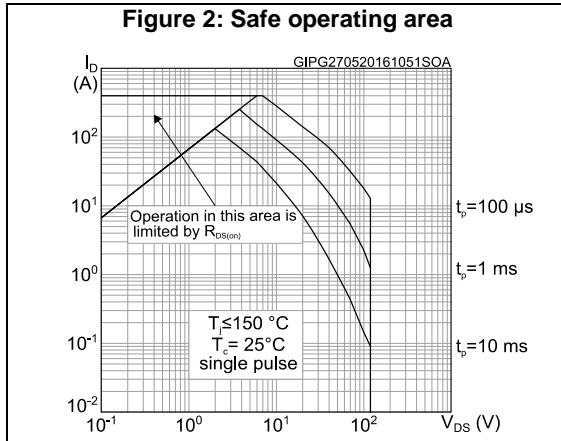


Figure 8: Capacitance variations

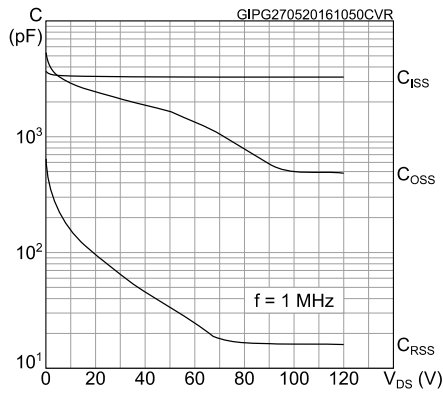


Figure 9: Normalized gate threshold voltage vs temperature



Figure 10: Normalized on-resistance vs temperature

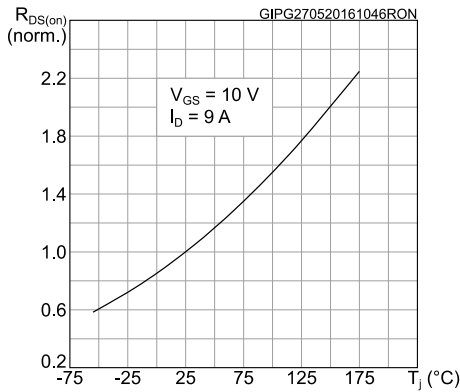


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

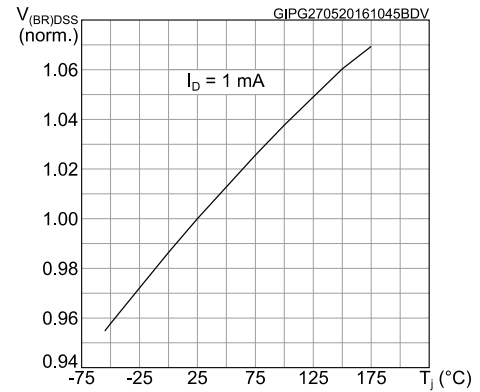
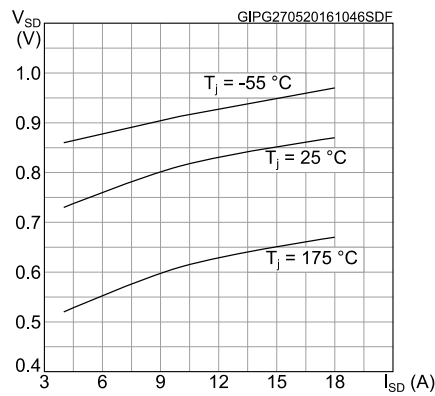
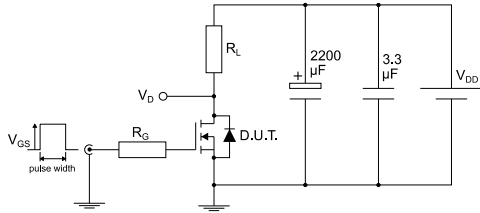


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times



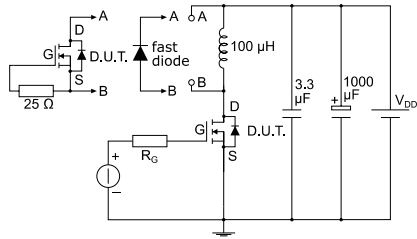
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Figure 14: Test circuit for gate charge behavior



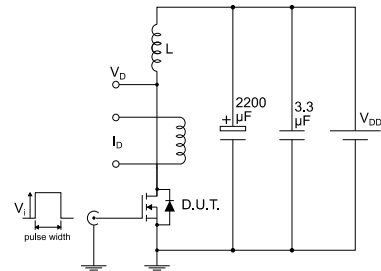
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Figure 15: Test circuit for inductive load switching and diode recovery times



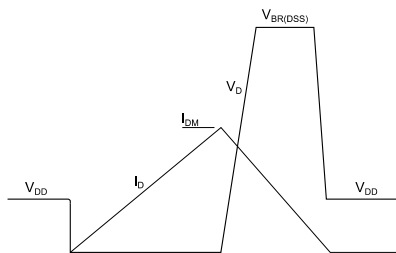
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Figure 16: Unclamped inductive load test circuit



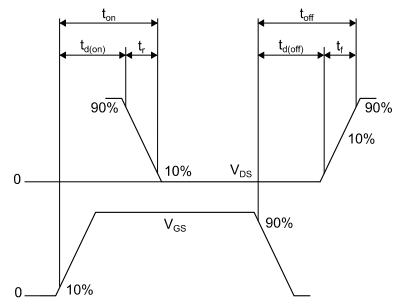
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 19: PowerFLAT™ 5x6 type C package outline

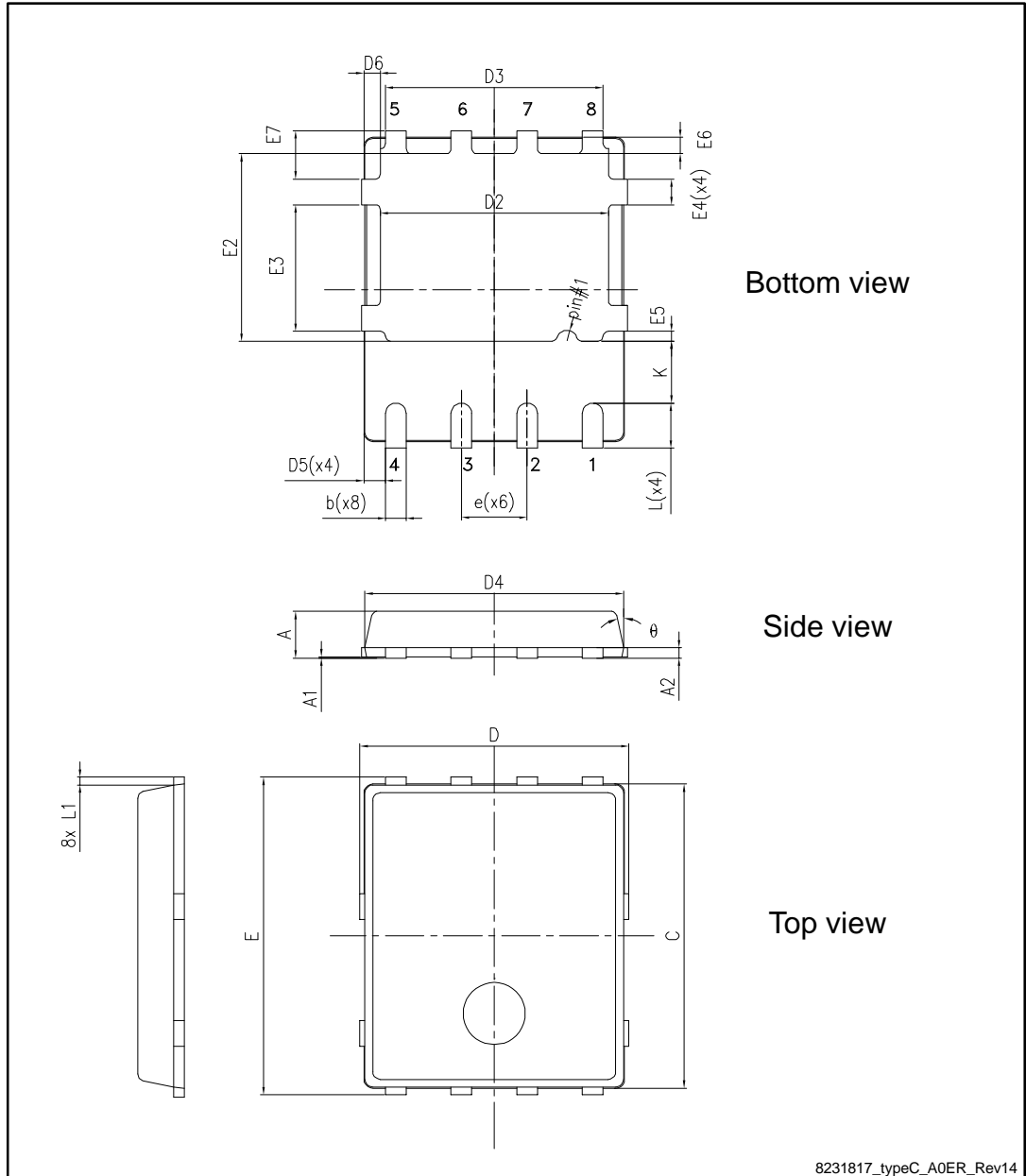
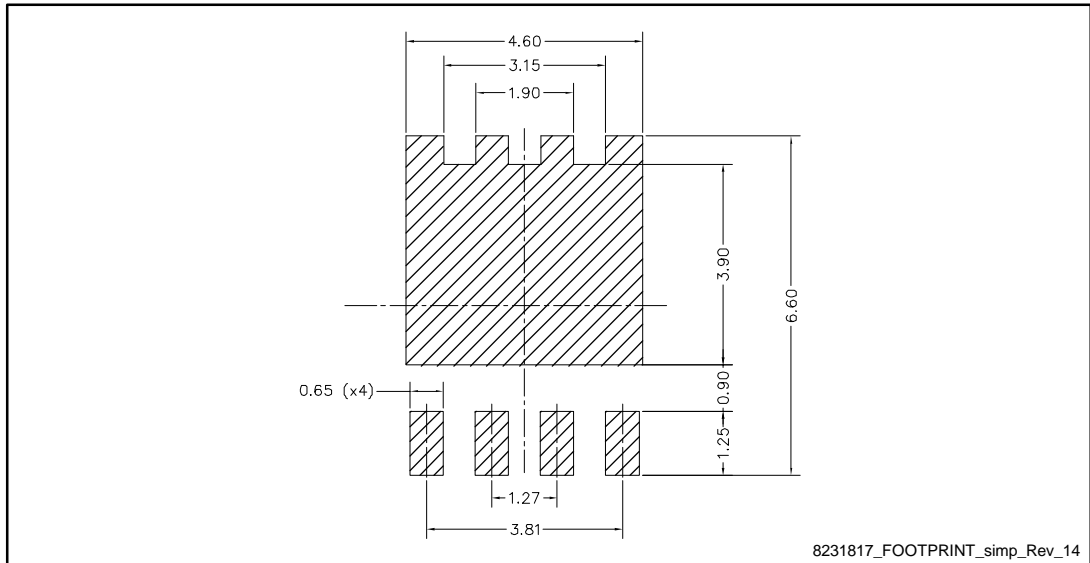


Table 8: PowerFLAT™ 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 type C packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

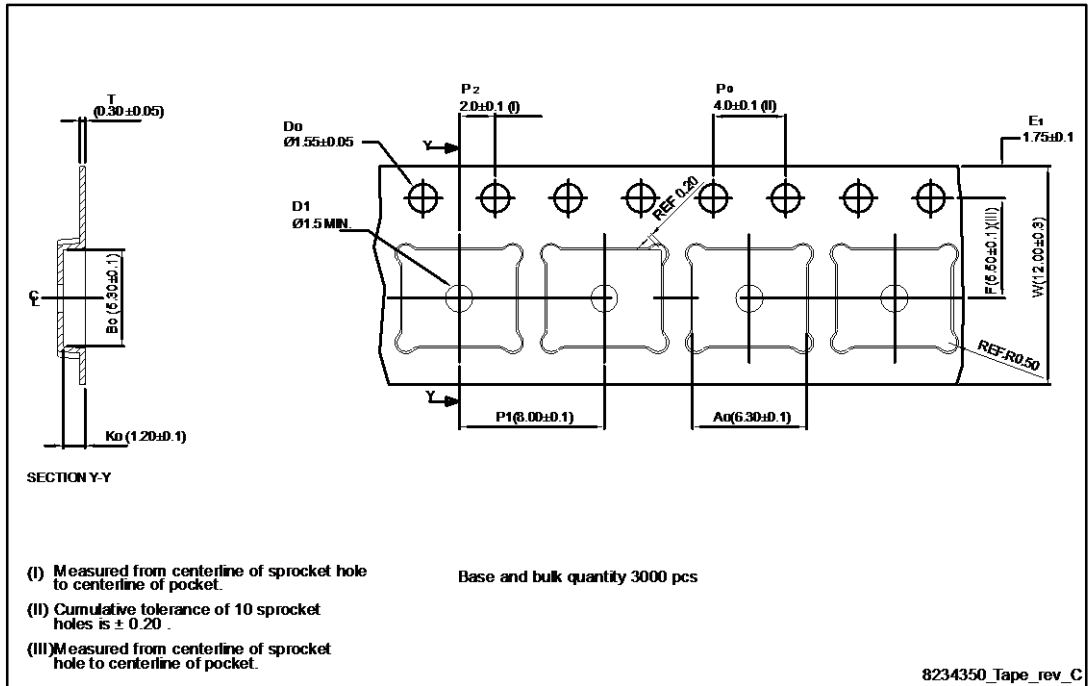


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

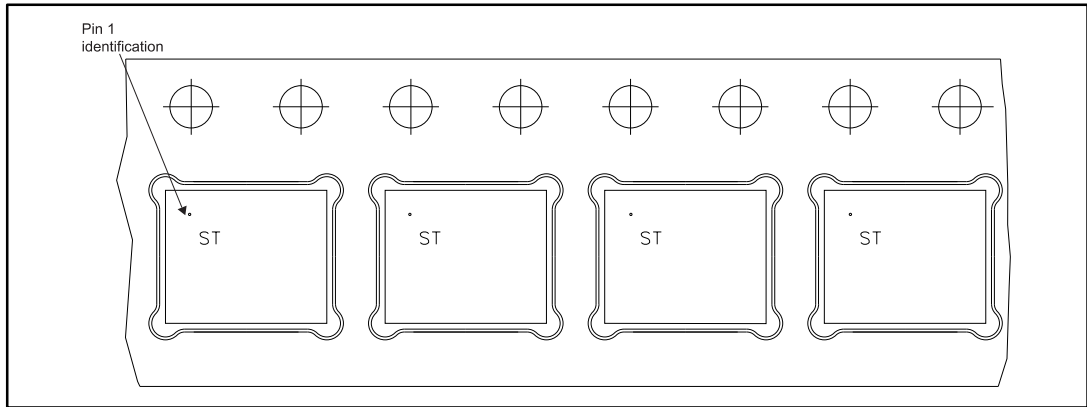
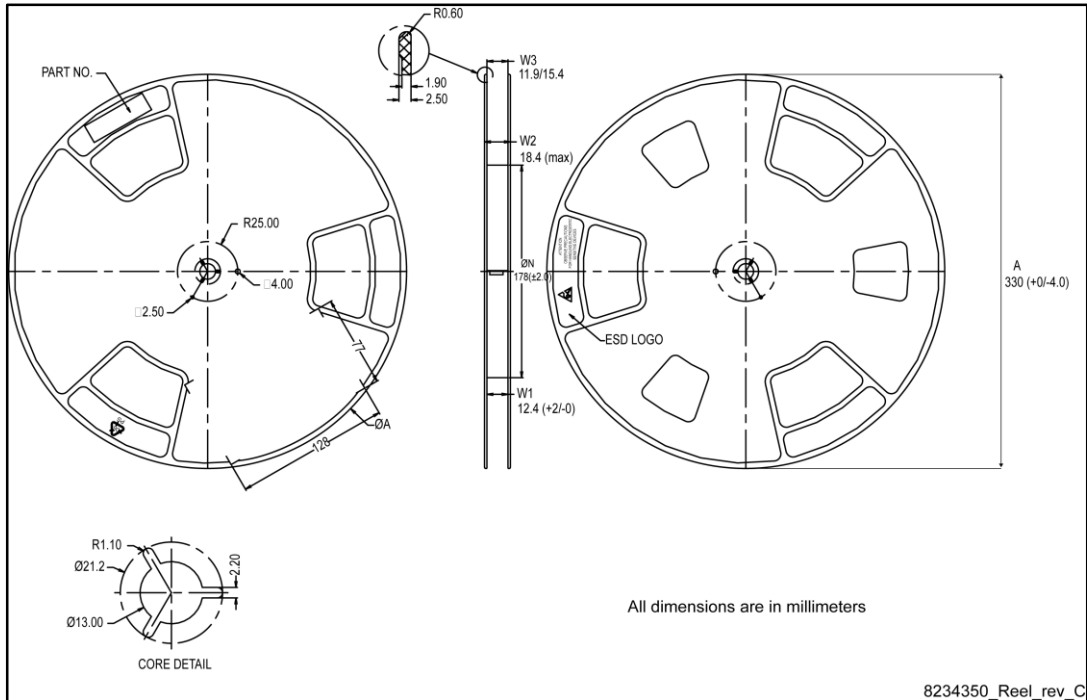


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
16-Jul-2015	1	Initial release.
03-Aug-2015	2	Updated section: Package information.
10-May-2016	3	Updated Table 2: "Absolute maximum ratings", Table 3: "Thermal data", Table 5: "Dynamic", Table 6: "Switching times" and Table 7: "Source drain diode". Updated Section 6.1: "PowerFLAT™ 5x6 type C package information". Minor text changes.
27-May-2016	4	Added: <i>Section 4.1: "Electrical characteristics (curves)"</i> . Minor text changes.
29-Aug-2016	5	Modified: <i>Figure 2: "Safe operating area"</i> Datasheet promoted from preliminary data to production data Minor text changes

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