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MC74VHC259

8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter

with LSTTL−Compatible Inputs

The MC74VHC259 is an 8−bit Addressable Latch fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL devices while maintaining CMOS low power dissipation.

The VHC259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table.. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non−addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one−of−eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the VHC259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The MC74VHC259 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC259 to be used to interface 5 V circuits to 3 V circuits.

- High Speed: t_{PD} = 7.6 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
- CMOS−Compatible Outputs: V_{OH} > 0.8 V_{CC}; V_{OL} < 0.1 V_{CC} @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V
- These Devices are Pb−Free and are RoHS Compliant

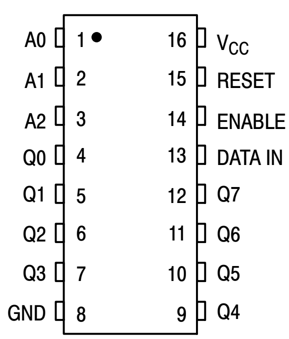

Figure 1. Pin Assignment

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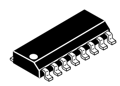
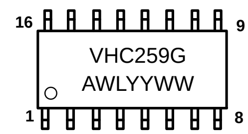
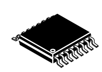
MARKING DIAGRAMS

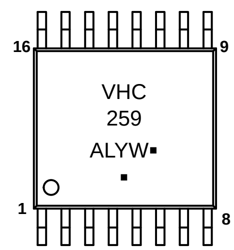


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC259DG	SOIC−16	48 Units/Rail
MC74VHC259DR2G	SOIC−16	2500 Units/Reel
MC74VHC259DTG	TSSOP−16	96 Units/Rail
MC74VHC259DTR2G	TSSOP−16	2500 Units/Reel

September, 2014 − Rev. 5

Publication Order Number:
MC74VHC259/D

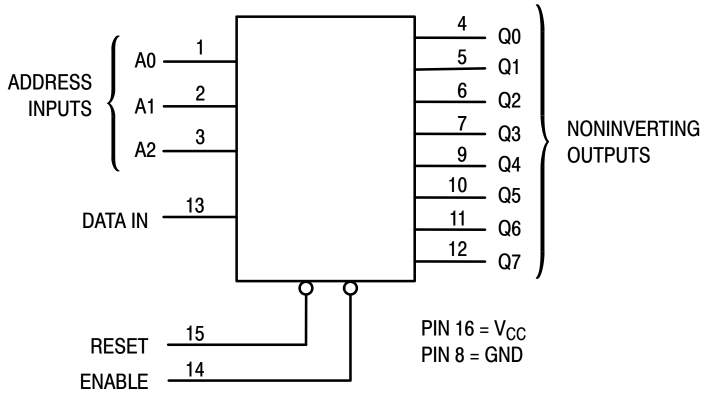


Figure 2. Logic Diagram

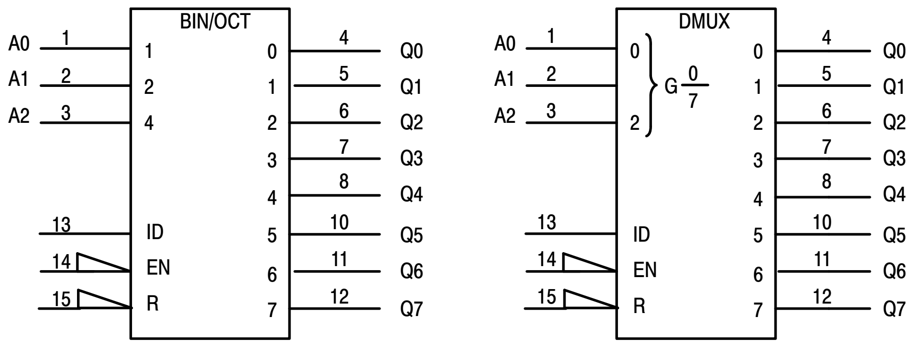


Figure 3. IEC Logic Symbol

LATCH SELECTION TABLE

Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8−Line Demultiplexer
H	L	Reset

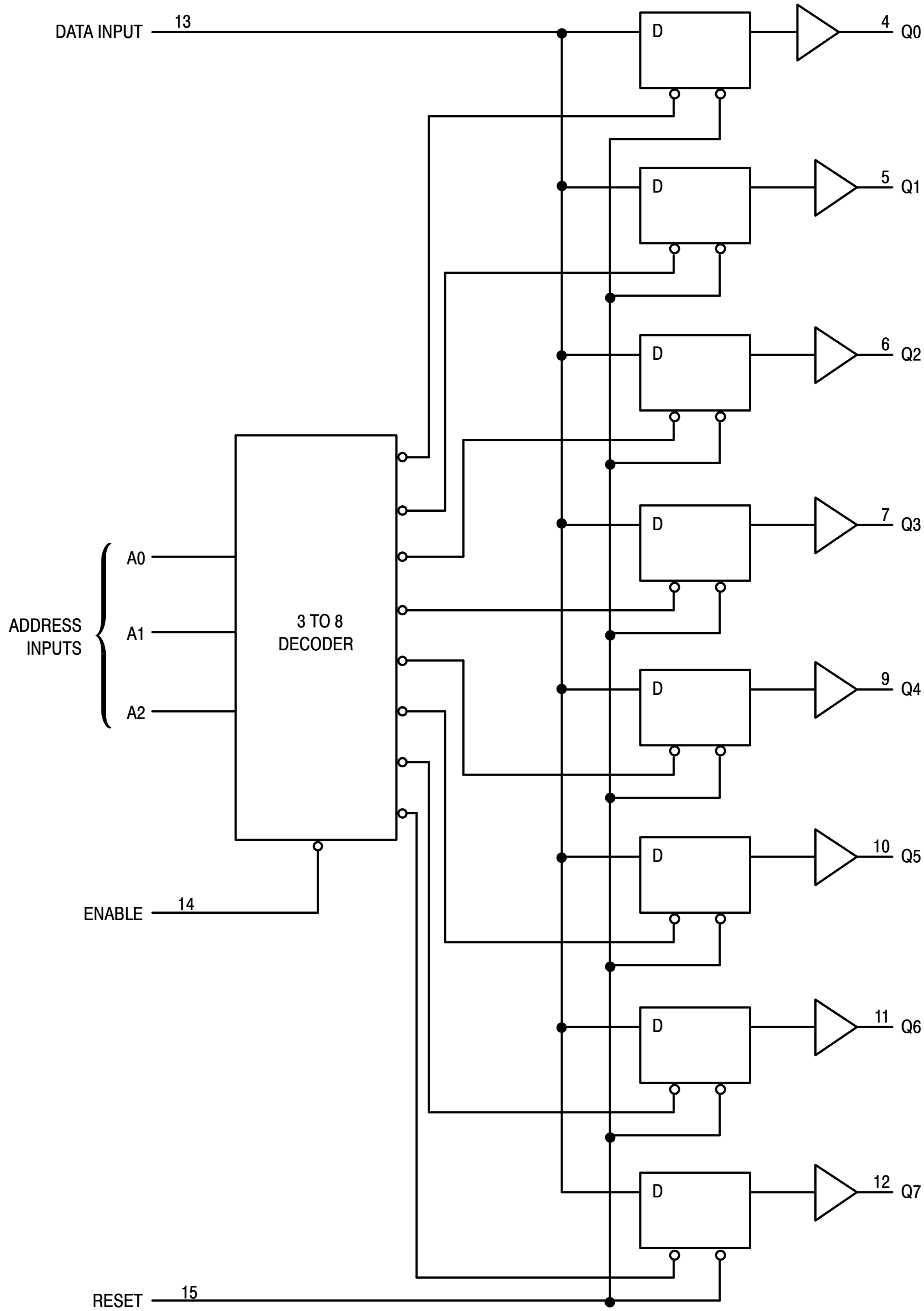


Figure 4. Expanded Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		± 20	mA
I_{OUT}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1.) Machine Model (Note 2.) Charged Device Model (Note 3.)	>2000 >200 >2000	V
$I_{LATCH-UP}$	Latch−Up Performance	Above V_{CC} and Below GND at 125°C (Note 4.)	± 300	mA
θ_{JA}	Thermal Resistance, Junction to Ambient	SOIC Package TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types		−55	125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 3.3 V $\pm$ 0.3 V V_{CC} = 5.0 V $\pm$ 0.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

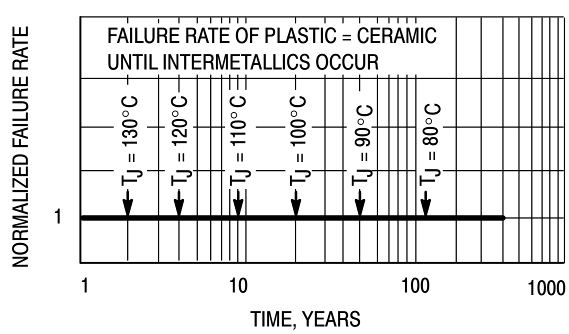


Figure 5. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C Min	Typ	Max	−55°C ≤ T_A ≤ 125°C Min	Max	Unit
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0to 5.5	1.5 V_{CCX} 0.7			1.5 V_{CCX} 0.7		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0to 5.5			0.5 V_{CCX} 0.3		0.5 V_{CCX} 0.3	V
V_{OH}	Maximum High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	 3.0 4.5	 2.58 3.94			 2.48 3.8		V
V_{OL}	Maximum Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 µA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	 3.0 4.5		 0.36 0.36			 0.44 0.44	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			4.0		40.0	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	Typ	Max	T_A ≤ 85°C Min	Max	−55°C ≤ T_A ≤ 125°C Min	Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Data to Output (Figures 6 and 11)	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		6.0 8.5	8.5 12.5	1.0 1.0	11.5 14.5	1.0 1.0	11.5 14.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.9 7.0	8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Address Select to Output (Figures 7 and 11)	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		6.0 8.5	8.5 12.5	1.0 1.0	11.5 14.5	1.0 1.0	11.5 14.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.9 7.0	8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to Output (Figures 8 and 11)	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		6.0 8.5	8.5 12.5	1.0 1.0	11.5 14.5	1.0 1.0	11.5 14.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.9 7.0	8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t_{PHL}	Maximum Propagation Delay, Reset to Output (Figures 9 and 11)	V_{CC} = 3.3 ± 0.3V	C_L = 15pF C_L = 50pF		6.0 8.5	8.5 12.5	1.0 1.0	11.5 14.5	1.0 1.0	11.5 14.5	ns
		V_{CC} = 5.0 ± 0.5V	C_L = 15pF C_L = 50pF		4.9 7.0	8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
C_{IN}	Maximum Input Capacitance				6	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1)	30	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0ns$)

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$T_A = \le 85°C$		$T_A = \le 125°C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_w	Minimum Pulse Width, Reset or Enable (Figure 10)	$V_{CC} = 3.3 \pm 0.3V$	5.0			5.5		5.5		ns
		$V_{CC} = 5.0 \pm 0.5V$	5.0			5.5		5.5		
t_{su}	Minimum Setup Time, Address or Data to Enable (Figure 10)	$V_{CC} = 3.3 \pm 0.3V$	4.5			4.5		4.5		ns
		$V_{CC} = 5.0 \pm 0.5V$	3.0			3.0		3.0		
t_h	Minimum Hold Time, Enable to Address or Data (Figure 8 or 9)	$V_{CC} = 3.3 \pm 0.3V$	2.0			2.0		2.0		ns
		$V_{CC} = 5.0 \pm 0.5V$	2.0			2.0		2.0		
t_r, t_f	Maximum Input, Rise and Fall Times (Figure 6)	$V_{CC} = 3.3 \pm 0.3V$			400		300		300	ns
		$V_{CC} = 5.0 \pm 0.5V$			200		100		100	

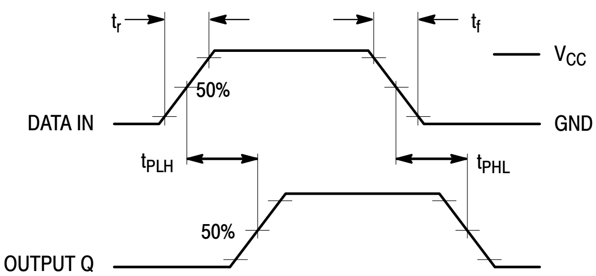


Figure 6. Switching Waveform

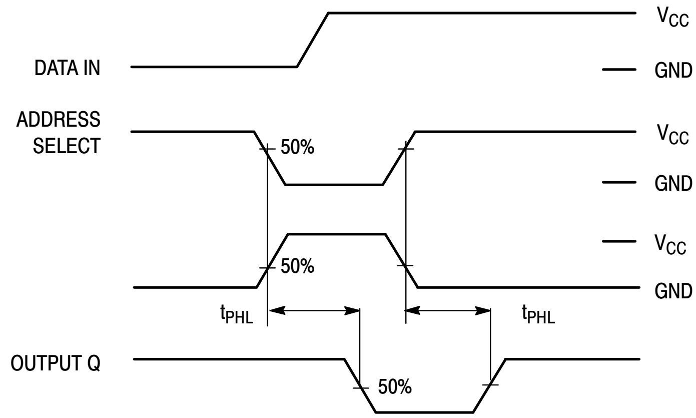


Figure 7. Switching Waveform

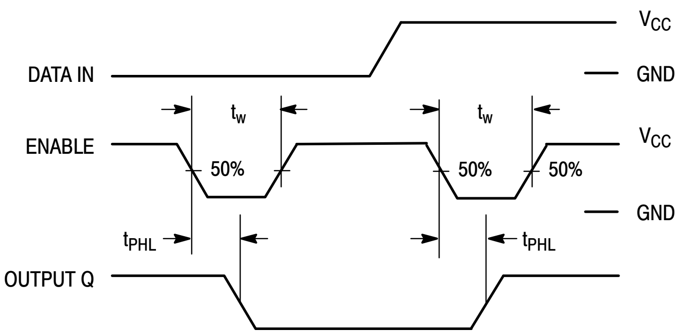


Figure 8. Switching Waveform

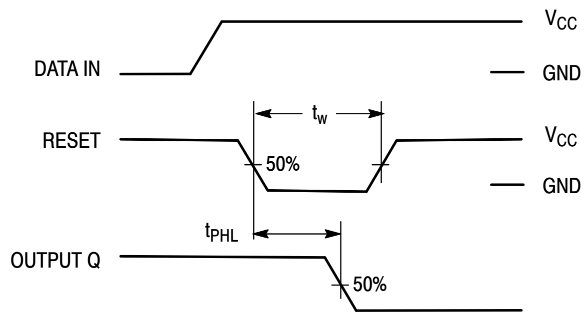


Figure 9. Switching Waveform

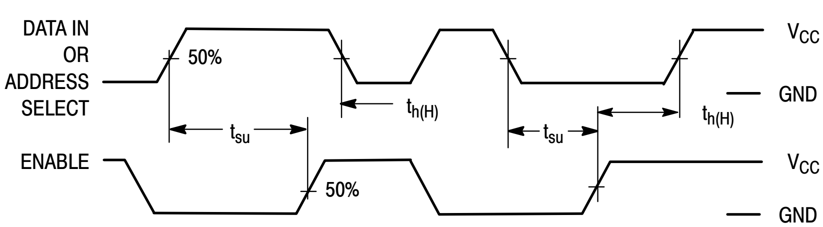
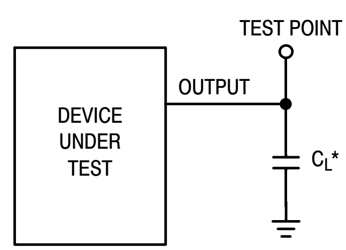


Figure 10. Switching Waveform

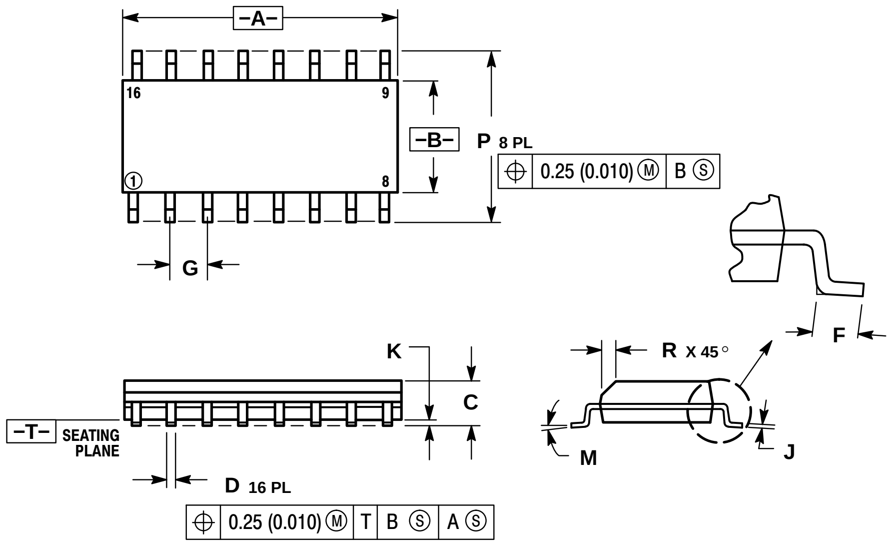


*Includes all probe and jig capacitance

Figure 11. Test Circuit

PACKAGE DIMENSIONS

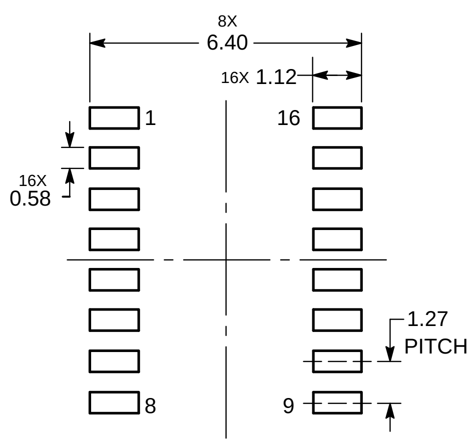
SOIC−16
CASE 751B−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

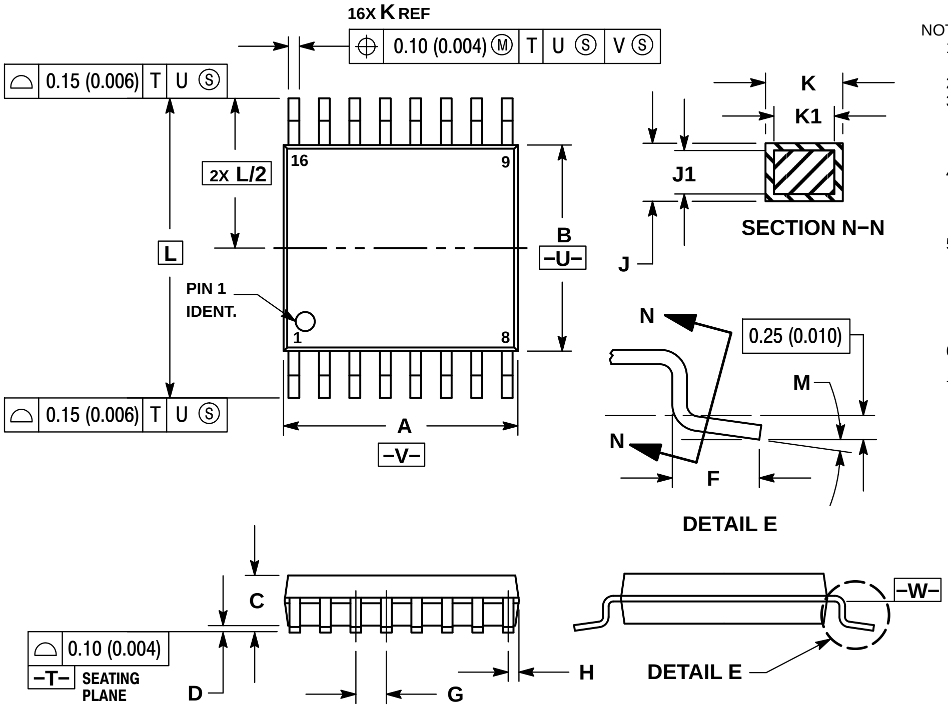
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

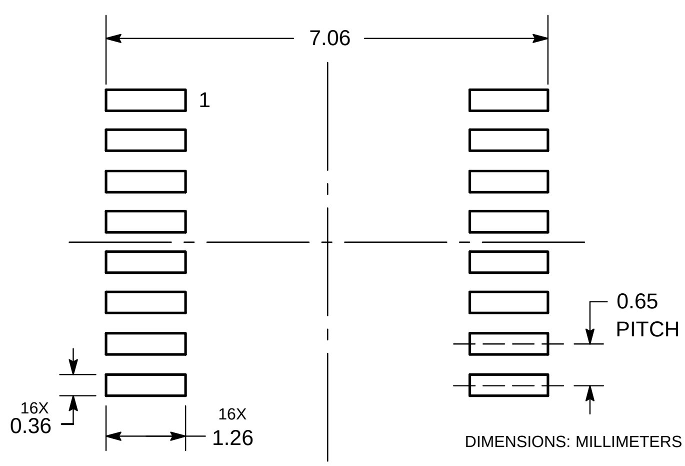
TSSOP−16
CASE 948F
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



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