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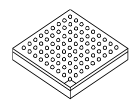
i.MX 7Solo Family of Applications Processors Datasheet



Package Information
Plastic Package
BGA 12 x 12 mm, 0.4 mm pitch
BGA 19 x 19 mm, 0.75 mm pitch

Ordering Information
See Table 1 on page 3

1 i.MX 7Solo introduction

The i.MX 7Solo family of processors represents NXP's latest achievement in high-performance processing for low-power requirements with a high degree of functional integration. These processors are targeted towards the growing market of connected and portable devices.

The i.MX 7Solo family of processors features advanced implementation of the ARM® Cortex®-A7 core, which operates at speeds of up to 800 MHz. The i.MX 7Solo family provides up to 32-bit DDR3/DDR3L/LPDDR2/LPDDR3-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

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The i.MX 7Solo family of processors is specifically useful for applications such as:

- Audio
- Connected devices
- Access control panels
- Human-machine interfaces (HMI)
- Portable medical and health care
- IP phones
- Smart appliances
- Point of Sale
- eReaders
- Wearables
- Home energy management systems

The features of the i.MX 7Solo family of processors include the following:

- ARM Cortex-A7 plus ARM Cortex-M4—Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux/Android on the Cortex-A7 core and an RTOS like FreeRTOS™ on the Cortex-M4 core.
- ARM Cortex-A7 core—The processor enhances the capabilities of portable, connected applications by fulfilling the ever-increasing MIPS needs of operating systems and applications at lowest power consumption levels per MHz.
- Multilevel memory system—The multilevel Cortex-A7 memory system is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, DDR3L, LPDDR2 and LPDDR3, NOR Flash, NAND Flash (MLC and SLC), QSPI Flash, and managed NAND, including eMMC rev.
- Power efficiency—Power management implemented throughout the IC enables features and peripherals to consume minimum power in both active and various low-power modes.
- Multimedia—The multimedia performance is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) coprocessor, a programmable smart DMA (SDMA) controller.
- Gigabit Ethernet with AVB—10/100/1000 Mbps Ethernet controllers supporting IEEE Std 1588 time synchronization.
- Human-machine interface (HMI)—i.MX 7Solo processor provides up to two separate display interfaces (parallel display and two-lane MIPI-DSI), CMOS sensor interface (two-lane MIPI-CSI and parallel).
- Interface flexibility—i.MX 7Solo processor supports connections to a variety of interfaces: one high-speed USB on-the-go module with PHY, High-Speed Inter-Chip USB, multiple expansion card ports (high-speed MMC/SDIO host and other), a Gigabit Ethernet controller with support for Ethernet AVB, two 12-bit ADCs with a total of 8 single-ended inputs, two CAN ports, and a variety of other popular interfaces (such as UART, I^2C, and I^2S).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure

software downloads. The security features are discussed in detail in the i.MX 7Dual security reference manual.

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different power domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 7Solo features, see Section 1.2, "Features."

1.1 Ordering information

Table 1 provides examples of orderable sample part numbers covered by this data sheet.

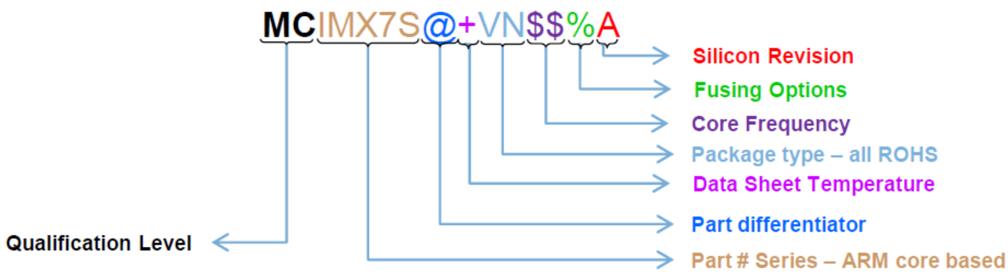
Table 1. Orderable parts

Part Number	Options	Cortex-A7 CPU Speed Grade	Qualification Tier	Temperature (T_j)	Package
MCIMX7S5EVM08SC	CAN, 1 x Gb ETH 10 tamper pins 2 x ADC	800 MHz	Industrial[1]	-20 to +105°C	19x19 mm 0.75mm pitch BGA
MCIMX7S3DVK08SC	No CAN, 1 x Gb ETH 4 tamper pins 1 x ADC	800 MHz	Consumer[2]	0 to +95°C	12x12 mm 0.4 mm pitch BGA
MCIMX7S5EVK08SC	CAN 1 x Gb ETH 4 tamper pins 1 x ADC	800 MHz	Industrial[1]	–20 to +105°C	12x12 mm 0.4 mm pitch BGA
MCIMX7S3EVK08SC	No CAN 1 x Gb ETH 4 tamper pins 1 x ADC	800 MHz	Industrial[1]	–20 to +105°C	12x12 mm 0.4 mm pitch BGA

[1] Industrial qualification grade assumes 10-year lifetime with 100% duty cycle.

[2] Consumer qualification grade assumes 5-year lifetime with 50% duty cycle.

Figure 1 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.



Qualification Level	MC
Samples	PC
Mass	MC
Special	SC

Part # Series	
IMX7D	2 x Cortex-A7 2 x USB2.0 OTG (w/ PHY) 1 x PCIe 3 x SDIO/MMC,
IMX7S	1 x Cortex-A7 1 x USB2.0 OTG (w/ PHY) 3 x SDIO/MMC

Part differentiator	@
Add 2x CAN and EPDC	7
Adds 2x CAN	5
Baseline Feature-set	3

Temperature Tj	+
Consumer: 0 to + 95°C	D
Extended Cons: -20 to + 105°C	E

Package Type	ROHS
MAPBGA 19x19 0.75mm	VM
MAPBGA 12 x12 0.4mm	VK

Frequency	$$
800 MHz	08
1 GHz	10

Fusing	%
Security Enabled	S
Security Disabled	A

Silicon Rev	A
Rev 1.0	A
Rev 1.1	B
Rev 1.2	C

Figure 1. Part number nomenclature—i.MX 7Solo family of processors

1.2 Features

The i.MX 7Solo family of processors is based on ARM Cortex-A7 MPCore™ Platform, which has the following features:

- ARM Cortex-A7 Core (with TrustZone® technology)
- The core includes:
  — 32 KByte L1 Instruction Cache
  — 32 KByte L1 Data Cache
  — Private Timer and Watchdog
  — NEON MPE (media processing engine) coprocessor

The ARM Cortex-A7 Core complex shares:

- General interrupt controller (GIC) with 128 interrupt support
- Global timer
- Snoop control unit (SCU)
- 512 KB unified I/D L2 cache
- Two master AXI bus interfaces output of L2 cache

- Frequency of the core (including NEON and L1 cache), as per Table 9.
- NEON MPE coprocessor
  — SIMD Media Processing Architecture
  — NEON register file with 32x64-bit general-purpose registers
  — NEON Integer execute pipeline (ALU, Shift, MAC)
  — NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  — NEON load/store and permute pipeline

The ARM Cortex-M4 platform:

- Cortex-M4 CPU core
- MPU (memory protection unit)
- FPU (floating-point unit)
- 16 KByte instruction cache
- 16 KByte data cache
- 64 KByte TCM (tightly-coupled memory)

The SoC-level memory system consists of the following additional components:

  — Boot ROM, including HAB (96 KB)
  — Internal multimedia / shared, fast access RAM (256 KB of total OCRAM)
  — Secure/nonsecure RAM (32 KB)
- External memory interfaces: The i.MX 7Solo family of processors supports the latest, high-volume, cost effective DRAM, NOR, and NAND Flash memory standards.
  — Up to 32-bit LP-DDR2-1066, DDR3-1066, DDR3L-1066, and LPDDR3-1066
  — 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 62 bits.
  — 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.

Each i.MX 7Solo processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Available interfaces.
  — One parallel 24-bit display port
  — One MIPI DSI port
- Camera sensors:
  — One parallel Camera port (up to 24 bit and up to 133 MHz peak)
  — One MIPI-CSI port
- Expansion cards:
  — Three MMC/SD/SDIO card ports all supporting the following. Moreover, the third port can support HS400.
    – 1-bit or 4-bit transfer mode specifications for SD and SDIO cards, up to 208 MHz

    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS200 and HS400 DDR modes
- USB:
  - One high-speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - One high-speed USB 2.0 (480 Mbps) host with integrated HSIC USB (high-speed inter-chip USB) PHY
- Miscellaneous IPs and interfaces:
  - Three instances of SAI supporting up to three I^2S and AC97 ports
  - Seven UARTs, up to 4.0 Mbps:
    - Providing RS232 interface
    - Supporting 9-bit RS485 Multidrop mode
  - Four eCSPI (Enhanced CSPI)
  - Four I^2C, supporting 400 kbps
  - 1-gigabit Ethernet controller (designed to be compatible with IEEE Std 1588), 10/100/1000 Mbps with AVB support
  - Four pulse width modulators (PWM)
  - System JTAG controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 key pad port (KPP)
  - One quad SPI
  - Four watchdog timers (WDOG)
  - One (12 x 12 mm) or two (19 x 19 mm) 2-channel, 12-bit analog-to-digital converters (ADC)—effective number of bits (ENOB) can vary (typically 9–10 bits) depending on the system implementation and the condition of the power/ground noise condition

The i.MX 7Solo family of processors integrates advanced power management unit and controllers:

- PMU (power-management unit), multiple LDO supplies, for on-chip resources
- Temperature sensor for monitoring the die temperature
- Software state retention and power gating for ARM and NEON
- Support for various levels of system power modes
- Flexible clock gating control scheme

The i.MX 7Solo family of processors uses dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 7Solo family of processors incorporates the following hardware accelerators:

- PXP—PiXel processing pipeline for imagine resize, rotation, overlay and CSC. Off loading key pixel processing operations are required to support the LCD.

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone technology including separation of interrupts and memory mapping

- SJC—System JTAG controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic acceleration and assurance module, containing cryptographic and hash engines supporting DPA (differential power analysis) protection, 32 KB secure RAM, and true and pseudo random number generator (NIST certified).
- SNVS—Secure non-volatile storage, including secure real time clock
- CSU—Central security unit. Enhancement for the IC identification module (IIM). Configured during boot and by eFuses and determines the security-level operation mode as well as the TrustZone policy.
- A-HAB—Advanced high-assurance boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, SRK revocation mechanism, warm boot, CSU, and TrustZone initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1. Functions, such as display and camera interfaces, connectivity interfaces, may not be enabled for specific part numbers.

2 Architectural overview

The following subsections provide an architectural overview of the i.MX 7Solo processor system.

2.1 Block diagram

Figure 2 shows the functional modules in the i.MX 7Solo processor system.

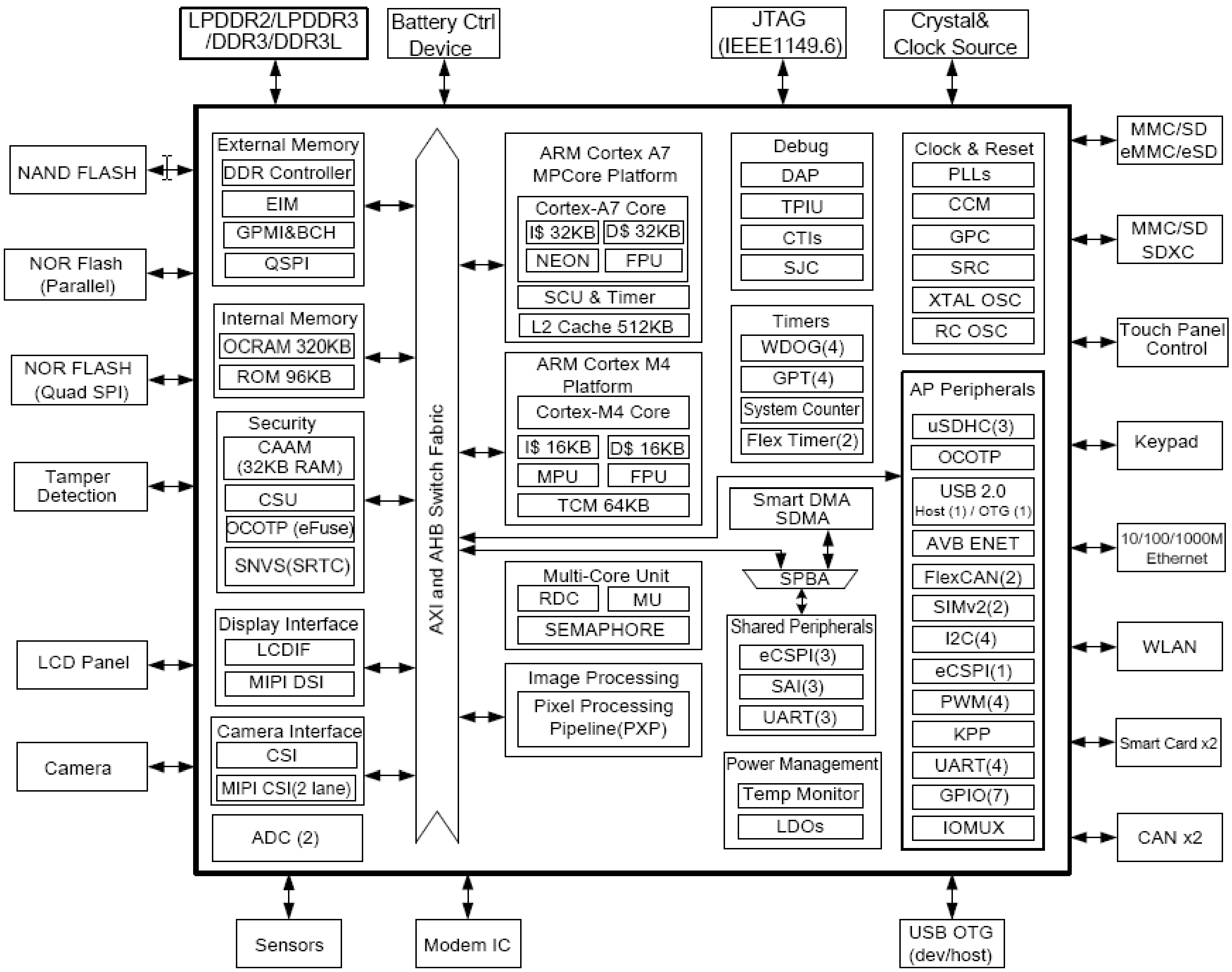


Figure 2. i.MX 7Solo System block diagram

3 Modules list

The i.MX 7Solo family of processors contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 7Solo modules list

Block Mnemonic	Block Name	Subsystem	Brief Description
ADC1 ADC2	Analog to Digital Converter		The ADC is a 12-bit general purpose analog to digital converter (ADC2 is not available in the 12x12 package).
ARM	ARM Platform	ARM	The ARM Core Platform includes a Cortex-A7 core and 1x Cortex-M4. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
BCH	Binary-BCH ECC Processor	System control peripherals	The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certifiable by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 7Solo processors, the security memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, resets, and power control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.
CSU	Central Security Unit	security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 7Solo platform.
DAP	Debug Access Port	System control peripherals	The DAP provides real-time access for the debugger without halting the core to access: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.

Table 2. i.MX 7Solo modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support for 16-bit (in Muxed I/O mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support for 16-bit (in muxed and non-muxed I/O modes) NOR-Flash memories, at slow frequency • Multiple chip selects
ENET1	Ethernet Controller	Connectivity peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) for details.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
FLEXTIMER1 FLEXTIMER2	Flexible Timer Module	Timer Peripherals	Provide input signal capture and PWM support
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7	General Purpose I/O Modules	System control peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPMI	General Purpose Memory Interface	Connectivity peripherals	The GPMI module supports up to 8x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.

Table 2. i.MX 7Solo modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPT	General Purpose Timer	Timer peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
I2C1 I2C2 I2C3 I2C4	I^2C Interface	Connectivity peripherals	I^2C provide serial interface for external devices. Data rates of up to 320 kbps are supported.
IOMUXC	IOMUX Control	System control peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
KPP	Key Pad Port	Connectivity peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LCDIF	LCD interface	Multimedia peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface).
MIPI-CSI (two-lane)	MIPI Camera Interface	Multimedia peripherals	This module provides a two-lane MIPI camera interface operating up to a maximum bit rate of 1.5 Gbps.
MIPI DSI (two-lane)	MIPI Display Interface	Connectivity peripherals	This module provides a two-lane MIPI display interface operating up to a maximum bit rate of 1.5 Gbps.
DDRC	DDR Controller	Connectivity peripherals	The DDR Controller has the following features: • Supports 16/32-bit DDR3/DDR3L, LPDDR3, and LPDDR2-1066 • Supports up to 2 Gbyte DDR memory space
MQS	Medium-quality sound module	Multimedia peripherals	MQS is used to generate 2-channel, medium-quality, PWM-like audio, via two standard digital GPIO pins. The electronic specification is the same as the GPIO digital output.

Table 2. i.MX 7Solo modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 7Solo processors, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
PMU	Power Management Unit	Data path	Integrated power management unit. Used to provide power to various SoC domains.
PWM1 PWM2 PWM3 PWM4	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	PiXel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications.
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module act as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master

Table 2. i.MX 7Solo modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SAI1 SAI2 SAI3	Synchronous Audio Interface	Connectivity peripherals	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I^2S, AC97, TDM, and codec/DSP interfaces.
SDMA	Smart Direct Memory Access	System control peripherals	The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (Copy mode) • Up to 8-word buffer for configurable burst transfers for EMIv2.5 • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SIMv2-1 SIMv2-2	Smart Card	Connectivity peripherals	Smart card interface designed to be compatible with ISO7816.
SJC	System JTAG Controller	System control peripherals	The SJC provides JTAG interface (designed to be compatible with JTAG TAP standards) to internal logic. The i.MX 7Solo family of processors uses JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, designed to be compatible with IEEE 1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 7Solo SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
TEMPSENSOR	Temperature Sensor	System control peripherals	Temperature sensor

Table 2. i.MX 7Solo modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4 UART5 UART6 UART7	UART Interface	Connectivity peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud
uSDHC1 uSDHC2 uSDHC3	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity peripherals	i.MX 7Solo SoC characteristics: All the MMC/SD/SDIO controller IPs are based on the uSDHC IP. They are designed to be: • Fully compatible with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2. • Fully compatible with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications v 3.0 including high-capacity SDXC cards up to 2 TB. • Fully compatible with SDIO command/response sets and interrupt/Read-Wait mode as defined in the SDIO Card Specification, Part E1, v. 3.0 All the ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS200 and HS400. However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • uSDHC1 and uSDHC2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. • uSDHC3 is primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for uSDHC1 and uSDHC2 in 4-bit configuration (SD interface). uSDHC3 is placed in his own independent power domain.

Table 2. i.MX 7Solo modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
USBOTG2	USB 2.0 High Speed OTG and HSIC USB	Connectivity peripherals	USBOTG2 contains: • One high-speed OTG module with integrated HS USB PHYs • One high-speed Host module connected to HSIC USB port.
WDOG1 WDOG3 WDOG4	Watchdog	Timer peripherals	The Watch dog timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG2 (TrustZone)	Watchdog (TrustZone technology)	Timer peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping Normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.

3.1 Special signal considerations

Table 3 lists special signal considerations for the i.MX 7Solo family of processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments." Signal descriptions are provided in the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

Table 3. Special signal considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N CCM_CLK2	One general purpose differential high speed clock input/output and one single-ended clock input are provided. Either or both of them can be used: • To feed an external reference clock to the PLLs and to the modules inside the SoC, for example, as an alternate reference clock for Video/Audio interfaces and so forth. • To output the internal SoC clock to be used outside the SoC as either a reference clock or as a functional clock for peripherals; for example, it can be used as an output of the PCIe master clock (root complex use) See the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) for details on the respective clock trees. The CCM_CLK1_* inputs/outputs are an LVDS differential pair. Alternatively, a single-ended signal may be used to drive CCM_CLK1_P input. In this case corresponding CCM_CLK1_N input should be tied to the constant voltage level equal to 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See the LVDS pad electrical specification for further details. CCM_CLK2 is a single-ended input referenced to ground. After initialization: • The CCM_CLK1_* inputs/outputs can be disabled if not used. Any of the unused CCM_CLK1_* pins may be left floating. • The CCM_CLK2 input should be grounded if not used.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (100 k ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. It is recommended to use the configurable load capacitors provided in the IP instead of adding them externally. To hit the exact oscillation frequency, the configurable capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 M). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level. In the case when a high-accuracy realtime clock is not required, the system may use internal low frequency oscillator. It is recommended to connect RTC_XTALI to ground and keep RTC_XTALO floating. This will however result in increased power consumption, because the internal oscillator uses higher power than the RTC oscillator. Thus for lowest power configuration it is recommended to always install a crystal.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO.

Table 3. Special signal considerations(continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 7Solo are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more than eight devices)
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
VDDA_MIPI_1P8	Short these pins to VDDA_PHY_1P8 if using MIPI. User can leave these pins floating or grounded if not using MIPI.
VDD_MIPI_1P0	Short these pins to VDDD_1P0_CAP if using MIPI. User can leave these pins floating or grounded if not using MIPI.
GPANAIO	This signal is reserved for manufacturing use only. User must leave this connection floating.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM). Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to high configures the JTAG interface to a mode compatible with the IEEE 1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	Do not connect. These signals are reserved and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	In Normal mode, may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
TEST_MODE	TEST_MODE is for factory use. This signal is internally connected to an on-chip pull-down device. The user must tie this signal to GND.
USB_OTG1_REXT/USB_OTG2_REXT	The bias generation and impedance calibration process for the USB OTG PHYs requires connection of 200 Ω (1% precision) reference resistors on each of the USB_OTG1_REXT and USB_OTG2_REXT pads to ground.

Table 3. Special signal considerations(continued)

Signal Name	Remarks
USB_OTG1_CHD_B	An external pullup resistor with value in range from 10 kΩ to 100 kΩ should be connected between open-drain output USB_OTG1_CHD_B and supply VDD_USB_OTG1_3P3_IN for 3.3 V signaling. Optionally, a similarly valued pullup resistor could be connected instead between USB_OTG1_CHD_B and an unrelated supply up to 1.8 V, but in that case the output is only valid when both that supply and VDD_USB_OTG1_3P3_IN are powered.
TEMPSENSOR_REXT	External 100 KΩ (1% precision) resistor connection pin

Table 4. JTAG controller interface summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	100 kΩ pull-up
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended connections for unused analog interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended connections for unused analog interfaces

Module	Package Net Name	Recommendation if Unused
ADC	VDDA_ADC2_1P8, VDDA_ADC2_1P8, VDDA_ADC1_1P8, VDDA_ADC1_1P8	1.8 V
	ADC2_IN3, ADC2_IN2, ADC2_IN1, ADC2_IN0, ADC1_IN0, ADC1_IN1, ADC1_IN2, ADC1_IN3	Tie to ground
LDO	VDD_1P2_CAP	Floating if USB_HSIC is not used
MIPI	VDD_MIPI_1P0, VDDA_MIPI_1P8	Floating or tie to ground
	MIPI_DSI_D0_N, MIPI_DSI_D0_P, MIPI_VREG_0P4V, MIPI_DSI_CLK_N, MIPI_DSI_CLK_P, MIPI_DSI_D1_N, MIPI_DSI_D1_P, MIPI_CSI_D0_N, MIPI_CSI_D0_P, MIPI_CSI_CLK_N, MIPI_CSI_CLK_P, MIPI_CSI_D1_N, MIPI_CSI_D1_P	No connect
PCIe	PCIE_REFCLKIN_N, PCIE_REFCLKIN_P, PCIE_REFCLKOUT_N, PCIE_REFCLKOUT_P, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, PCIE_TX_P	Floating
	PCIE_VP,PCIE_VP_RX,PCIE_VP_TX, PCIE_VPH,PCIE_VPH_RX,PCIE_VPH_TX, PCIE_REXT	Tie to ground

Table 5. Recommended connections for unused analog interfaces(continued)

Module	Package Net Name	Recommendation if Unused
SNVS	SNVS_TAMPER00, SNVS_TAMPER01, SNVS_TAMPER02, SNVS_TAMPER03, SNVS_TAMPER04, SNVS_TAMPER05, SNVS_TAMPER06, SNVS_TAMPER07, SNVS_TAMPER08, SNVS_TAMPER09	Float—configure with software
Temperature sensor	TEMPSENSOR_REXT	Tie to ground or pulldown with 100 KΩ resistor
	TEMPSENSOR_RESERVE	Floating
	VDD_TEMPSENSOR_1P8	1.8 V
USB HSIC	VDD_USB_H_1P2	Tie to ground
	USB_H_DATA, USB_H_STROBE	Floating
USB OTG1	VDD_USB_OTG1_3P3_IN, VDD_USB_OTG1_1P0_CAP	Tie to ground
	USB_OTG1_VBUS, USB_OTG1_DP, USB_OTG1_DN, USB_OTG1_ID, USB_OTG1_REXT, USB_OTG1_CHD_B	Floating
USB OTG2	VDD_USB_OTG2_3P3_IN, VDD_USB_OTG2_1P0_CAP	Tie to ground
	USB_OTG2_VBUS, USB_OTG2_DP, USB_OTG2_DN, USB_OTG2_ID, USB_OTG2_REXT	Floating

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 7Solo family of processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 7Solo Chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 20
FPBGA case “X” and case “Y” package thermal resistance	on page 21
Operating ranges	on page 21
External clock sources	on page 24
Maximum supply currents	on page 24
Power modes	on page 28
USB PHY Suspend current consumption	on page 31

4.1.1 Absolute maximum ratings

CAUTION

Stresses beyond those listed under Table 7 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operating ranges or parameters tables is not implied.

Table 7. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDD_ARM VDD_SOC	–0.5	1.5	V
GPIO supply voltage	NVCC_ENET1 NVCC_I2C NVCC_LCD NVCC_SAI NVCC_SD1 NVCC_SD2 NVCC_SD3 NVCC_SPI NVCC_UART	–0.3	3.6	V
DDR I/O supply voltage	NVCC_DRAM	–0.3	1.975	V
Clock I/O supply voltage	NVCC_DRAM_CKE	–0.3	1.98	V
VDD_SNVS_IN supply voltage	VDD_SNVS_IN	–0.3	3.6	V
USB OTG PHY supply voltage	VDD_USB_OTG1_3P3_IN VDD_USB_OTG2_3P3_IN	–0.3	3.6	V
USB_VBUS input detected	USB_OTG1_VBUS USB_OTG2_VBUS	–0.3	5.25	V
Input voltage on USB_OTG*_DP, USB_OTG*_DN pins	USB_OTG1_DP/USB_OTG1_DN USB_OTG2_DP/USB_OTG2_DN	–0.3	3.63	V
USB_OTG1_CHD_B open-drain pullup voltage when external pullup resistor is connected to VDD_USB_OTG1_3P3_IN supply only	USB_OTG1_CHD_B	—	3.6	V
USB_OTG1_CHD_B open-drain pullup voltage when external pullup resistor is connected to any supply other than VDD_USB_OTG1_3P3_IN	USB_OTG2_CHD_B	—	1.975	V
Input/output voltage range	V_{in}/V_{out}	–0.3	OVDD[1]+0.3	V
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	–40	150	°C

[1] OVDD is the I/O supply voltage.

4.1.2 Thermal resistance

4.1.2.1 FPBGA case “X” and case “Y” package thermal resistance

Table 8 displays the thermal resistance data.

Table 8. Thermal Resistance Data

Rating	Test conditions	Symbol	12x12 pkg value	19x19 pkg value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	55.4 32.6	44.4 30.2	°C/W °C/W
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	41.8 28.0	34.3 25.8	°C/W °C/W
Junction to Board[1,4]	—	$R_{\theta JB}$	16.0	17.4	°C/W
Junction to Case[1,5]	—	$R_{\theta JC}$	10.5	10.4	°C/W
Junction to Package Top[1,6]	Natural Convection	Ψ_{JT}	0.2	0.2	°C/W
Junction to Package Bottom	Natural Convection	$R_{\theta B\_CSB}$	15.3	17.3	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.
3 Per JEDEC JESD51-6 with the board horizontal.
4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating ranges

Table 9 provides the operating ranges of the i.MX 7Solo family of processors. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

Table 9. Operating ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run Mode	VDD_ARM	0.95	1.0	1.155	V	Operation at 800 MHz and below
	VDD_SOC	0.95	1.0	1.25	V	—
Standby/ Deep Sleep mode	VDD_ARM	0	1.0	1.25	V	See Table 14, “Power modes,” on page 28.
	VDD_SOC	0.95	1.0	1.155	V	

Table 9. Operating ranges(continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Power Supply Analog Domain and LDOs	VDDA_1P8	1.71	1.8	1.89	V	Power for analog LDO and internal analog blocks. Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN	2.4	3.0	3.6	V	—
LDO for Low-Power State Retention mode	VDD_LPSR	1.71	1.8	1.89	V	Power rail for Low Power State Retention mode
Supply for 24 MHz crystal	VDD_XTAL_1P8	1.650	1.8	1.950	V	—
Temperature sensor	VDD_TEMPSENSOR	1.710	1.8	1.890	V	—
USB supply voltages	VDD_USB_OTG1_3P3_IN	3.0	3.3	3.6	V	This rail is for USB
	VDD_USB_OTG2_3P3_IN	3.0	3.3	3.6	V	This rail is for USB
DDR I/O supply voltage	NVCC_DRAM, NVCC_DRAM_CKE	1.14	1.2	1.3	V	LPDDR2, LPDDR3
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3L
	DRAM_VREF	0.49 × NVCC_DRAM)	0.5 × NVCC_DRAM	0.51 × NVCC_DRAM	V	Set to one-half NVCC_DRAM
GPIO supply voltages	NVCC_ENET1 NVCC_I2C NVCC_LCD NVCC_SAI NVCC_SD1 NVCC_SD2 NVCC_SD3 NVCC_SPI NVCC_UART	1.65, 3.0	1.8, 3.3	1.95, 3.6	V	—
	NVCC_GPIO1	1.65 3.0	1.8, 3.3	1.95, 3.6	V	Power for GPIO1_DATA00 ~ GPIO1_DATA07
	NVCC_GPIO2	1.65 3.0	1.8, 3.3	1.95, 3.6	V	Power for GPIO1_DATA08 ~ GPIO1_DATA15 and JTAG port

Table 9. Operating ranges(continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Voltage rails supplied from internal LDO	VDDA_MIPI_1P8	1.71	1.8	1.89	V	Supplied from VDDA_PHY_1P8
	VDD_MIPI_1P0	0.95	1.0	1.050	V	Supplied from VDDD_CAP_1P0
	VDD_USB_H_1P2	1.150	1.2	1.250	V	Supplied from VDD_1P2_CAP
Temperature sensor accuracy	T_{delta}	—	±3	—	°C	Typical accuracy over the range –40°C to 125°C
A/D converter	VDDA_ADC1_1P8	1.71	1.8	1.89	V	—
	VDDA_ADC2_1P8	1.71	1.8	1.89	V	—
Fuse power	FUSE_FSOURCE	1.710	1.8	1.890	V	Power supply for internal use
Junction temperature, industrial	T_J	-20	—	105	°C	See Table 1 for complete list of junction temperature capabilities.

[1] Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This results in an optimized power/speed ratio. Operating a voltage of 1.2V and above will reduce the overall lifetime of the part. For details, see *i.MX 7Dual/Solo Product Lifetime Usage* (AN5334).

Table 10 shows on-chip LDO regulators that can supply on-chip loads.

Table 10. On-chip LDOs[1] and their on-chip loads

Voltage Source	Load	Comment
VDDD_1P0_CAP	VDD_MIPI_1P0	Connect directly (short) via board level
VDD_USB_H_1P2	VDD_USB_H_1P2	Connect directly (short) via board level
VDDA_PHY_1P8	VDDA_MIPI_1P8	Connect directly (short) via board level

[1] On-chip LDOs are designed to supply i.MX 7Solo loads and must not be used to supply external loads.

4.1.4 External clock sources

Each i.MX 7Solo processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal resistor-capacitor (RC) oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using internal oscillator amplifier.

Table 11 shows the interface frequency requirements.

Table 11. External input clock frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]	—	kHz
XTALI Oscillator[2,4]	f_{xtal}		24		MHz

1 External oscillator or a crystal with internal oscillator amplifier.
2 The required frequency stability of this clock source is application dependent. See *Hardware Development Guide for i.MX7Dual and 7Solo Applications Processors.*
3 Recommended nominal frequency 32.768 kHz.
4 External oscillator or a fundamental frequency crystal appropriately coupled to the internal oscillator amplifier.

The typical values shown in Table 11 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available. If there is not an externally applied oscillator to RTC_XTALI, the internal oscillator takes over.

- On-chip 32 kHz RC oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more I_{DD} than crystal oscillator
  - Approximately ±10% tolerance
  - No external component required
  - Starts up faster than 32 kHz crystal oscillator
  - Three configurations for this input:
    - External oscillator
    - External crystal coupled to RTC_XTALI and RTC_XTALO
    - Internal oscillator

External crystal oscillator with on-chip support circuit:

- At power up, RC oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
- Higher accuracy than RC oscillator
- If no external crystal is present, then the RC oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximum supply currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MC3xPF3000xxxx, NXP's power management IC targeted for the i.MX 7Solo family of processors, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

Table 12 represents the maximum momentary current transients on power lines, and should be used for power supply selection. Maximum currents are higher by far than the average power consumption of typical use cases. For typical power consumption information, see the application note, *i.MX 7DS Power Consumption Measurement* (AN5383).

Table 12. Maximum supply currents

Power Rail	Source	Conditions	Max Current	Unit
VDD_ARM	From PMIC	—	500	mA
VDD_SOC	From PMIC	—	1000	mA
VDDA_1P8_IN	From PMIC	—	150[1]	mA
VDD_SNVS_IN	From PMIC or Coin cell	—	1	mA
VDD_XTAL_1P8	From PMIC	—	5	mA
VDD_LPSR_IN	From PMIC	—	5	mA
VDD_TEMPSENSOR_1P8	From PMIC	—	1	mA
VDDA_ADC1_1P8	From PMIC	—	5	mA
VDDA_ADC2_1P8	From PMIC	—	5	mA
FUSE_FSOURCE	From PMIC	—	150	mA
VDD_MIPI_1P0	From i.MX 7 internal LDO	—	80	mA

Table 12. Maximum supply currents(continued)

Power Rail	Source	Conditions	Max Current	Unit
NVCC_GPIO1	From PMIC	N=12	Use max IO equation[2]	mA
NVCC_GPIO2	From PMIC	N=14		mA
NVCC_SD2	From PMIC	N=9		mA
NVCC_SD3	From PMIC	N=12		mA
NVCC_SD1	From PMIC	N=9		mA
NVCC_ENET1	From PMIC	N=16		mA
NVCC_EPDC1	From PMIC	N=16		mA
NVCC_EPDC2	From PMIC	N=17		mA
NVCC_SAI	From PMIC	N=11		mA
NVCC_LCD	From PMIC	N=29		mA
NVCC_SPI	From PMIC	N=8		mA
NVCC_ECSPI	From PMIC	N=8		mA
NVCC_I2C	From PMIC	N=8		mA
NVCC_UART	From PMIC	N=8		mA
VDD_USB_OTG1_3P3_IN	From PMIC	—	50	mA
VDD_USB_OTG2_3P3_IN	From PMIC	—	50	mA
VDD_USB_H_1P2	From i.MX 7 internal LDO	—	20	mA
VDDA_MIPI_1P8	From i.MX 7 internal LDO	—	5	mA
DRAM_VREF	From PMIC	—	30	mA
NVCC_DRAM_CKE	From PMIC	—	30	mA
NVCC_DRAM	From PMIC	—	—[3]	mA

1 The actual maximum current drawn from VDDA_1P8_IN is as shown plus any additional current drawn from the VDDD_1P0_CAP, VDD_1P2_CAP, VDDA_PHY_1P8 outputs, depending on actual application configuration (for example, VDD_MIPI_1P0, VDD_USB_H_1P2 and supplies).

2 General equation for estimated, maximal power consumption of an I/O power supply:

$$I_{max} = N \times C \times V \times (0.5 \times F)$$

where:

N = Number of I/O pins supplied by the power line
C = Equivalent external capacitive load
V = IO voltage
$(0.5 \times F)$ = Data change rate, up to 0.5 of the clock rate (F)
In this equation, I_{max} is in amps, C in farads, V in volts, and F in hertz.

3 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take into account factors such as signal termination. See the application note, *i.MX 7DS Power Consumption Measurement* (AN5383) for examples of DRAM power consumption during specific use case scenarios.

4.1.6 Power modes

The i.MX 7Solo has the following power modes:

- OFF mode: all power rails are off
- SNVS mode: only RTC and tamper detection logic is active
- LPSR mode: an extension of SNVS mode, with 16 GPIOs in low power state retention mode
- RUN Mode: all external power rails are on, CPU is active and running, other internal module can be on/off based on application;
- Low Power mode (System Idle, Low Power Idle, and Deep Sleep): most external power rails are still on, CPU is in WFI state or power gated, most of the internal modules are clock gated or power gated

The valid power mode transition is shown in this diagram.

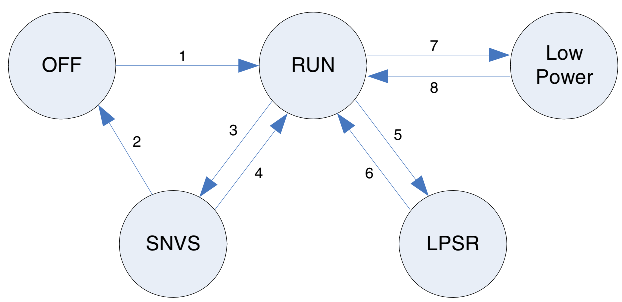


Figure 3. i.MX 7Solo Power Modes

The power mode transition condition is defined in the following table.

Table 13. Power Mode Transition

Transition	From	To	Condition
1	OFF	RUN	VDD_SVNS_IN supply present.
2	SNVS	OFF	VDD_SNVS_IN supply removal.
3	RUN	SNVS	ONOFF long press, or SW.
4	SNVS	RUN	ONOFF press, or RTC, or tamper event.
5	RUN	LPSR	SW.
6	LPSR	RUN	ONOFF press, or RTC, or tamper event, or GPIO event.
7	RUN	Low Power	SW (CPU execute WFI)
8	Low Power	RUN	RTC, tamper event, IRQ.

The following table summarizes the external power supply state in all the power modes.

Table 14. Power modes

Power rail	OFF	SVNS	LPSR	RUN	Low Power
VDD_ARM	OFF	OFF	OFF	ON	ON/ OFF
VDD_SOC	OFF	OFF	OFF	ON	ON
VDDA_1P8_IN	OFF	OFF	OFF	ON	ON
VDD_SNVS_IN	OFF	ON	ON	ON	ON
VDD_LPSR_IN	OFF	OFF	ON	ON	ON
NVCC_GPIO1/2	OFF	OFF	ON	ON	ON
NVCC_DRAM	OFF	OFF	OFF	ON	ON
NVCC_DRAM_CKE	OFF	OFF / ON	OFF / ON	ON	ON
NVCC_XXX	OFF	OFF	OFF	ON / OFF	ON / OFF
VDD_USB_OTG1_3P3_IN VDD_USB_OTG2_3P3_IN	OFF / ON	OFF / ON	OFF / ON	ON / OFF	ON / OFF

The NVCC_DRAM_CKE can be still ON during SNVS/LPSR mode to keep the CKE/RESET pad in correct state to hold DRAM device in self-refresh mode.

The NVCC_XXX can be off in RUN mode / Low Power mode if all the pads in that IO bank is not used in the application, the NVCC_XXX supply could be tied to GND.

The VDD_USB_OTG1_3P3_IN and VDD_USB_OTG2_3P3_IN are fully asynchronous to other power rails, so it can be either ON/OFF in any of the power modes.

4.1.6.1 OFF Mode

In OFF mode, all the power rails are shut off.

4.1.6.2 SNVS Mode

SNVS mode is also called RTC mode, where only the power for the SNVS domain remain on. In this mode, only the RTC and tamper detection logic is still active.

The power consumption in SNVS model with all the tamper detection logic enabled will be less than 5 uA @ 3.0 V on VDD_SNVS_IN for typical silicon at 25°C.

The external DRAM device can keep in self-refresh when the chip stays in SNVS mode with NVCC_DRAM_CKE still powered. During the state transition between SNVS mode to/from ON mode, the DRAM_CKE pad and DRAM_RESET pad has to always stay in correct state to keep DRAM in self-refresh mode. No glitch / floating is allowed.

4.1.6.3 LPSR Mode

LPSR is considered as an extension of the SNVS mode. All the features supported in SNVS mode is also supported in LPSR mode, including the capability of keeping DRAM device in self-refresh.

In LPSR mode, three additional power rails will remain on: VDD_LPSR_IN, NVCC_GPIO1, and NVCC_GPIO2. These three power rails are used to supply the logic and IO pads in the LPSR domain. The purpose of this mode is to retain the state of 16 GPIO pads, so the other components in the whole system will have their control signal in correct state.

Among all the 16 GPIO pads, the NVCC_GPIO1 supply the power for 8 GPIO pads, and the NVCC_GPIO2 supply the power for the other 8 GPIO pads. This allows the SoC to have some of its GPIO working at 1.8 V while others working at 3.3 V in the LPSR mode.

When LPSR mode is not needed for the application, the VDD_LPSR can be connected to VDDA_1P8 and NVCC_GPIO1/2 can be connected to the same power supply as NVCC_XXX for other GPIO banks.

In LPSR mode, the supported wakeup source are RTC alarm, ONOFF event, security/tamper and also the 16 GPIO pads.

4.1.6.4 RUN Mode

In RUN mode, the CPU is active and running, and the analog / digital peripheral modules inside the processor will be enabled. In this mode, all the external power rails to the processor have to be ON and the SoC will be able to draw as many current as listed in the Table 5 Maximum Power Requirement.

In this mode, the PMIC should allow SoC to change the voltage of power rails through I2C/SPI interface. Typically, when the CPU is doing DVFS, it switches the VDD_ARM voltage according to Table 9.

4.1.6.5 Low Power Mode

When the CPU is not running, the processor can enter low power mode. i.MX 7Dual processor supports a very flexible set of power mode configurations in low power mode.

Typically there are 3 low power modes used, System IDLE, Low Power IDLE and SUSPEND:

- System IDLE—This is a mode that the CPU can automatically enter when there is no thread running. All the peripherals can keep working and the CPU’s state is retained so the interrupt response can be very short. The cores are able to individually enter the WAIT state.
- Low Power IDLE—This mode is for the case when the system needs to have lower power but still keep some of the peripherals alive. Most of the peripherals, analog modules, and PHYs are shut off; see Table 5-5, “Low Power Mode Definition,” in the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) for details. The interrupt response in this mode is expected to be longer than the System IDLE, but its power is much lower.
- Suspend—This mode has the greatest power savings; all clocks, unused analog/PHYs, and peripherals are off. The external DRAM stays in Self-Refresh mode. The exit time from this mode is much longer.

In System IDLE and Low Power IDLE mode, the voltage on external power supplies remains the same as in RUN mode, so the external PMIC is not aware of the state of the processor. If any low-power setting needs to be applied to PMIC, it is done through the I2C/SPI interface before the processor enters a low-power mode.

When the processor enters SUSPEND mode, it will assert the PMIC_STBY_REQ signal to PMIC. When this signal is asserted, the processor allows the PMIC to shut off VDD_ARM externally. However, in some application scenario, SW want to keep the data in L2 Cache to avoid performance impact on cache miss. In this case, the VDD_ARM cannot be shut off. To support both scenarios, the PMIC should have an option to shut off or keep VDD_ARM when it receives the PMIC_STBY_REQ. This should be configured through I2C/SPI interface before the processor enters SUSPEND mode.

Except the VDD_ARM, the other power rails have to keep active in SUSPEND mode. Since the current on each power rail is greatly reduced in this mode, PMIC can enter its own low power mode to get extra power saving. For example, the PMIC can change the DCDC rails to PFM mode to reduce the power consumption.

The power consumption in low power modes is defined in Table 15.

Table 15. Low Power Measurements

Power rail	System IDLE			Low Power IDLE			SUSPEND			LPSR		
	Voltage	Current	Power	Voltage	Current	Power	Voltage	Current	Power	Voltage	Current	Power
	(V)	(mA)	(mW)	(V)	(mA)	(mW)	(V)	(mA)	(mW)	(V)	(mA)	(mW)
VDD_ARM	1.0	2.7	2.70	1.0	0.428	0.43	1.0	0.3	0.30	0.0	—	0.00
VDD_SOC	1.0	19.38	19.38	1.0	1.423	1.42	1.0	0.6	0.60	0.0	—	0.00
VDDA_1P8_IN	1.8	3.46	6.23	1.8	0.206	0.37	1.8	0.4	0.72	0.0	—	0.00
VDD_SNVS_IN	3.0	0.006	0.018	3.0	0.005	0.015	3.0	0.006	0.018	3.0	0.003	0.009
VDD_LPSR_IN	1.8	0.04	0.07	1.8	0.041	0.07	1.8	0.039	0.0702	1.8	0.04	0.07
NVCC_GPIO1/2	1.8	0.072	0.13	1.8	0.073	0.13	1.8	0.072	0.13	1.8	0.072	0.13
Total	—	—	**28.53**	—	—	**2.45**	—	—	**1.84**	—	—	**0.21**

All the power numbers defined in Table 15 are based on typical silicon at 25°C.

4.1.7 USB PHY Suspend current consumption

4.1.7.1 Low Power Suspend Mode

The VBUS Valid comparators and their associated bandgap circuits are enabled by default. Table 16 shows the USB interface current consumption in Suspend mode with default settings.

Table 16. USB PHY current consumption with default settings[1]

	VDD_USB_OTG1_3P3_IN	VDD_USB_OTG2_3P3_IN
Current	790 uA	790 uA

1 Low Power Suspend is enabled by setting USBx_PORTSC1 [PHCD]=1 [Clock Disable (PLPSCD)].

4.1.7.2 4.1.7.2 Power-Down modes

Table 17 shows the USB interface current consumption with only the OTG block powered down.

Table 17. USB PHY current consumption with VBUS Valid Comparators disabled[1]

	VDD_USB_OTG1_3P3_IN	VDD_USB_OTG2_3P3_IN
Current	730 uA	730 uA

1 VBUS Valid comparators can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1. This signal powers down only the VBUS Valid comparator, and does not control power to the Session Valid Comparator, ADP Probe and Sense comparators, or the ID detection circuitry.

In Power-Down mode, everything is powered down, including the USB_VBUS valid comparators and their associated bandgap circuity in typical condition. Table 18 shows the USB interface current consumption in Power-Down mode.

Table 18. USB PHY current consumption in Power-Down mode[1]

	VDD_USB_OTG1_3P3_IN	VDD_USB_OTG2_3P3_IN
Current	200 uA	200 uA

1 The VBUS Valid Comparators and their associated bandgap circuits can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1 and USBNC_OTG*_PHY_CFG2[DRVVBUS0] to 0, respectively.

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.1.8 Power-up sequence

The i.MX7 processor has the following power-up sequence requirements:

- VDD_SNVS_IN to be turned on before any other power supply. If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- VDD_SOC to be turned on before NVCC_DRAM and NVCC_DRAM_CKE.
- VDD_ARM, VDD_SOC, VDDA_1P8_IN, VDD_LPSR_IN and all I/O power (NVCC_*) should be turned on after VDD_SVNS_IN is active. But there is no sequence requirement among these power rails other than the sequence requirement between VDD_SOC and NVCC_DRAM/NVCC_DRAM_CKE.
- There are no special timing requirements for VDD_USB_OTG1_3P3_IN and VDD_USB_OTG2_3P3_IN.

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control.

The power-up sequence is shown in Figure 4 with the following timing parameters:

T1 Time from SVNS power stable to other power rails start to ramp, minimal delay is 2ms, no max delay requirement.

T2 Time from first power rails (except SNVS) ramp up to all the power rails get stable, minimal delay is 0ms, no max delay requirement.

T3 Time from all power rails get stable to power-on reset, minimal delay is 0ms, no max delay requirement.

T6 Time from VDD_SOC get stable to NVCC_DRAM/NVCC_DRAM_CKE start to ramp, minimal delay is 0ms, no max delay requirement.

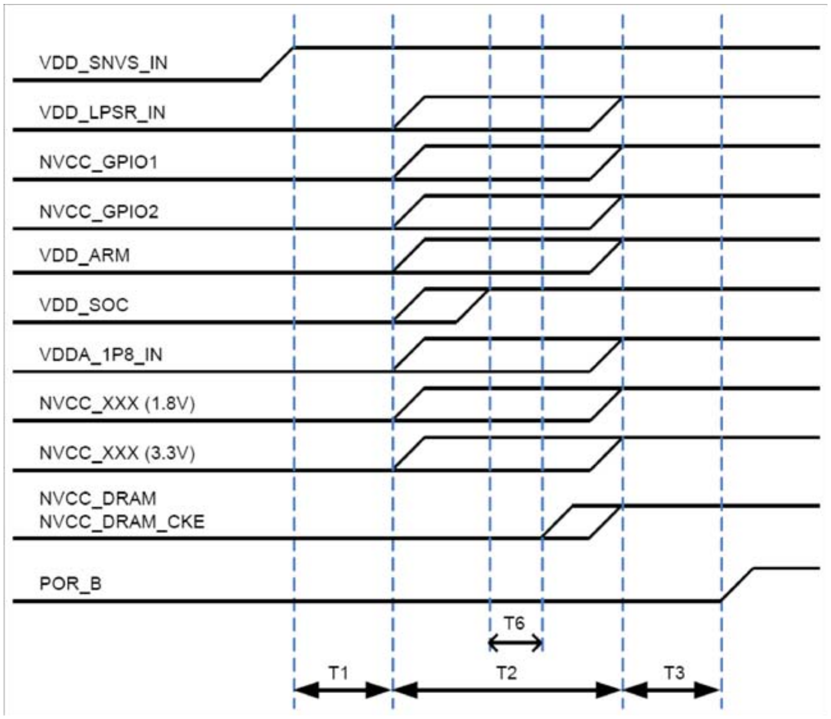


Figure 4. i.MX 7Solo power-up sequence

4.1.9 Power-down sequence

The i.MX7 processors have the following power-down sequence requirements:

- VDD_SNVS _IN to be turned off last after any other power supply.
- NVCC_DRAM/NVCC_DRAM_CKE to be turned off before VDD_SOC.
- There are no special timing requirements forVDD_USB_OTG1_3P3_IN andVDD_USB_OTG2_3P3_IN.

The power-down sequence is shown in Figure 5 with the following timing parameters:

T4 Time from first power rails (except SNVS) to ramp down to all the power rails (except SNVS) get to ground, minimal delay is 0ms, no max delay requirement.

T5 Time from all the power rails power down (except SNVS) to SVNS power down, minimal delay is 0ms, no max delay requirement.

T7 Time from NVCC_DRAM/NVCC_DRAM_CKE power down to VDD_SOC power down, minimal delay is 0ms, no max delay requirement.

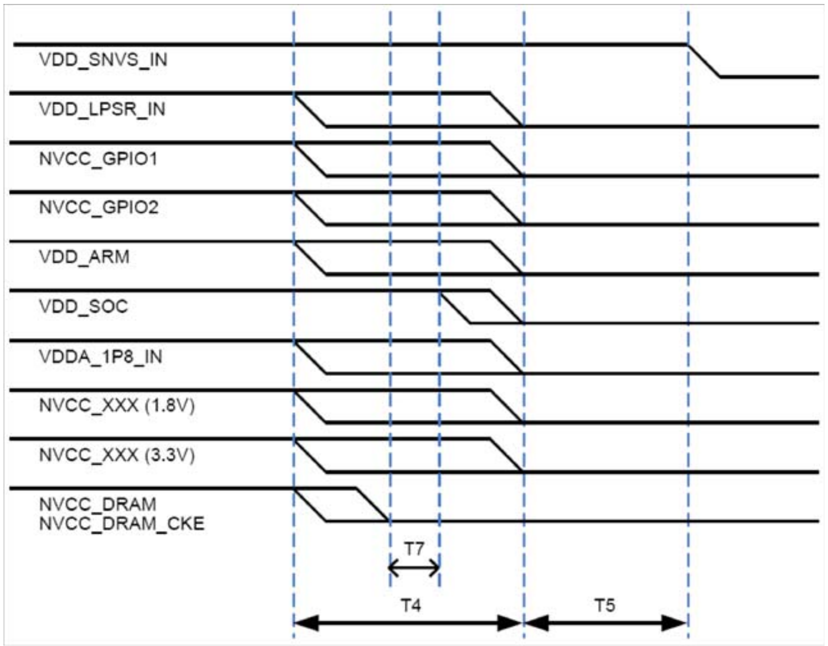


Figure 5. i.MX 7Solo power-down sequence

4.1.10 Power supplies usage

I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package information and contact assignments.”

4.2 Integrated LDO voltage regulator parameters

Various internal supplies can be powered from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) for details on the power tree scheme.

NOTE

The *_CAP signals must not be powered externally. The *_CAP pins are for the bypass capacitor connection only.

4.2.1 Internal regulators

Table 19. LDO parameters

Parameter	Min	Max	Units
PVCC_GPIO_AT3P3_1P8	1.6	1.98	V
VDD_1P2	1.1	1.32	V
LPSR_1P0	0.95	1.155	V
VDDA_PHY_1P8	1.6	1.98	V
USB_OTG1_1P0	0.95	1.155	V

4.2.1.1 LDO_1P2

The LDO_1P2 regulator implements a programmable linear-regulator function from VDDA_1P8_IN (see Table 9 for minimum and maximum input requirements). The typical output of the LDO, VDD_1P2_CAP, is 1.2 V. It is intended for use with the USB HSIC PHY, which uses this voltage level for its output driver. For additional information, see the “Power Management Unit (PMU)” chapter of the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

4.2.1.2 LDO_1P0D

The LDO_1P0D regulator implements a programmable linear-regulator function from VDDA_1P8_IN (see Table 9 for minimum and maximum input requirements). The typical output of the LDO, VDD_1P0D_CAP, is 1.0 V. It is intended for use with the internal physical interfaces, including MIPI. For additional information, see the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

4.2.1.3 LDO_1P0A

The LDO_1P0A regulator implements a programmable linear-regulator function from VDDA_1P8_IN (see Table 9 for minimum and maximum input requirements). The typical output of the LDO, VDD_1P0A_CAP, is 1.0 V. It is intended for use with the internal analog modules, including the XTAL, ADC, PLL, and Temperature Sensor. For additional information, see the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

4.2.1.4 LDO_USB1_1PO/LDO_USB2_1P0

The LDO_USB1_1P0/LDO_USB2_1P0 regulators implement a fixed linear-regulator function from VDD_USB_OTG1_3P3_IN and VDD_USB_OTG2_3P3_IN power inputs respectively (see Table 9 for minimum and maximum input requirements). The typical output voltage is 1.0 V. It is intended for use with the internal USB physical interfaces (USB PHY1 and USB PHY2). For additional information, see the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

4.2.1.5 LDO_SVNS_1P8

1.8 V LDO from coin cell to generate 1.8 V power for SNVS and 32 K RTC. The LDO_SNVS_1P8 regulator implements a fixed linear-regulator function from VDD_SNVS_IN (see Table 9 for minimum and maximum input requirements). The typical output is 1.7 V. It is intended for use with the internal SNVS circuitry. For additional information, see the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

4.3 PLL electrical characteristics

Table 20. PLL Electrical Parameters

PLL type	Parameter	Value
AUDIO_PLL	Clock output range	650 MHz–1.3 GHz
	Reference clock	24 MHz
	Lock time	<11250 reference cycles
VIDEO_PLL	Clock output range	650 MHz–1.3 GHz
	Reference clock	24 MHz
	Lock time	<383 reference cycles
SYS_PLL	Clock output range	480 MHz
	Reference clock	24 MHz
	Lock time	<383 reference cycles
ENET_PLL	Clock output range	650 MHz–1.3 GHz, set to 1.0 GHz
	Reference clock	24 MHz
	Lock time	<11250 reference cycles
ARM_PLL	Clock output range	800 MHz–1.2 GHz
	Reference clock	24 MHz
	Lock time	<2250 reference cycles
DRAM_PLL	Clock output range	800 MHz–1066 MHz
	Reference clock	24 MHz
	Lock time	>2250 reference cycles

4.4 On-chip oscillators

4.4.1 OSC24M

Power for the oscillator is supplied from a clean source of VDDA_1P8. This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from VDDA_1P8.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.4.2 OSC32K

This block implements an internal amplifier, trimable load capacitors and a resistor that when combined with a suitable quartz crystal implements a low power oscillator.

In addition, if the clock monitor determines that the OSC32K is not present then the source of the 32 kHz clock will automatically switch to the internal relaxation oscillator of lesser frequency accuracy.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_1p8_CAP, which is regulated from VDD_SNVS. The target battery is an ~3 V coin cell for VDD_SNVS and the regulated output is ~1.75V.

Table 21. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Fosc	—	32.768 KHz	—	This frequency is nominal and determined by the crystal selected. 32.0 K would work as well.
Current consumption	—	350 nA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the interrelaxation oscillator is used instead of an external crystal then approximately 250 nA should be added to this value.
Bias resistor	—	200 MΩ		This is the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually, crystals can be purchased tuned for different Cload. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin but increases current oscillating through the crystal. The Cload is programmable in 2 pF steps.
ESR	—	50 KΩ	—	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease oscillating margin.

4.5 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR3 and DDR3 modes
- Differential I/O (CCM_CLK1)

4.5.1 General purpose I/O (GPIO) DC parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 22. GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage	V_{OH}	I_{OH}= –1.8mA, –3.6mA, –7.2mA, –10.8mA	0.8 × OVDD	OVDD	V
Low-level output voltage	V_{OL}	I_{OL}=1.8mA, 3.6mA, 7.2mA, 10.8mA	0	0.2 × OVDD	V
High-level input voltage	V_{IH}	—	0.7 × OVDD	OVDD + 0.3	V
Low-level input voltage	V_{IL}	—	–0.3	0.3 × OVDD	V
Input hysteresis	V_{HYS}	—	0.15	—	V
Pull-up resistor (5_kΩ PU)	—	V_{DD} = 1.8 ± 0.15 V	5.94	5.98	KΩ
Pull-up resistor (5_kΩ PU)	—	V_{DD} = 3.3 ± 0.3 V	4.8	5.3	KΩ
Pull-up resistor (47_kΩ PU)	—	V_{DD} = 1.8 ± 0.15 V	46.1	50.6	KΩ
Pull-up resistor (47_kΩ PU)	—	V_{DD} = 3.3 ± 0.3 V	45.8	49.8	KΩ
Pull-up resistor (100_kΩ PU)	—	V_{DD} = 1.8 ± 0.15 V	97.5	105.9	KΩ
Pull-up resistor (100_kΩ PU)	—	V_{DD} = 3.3 ± 0.3 V	101	105	KΩ
Pull-down resistor (100_kΩ PU)	—	V_{DD} = 1.8 ± 0.15 V	101	108.6	KΩ
Pull-down resistor (100_kΩ PD)	—	V_{DD} = 3.3 ± 0.3 V	101	108	KΩ
Input current (no PU/PD)	I_{OZ}	—	–5	5	µA
Sink/source current in Push-Pull mode	—	Driving currents (@100MHz, V_{OL}/H = 0.5×OV_{DD}, SS, 125°C) OV_{DD} = 2.7 V	–32.9	32.9	mA

4.5.2 DDR I/O DC electrical characteristics

The DDR I/O pads support DDR3/DDR3L, LPDDR2, and LPDDR3 operational modes. The DDR Memory Controller (DDRMC) is designed to be compatible with JEDEC-compliant SDRAMs. The DDRC supports the following memory types:

- DDR3 SDRAM compliant to JESD79-3E DDR3 JEDEC standard release July, 2010
- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- LPDDR3 SDRAM compliant to JESD209-3B LPDDR3 JEDEC standard release August, 2013

DDRMC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 7 application processor.

Table 23. DC input logic level

Characteristics	Symbol	Min	Max	Unit
DC input logic high[1]	$V_{IH(DC)}$	V_{REF} +100	—	mV
DC input logic low[1]	$V_{IL(DC)}$	—	V_{REF} –100	

1 It is the relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device that determines noise margins. However, in the case of V_{IH}(DC) max (that is, input overdrive), it is the V_{DDQ} of the receiving device that is referenced.

Table 24. Output DC current drive

Characteristics	Symbol	Min	Max	Unit
Output minimum source DC current[1]	I_{OH}(DC)	–4	—	mA
Output minimum sink DC current[1]	I_{OL}(DC)	4	—	mA
DC output high voltage(I_{OH} = –0.1mA)[1,2]	V_{OH}	0.9 × V_{DDQ}	—	V
DC output low voltage(I_{OL} = 0.1mA)[1,2]	V_{OL}	—	0.1 × V_{DDQ}	V

1 When DDS=[111] and without ZQ calibration.

2 The values of V_{OH} and V_{OL} are valid only for 1.2 V range.

Table 25. Input DC current

Characteristics	Symbol	Min	Max	Unit
High level input current[1,2]	I_{IH}	–25	25	µA
Low level input current[1,2]	I_{IL}	–25	25	µA

1 The values of V_{OH} and V_{OL} are valid only for 1.2 V range.

2 Driver Hi-Z and input power-down (PD=High)

4.5.2.1 LPDDR3 mode I/O DC parameters

Table 26. LPDDR3 I/O DC electrical parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA	0.9 × OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1mA	—	0.1 × OVDD	V
Input Reference Voltage	Vref	—	0.49 × OVDD	0.51 × OVDD	V

Table 26. LPDDR3 I/O DC electrical parameters(continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
DC High-Level input voltage	Vih_DC	—	VRef + 0.100	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	VRef – 0.100	V
Differential Input Logic High	Vih_diff	—	0.26	See note[1]	—
Differential Input Logic Low	Vil_diff	—	See note[1]	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	–15	15	%
240 ?unit calibration resolution	Rres	—	—	10	?
Keeper Circuit Resistance	Rkeep	—	110	175	k?
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	µA

[1] The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.5.3 Differential I/O port (CCM_CLK1P/N)

The clock I/O interface is designed to be compatible with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001), for details.

Table 27 shows the clock I/O DC parameters.

Table 27. Differential clock I/O DC electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Vod	Output Differential Voltage	Rload=100 Ω between padp and padn	250	350	450	mV	Vpadp–Vpadn
Voh	High-level output voltage		1.025	1.175	1.325	V	[1]
Vol	Low-level output voltage		0.675	0.825	0.975		[2]
Vocm	Output common mode voltage		0.9	1	1.1		Core supply is used
Vid	Input Differential Voltage		100		600	mV	Vpadp–Vpadn
Vicm	Input common mode voltage		50m		1.57	V	Vicm(max)=ovdd(min)–Vid(min)/2
Icc-ovdd	Tri-state I/O supply current	ipp_ibe=ipp_obe=0 irefin disabled (0uA)			0.46	uA	

Table 27. Differential clock I/O DC electrical characteristics(continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Icc-ovdd-lp	Tri-state I/O supply current in low-power mode	ipp_pwr_stable_b_1p8 =1 (means 1.8 V) vddi is OFF irefin disabled (0 uA)		0.35	1	uA	
Icc-vddi	Tri-state core supply current	ipp_ibe=ipp_obe=0 irefin disabled (0 uA)			0.8		
Icc	Power supply current (ovdd)	Rload=100 Ω between padp and padn			4.7	mA	This is not including current through external Rload=100 Ω

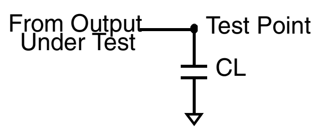
[1] VOH_max = Vos_max + Vod_max/2 = 1.1+0.225 = 1.325 V. VOH_min = Vos_min + Vod_min/2 = 0.9+0.125 = 1.025 V.
[2] VOL_max = Vos_max - Vod_min/2 = 1.1-0.125 = 0.975 V. VOL_min = Vos_min - Vod_max/2 = 0.9 - 0.225 = 0.675 V

4.6 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, LPDDR3 and DDR3/DDR3L modes
- Differential I/O (CCM_CLK1)

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 6 and Figure 7.



CL includes package, probe and fixture capacitance

Figure 6. Load circuit for output

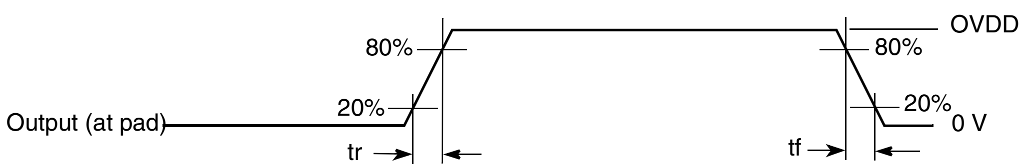


Figure 7. Output transition time waveform

4.6.1 General purpose I/O AC parameters

This section presents the I/O AC parameters for GPIO in different modes. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 28. Maximum input cell delay time

Cell name	Max Delay PAD → Y (ns)		
	VDD=1.65 V T=125°C Process=Slow	VDD=2.3 V T=125°C Process=Slow	VDD=3.0 V T=125°C Process=Slow
PBIDIRPUD_E33_33_NT_DR	0.9	1.5	1.4

Table 29. Output cell delay time for fixed load

Parameter				Simulated Cell Delay A → PAD (ns)								
				VDD = 1.65 V, T = 125°C			VDD = 2.3 V, T = 125°C			VDD = 3.0 V, T = 125°C		
DS0	DS1	SR	Driver Type	CL= 5 pF	CL= 10 pF	CL= 40 pF	CL= 5 pF	CL= 10 pF	CL= 40 pF	CL= 5 pF	CL= 10 pF	CL= 40 pF
0	0	1	1× Slow Slew	4.9	6.0	12.5	4.8	6.1	11.9	5.4	6.7	14.6
0	0	0	1× Fast Slew	3.8	4.7	11.2	3.8	5.1	12.8	4.2	5.3	13.5
0	1	1	2× Slow Slew	4.1	4.8	8.2	4.2	4.9	8.8	4.5	5.3	9.1
0	1	0	2× Fast Slew	2.8	3.3	6.4	2.9	3.4	7.2	3.1	3.7	7.2
1	0	1	4× Slow Slew	3.6	4.1	6.0	3.7	4.1	6.4	3.9	4.4	6.6
1	0	0	4× Fast Slew	2.2	2.5	4.1	2.3	2.6	4.6	2.4	2.8	4.8
1	1	1	6× Slow Slew	3.6	4.0	5.5	3.6	4.0	5.9	3.8	4.3	6.2
1	1	0	6× Fast Slew	2.0	2.3	3.4	2.1	2.3	3.8	2.2	2.5	3.9

Table 30. Maximum frequency of operation for input

Maximum frequency (MHz)		
VDD = 1.8 V, CL = 50 fF	VDD=2.5 V, CL =5 0 fF	VDD = 3.3 V, CL = 50 fF
550	400	430

Table 31. Maximum frequency of operation for output[1]

Parameter				Maximum frequency (MHz)								
				VDD = 1.8 V			VDD = 2.5 V			VDD = 3.3 V		
DS0	DS1	SR	Driver Type	CL= 5 pF	CL= 10 pF	CL= 40 pF	CL= 5 pF	CL= 10 pF	CL= 40 pF	CL= 5 pF	CL= 10 pF	CL= 40 pF
0	0	1	1× Slow Slew	100	70	25	90	60	20	95	60	20
0	0	0	1× Fast Slew	110	75	25	100	65	20	100	65	20
0	1	1	2× Slow Slew	120	100	50	120	100	40	115	95	40
0	1	0	2× Fast Slew	185	145	50	180	130	40	170	130	40
1	0	1	4× Slow Slew	140	125	85	135	120	70	130	115	70
1	0	0	4× Fast Slew	235	200	100	225	195	80	215	185	80
1	1	1	6× Slow Slew	140	125	90	135	120	85	130	115	80
1	1	0	6× Fast Slew	250	225	140	240	215	120	235	205	120

[1] Maximum frequency value is obtained with lumped capacitor load. If you consider transmission line or SSN noise effect, it could be worse than suggested value.

4.6.2 Clock I/O AC parameters—CCM_CLK1_N/CCM_CLK1_P

The differential output transition time waveform is shown in Figure 8.

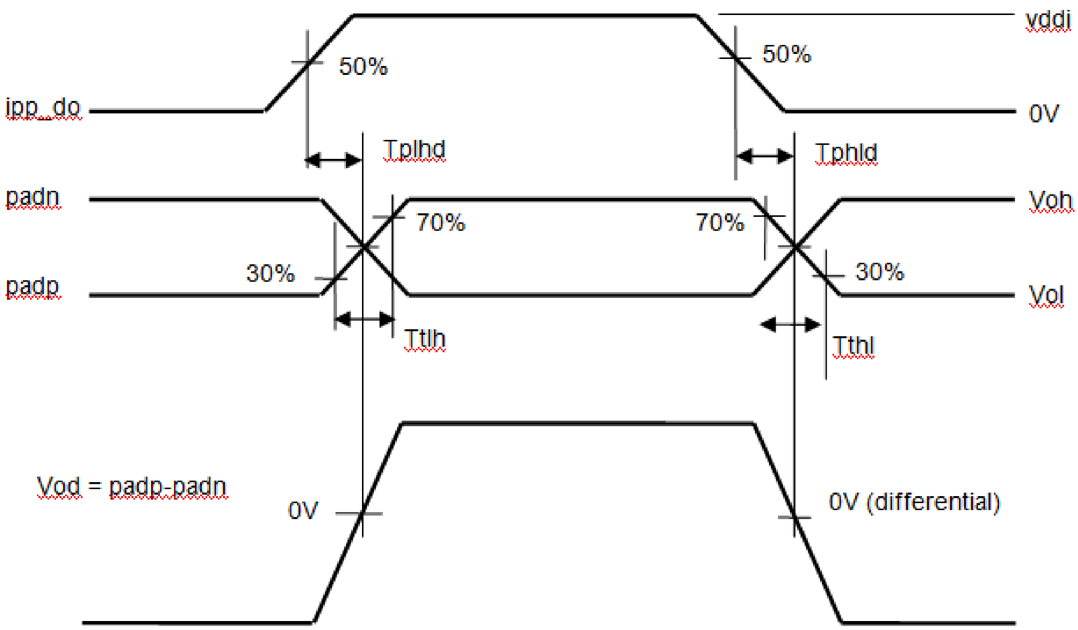


Figure 8. Differential LVDS driver transition time waveform

Table 32 shows the AC parameters for clock I/O.

Table 32. I/O AC Parameters of LVDS Pad

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Tphld	Output Differential propagation delay high to low	Rload=100 Ω between padp and padn, Cload = 2pF	—	—	0.61	ns	1
Tplhd	Output Differential propagation delay low to high		—	—	0.61		
Ttlh	Output Transition time low to high		—	—	0.17		2
Tthl	Output Transition time high to low		—	—	0.17		
Tphlr	Input Differential propagation delay high to low	Rload=100 Ω between padp and padn, Cload on ipp_ind=0.1 pF	—	—	0.33	ns	3
Tplhr	Input Differential propagation delay low to high		—	—	0.33		
Ttx	Transmitter startup time (ipp-obe low to high)	—	—	—	40	ns	4
F	Operating frequency	—	—	500	1000	MHz	—

1 At WCS, 125C, 1.62 V ovdd, 0.9 V vddi. Measurement levels are 50-50%. Output differential signal measured.

2 WCS, 125C, 1.62 V ovdd, 0.9 V vddi. Measurement levels are 20-80%. Output differential signal measured

3 At WCS, 125C, 1.62 V ovdd, 0.9 V vddi. Measurement levels are 50-50%.

4 TX startup time is defined as the time taken by transmitter for settling after its ipp_obe has been asserted. It is to stabilize the current reference. Functionality is guaranteed only after the startup time

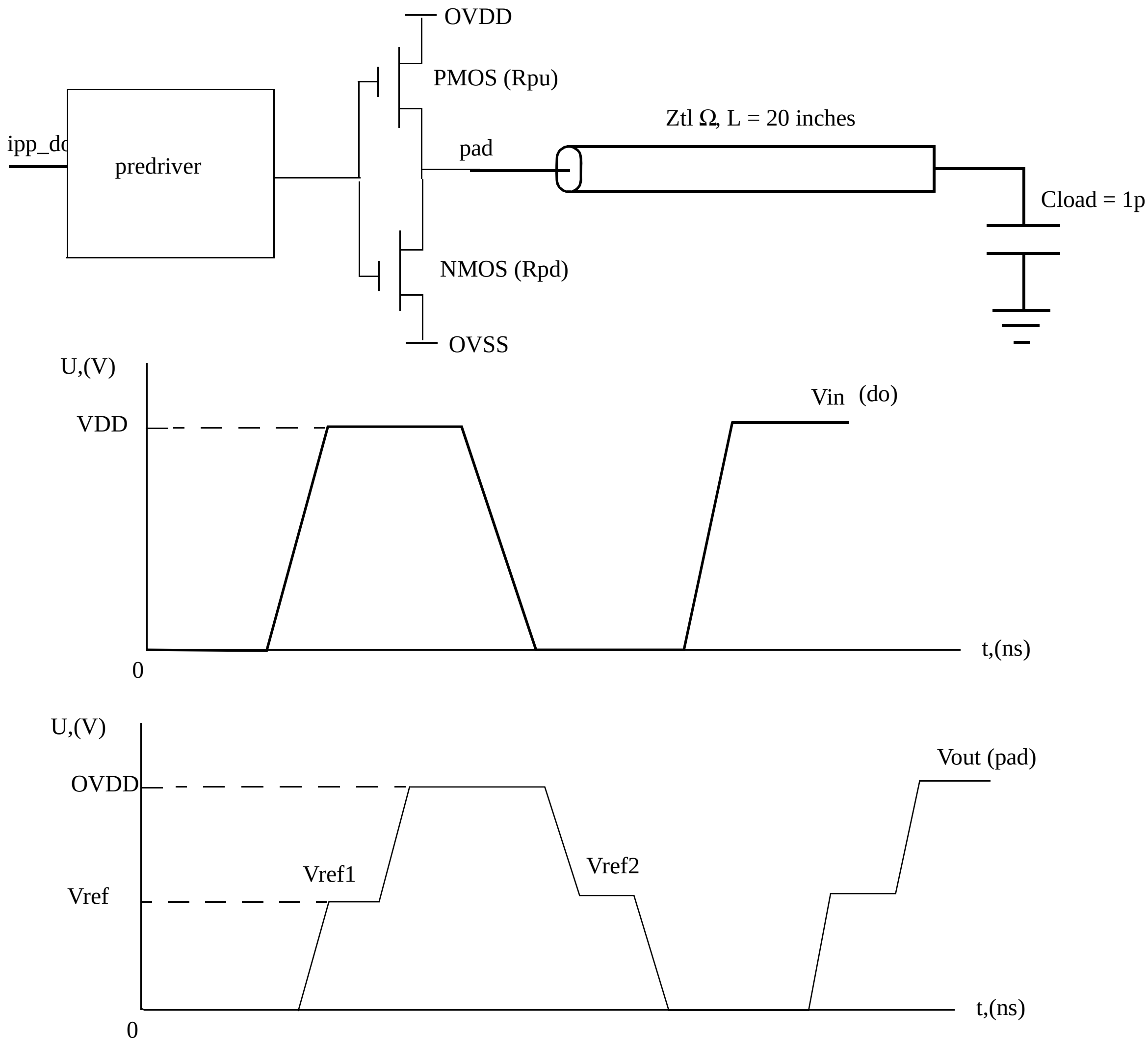
4.7 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 7Solo family of processors for the following I/O types:

- Double Data Rate I/O (DDR) for LPDDR2, LPDDR3, and DDR3/DDR3L modes
- Differential I/O (CCM_CLK1)
- USB battery charger detection open-drain output (USB_OTG1_CHD_B)

NOTE

DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 9).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 9. Impedance matching load for measurement

4.7.1 DDR I/O output buffer impedance

The LPDDR2 interface is designed to be fully compatible with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The LPDDR3 interface mode is designed to be compatible with JESD209-3B JEDEC standard released August, 2013. The DDR3 interface is designed to be fully compatible with JESD79-3F DDR3 JEDEC standard release July, 2012.

Table 33 shows DDR I/O output buffer impedance of i.MX 7Solo family of processors.

Table 33. DDR I/O output buffer impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.7.2 Differential I/O output buffer impedance

The Differential CCM interface is designed to be compatible with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001) for details.

4.7.3 USB battery charger detection driver impedance

The USB_OTG1_CHD_B open-drain output pin can be used to signal the results of USB Battery Charger detection routines for the USB_OTG1 PHY instance to power management and monitoring devices. Use of this pin requires an external pullup resistor, for more information see Table 3, and Table 7.

Table 34 shows the USB_OTG1_CHD_B pulldown driver impedance for the USB_OTG1_CHD_B pin.

Table 34. USB_OTG1_CHD_B pulldown driver impedance (VDD_USB_OTG1_3P3_IN 3.3 V)

Parameter	Symbol	Typical	Unit
Open-drain output driver pulldown impedance	Rdrv_pd	1000	Ω

4.8 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 7Solo processor.

4.8.1 Reset timings parameters

Figure 10 shows the reset timing and Table 35 lists the timing parameters.

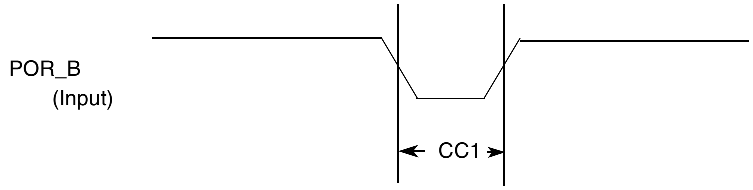


Figure 10. Reset timing diagram

Table 35. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid. **Note:** POR_B rise/fall times must be 5 ns or less.	1	—	RTC_XTALI cycle

4.8.2 WDOG Reset timing parameters

Figure 11 shows the WDOG reset timing and Table 36 lists the timing parameters.

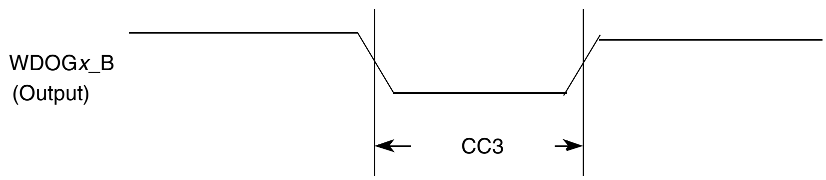


Figure 11. WDOG*x*_B timing diagram

Table 36. WDOG*x*_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG*x*_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) for detailed information.

4.8.3 External interface module (EIM)

The following subsections provide information on the EIM.

4.8.3.1 EIM interface pads allocation

EIM supports 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 37 provides EIM interface pads allocation in different modes.

Table 37. EIM internal module multiplexing[1]

Setup	Non Multiplexed Address/Data Mode			Multiplexed Address/ Data Mode
	8 Bit		16 Bit	16 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 001	MUM = 1, DSZ = 001
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	EIM_DATA [15:08]	EIM_AD [15:08]

1 For more information on configuration ports mentioned in this table, see the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

4.8.3.2 General EIM Timing—Synchronous mode

Figure 12, Figure 13, and Table 38 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

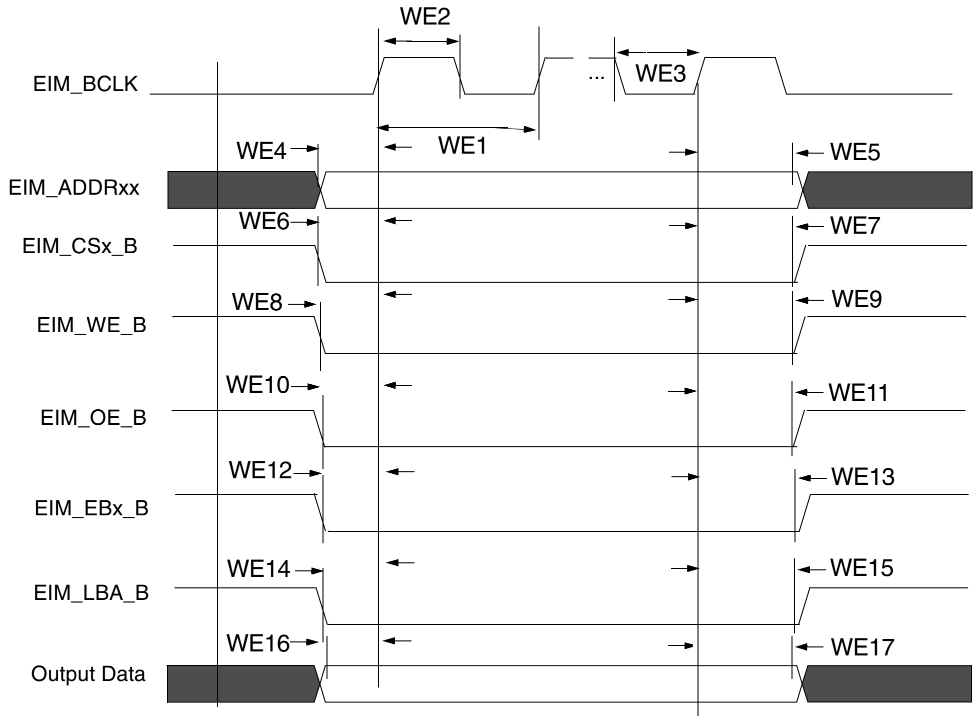


Figure 12. EIM outputs timing diagram

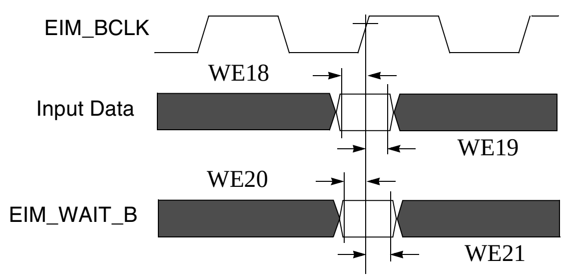


Figure 13. EIM inputs timing diagram

4.8.3.3 Examples of EIM synchronous accesses

Table 38. EIM bus timing parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2 x t	—	3 x t	—	4 x t	—
WE2	EIM_BCLK Low Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE3	EIM_BCLK High Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to EIM_CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to EIM_WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to EIM_OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to EIM_EBx_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to EIM_LBA_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	EIM_WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	EIM_WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

[1] t is the maximum EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed EIM_BCLK frequency is:

—Fixed latency for both read and write is 132 MHz.

—Variable latency for read only is 132 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz. Write BCD = 1 and 104 MHz axi_clk, will result in a EIM_BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

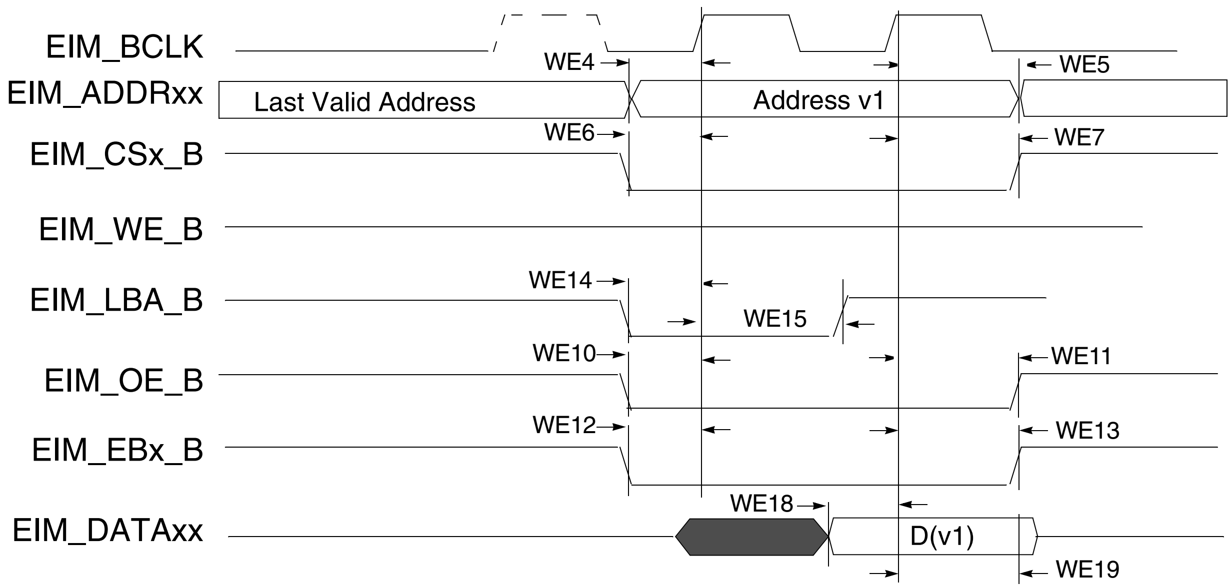


Figure 14. Synchronous memory read access, WSC=1

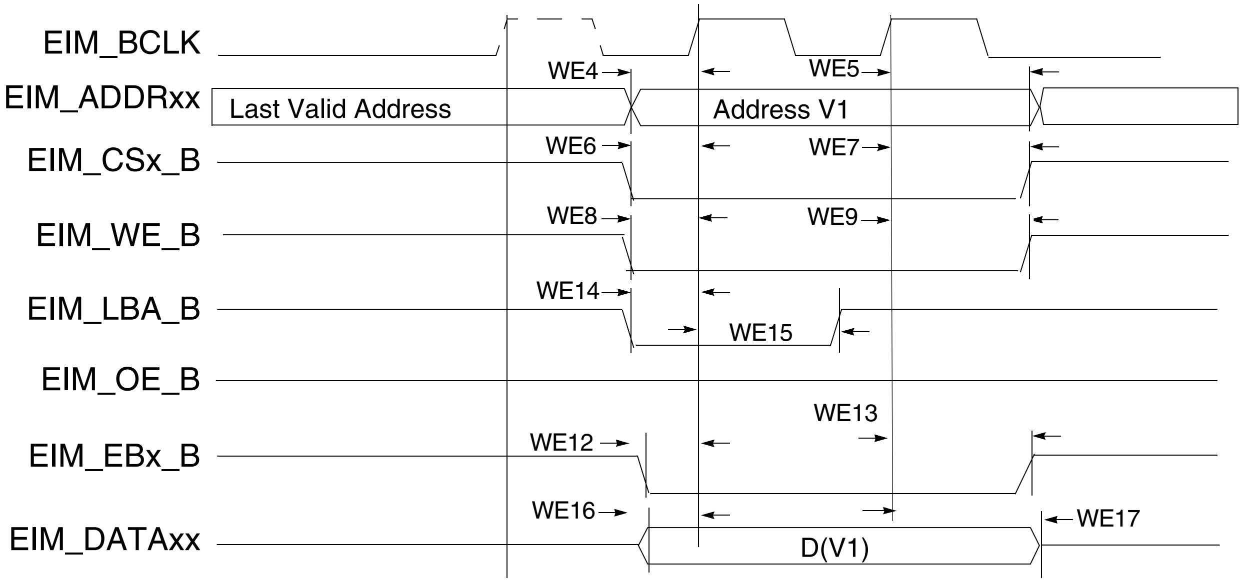


Figure 15. Synchronous memory, write access, WSC=1, WBEA=0 and WADVN=0

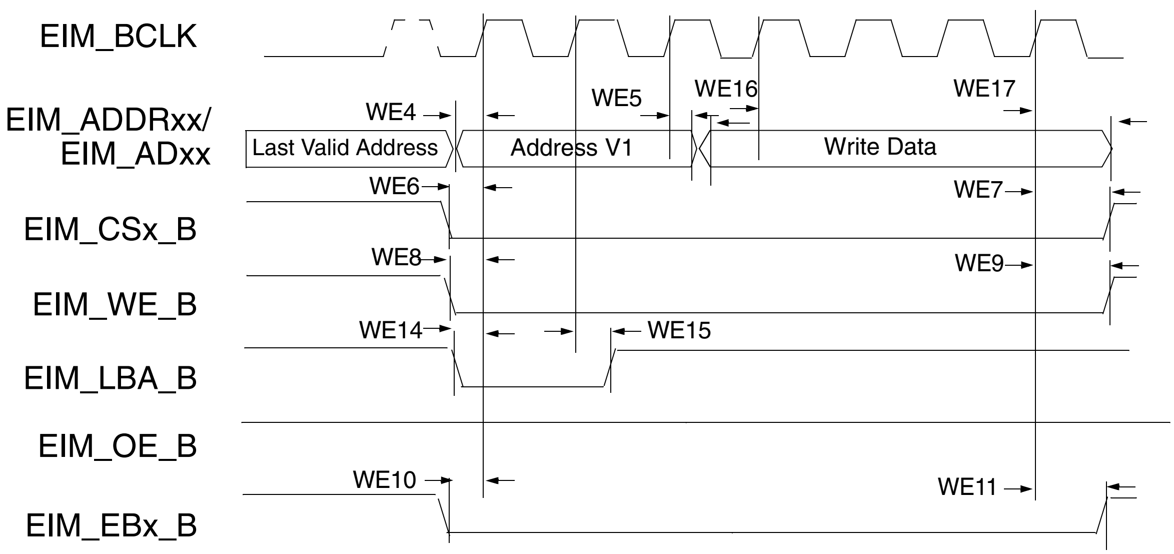


Figure 16. Muxed Address/Data (A/D) mode, synchronous write access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit Muxed Address/Data (A/D) mode the 16 MSBs are driven on the data bus.

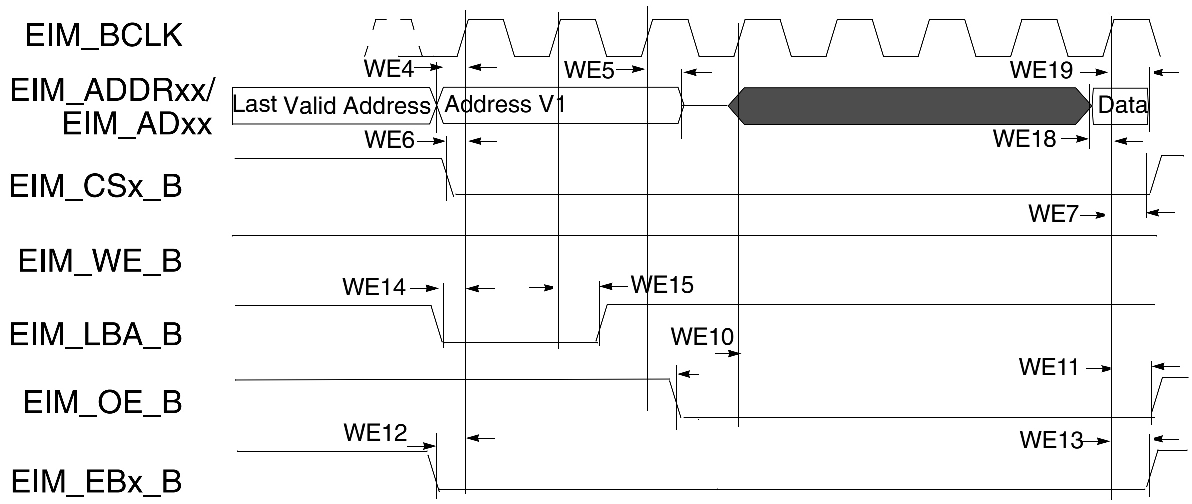


Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.8.3.4 General EIM timing—Asynchronous mode

Figure 18 through Figure 22, and Table 39 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN and CSN is configured differently. See the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) for the EIM programming model.

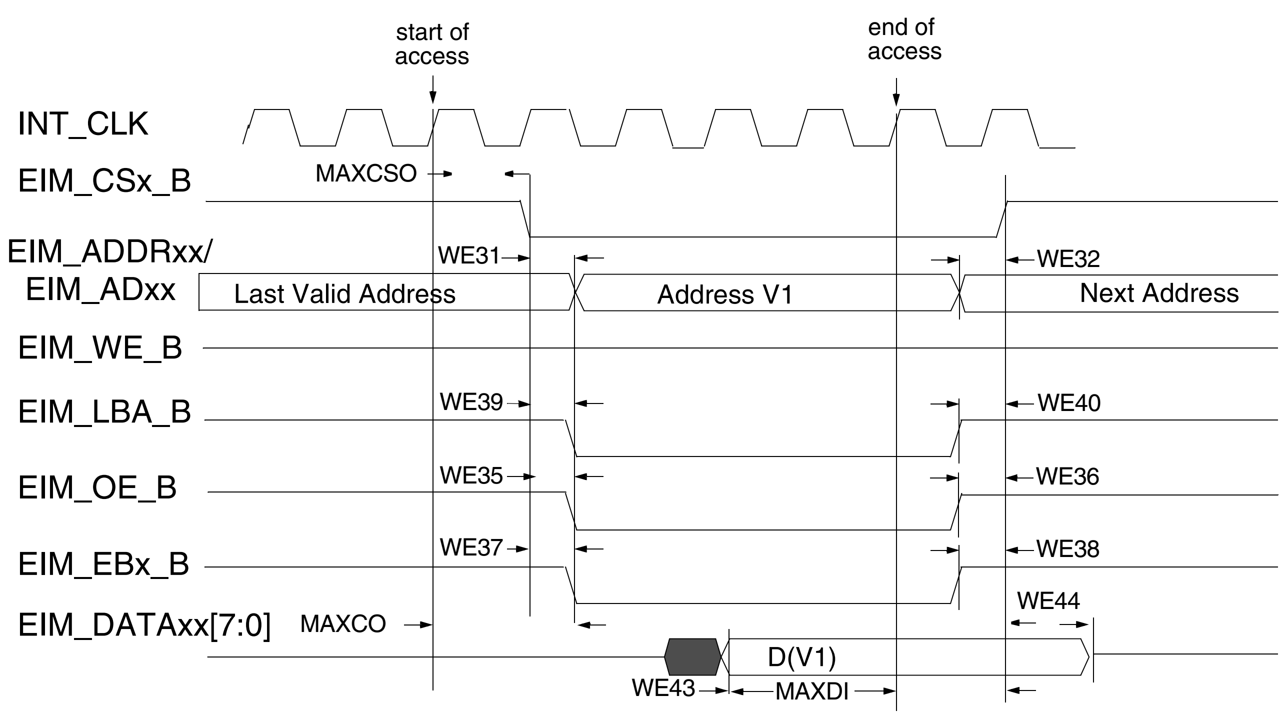


Figure 18. Asynchronous memory read access (RWSC = 5)

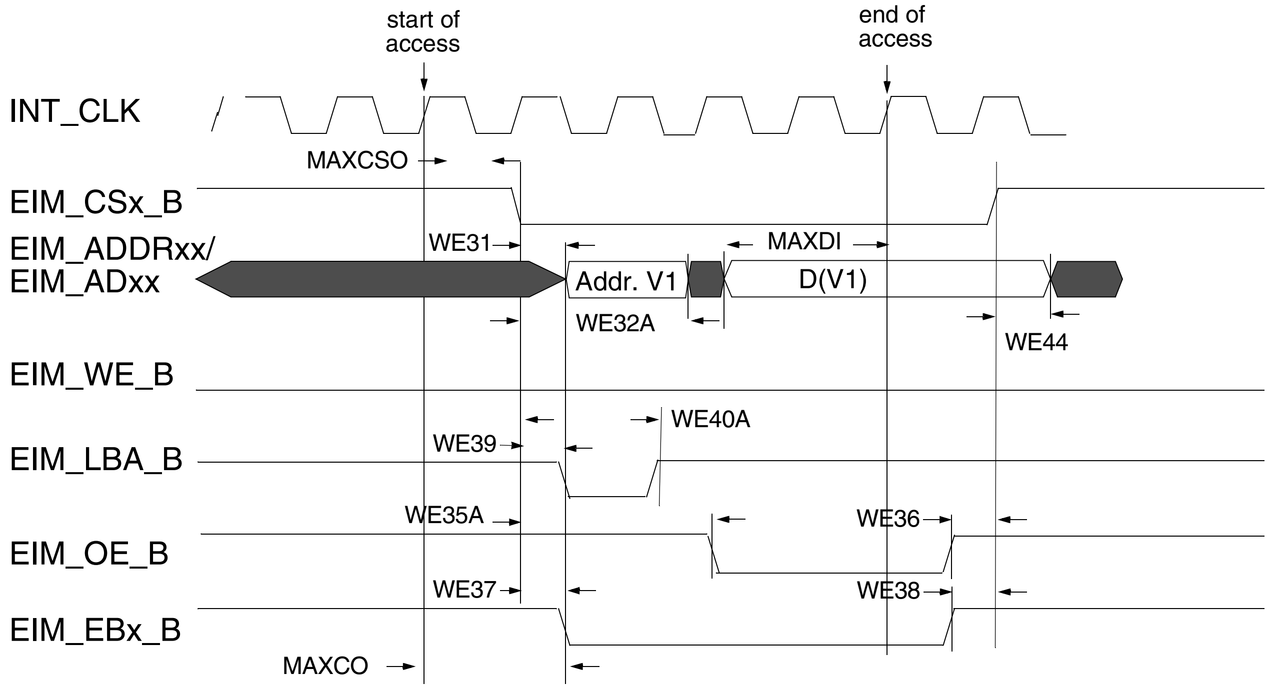


Figure 19. Asynchronous A/D muxed read access (RWSC = 5)

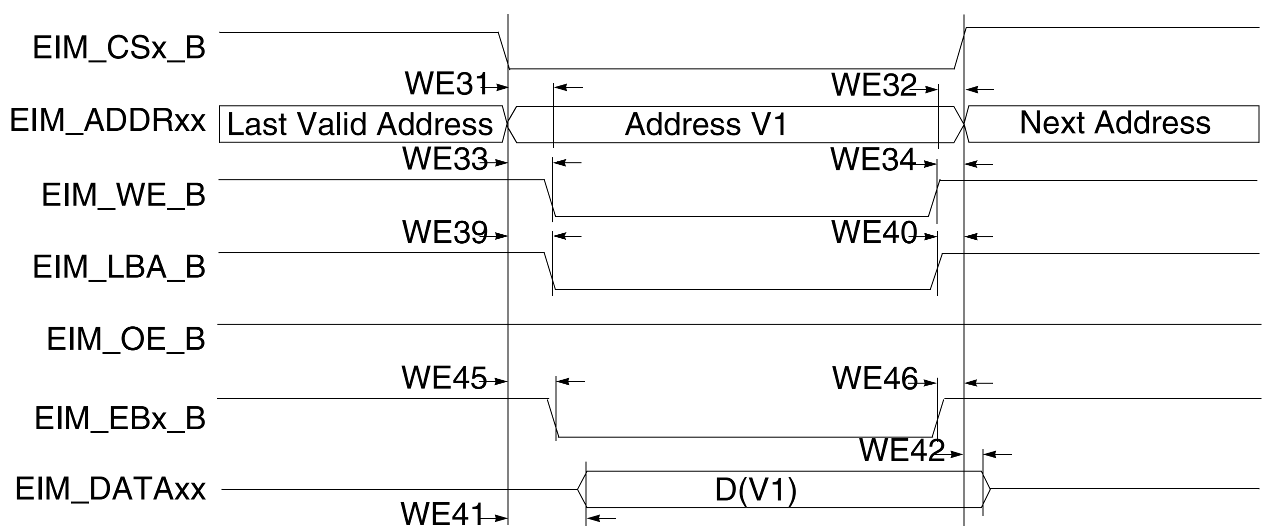


Figure 20. Asynchronous memory write access

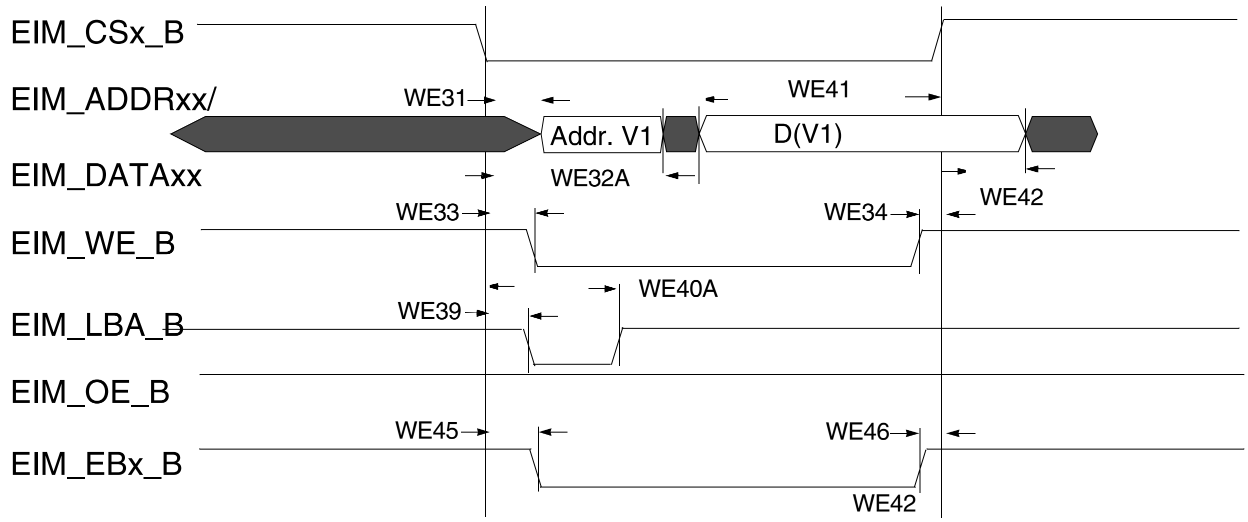


Figure 21. Asynchronous A/D muxed write access

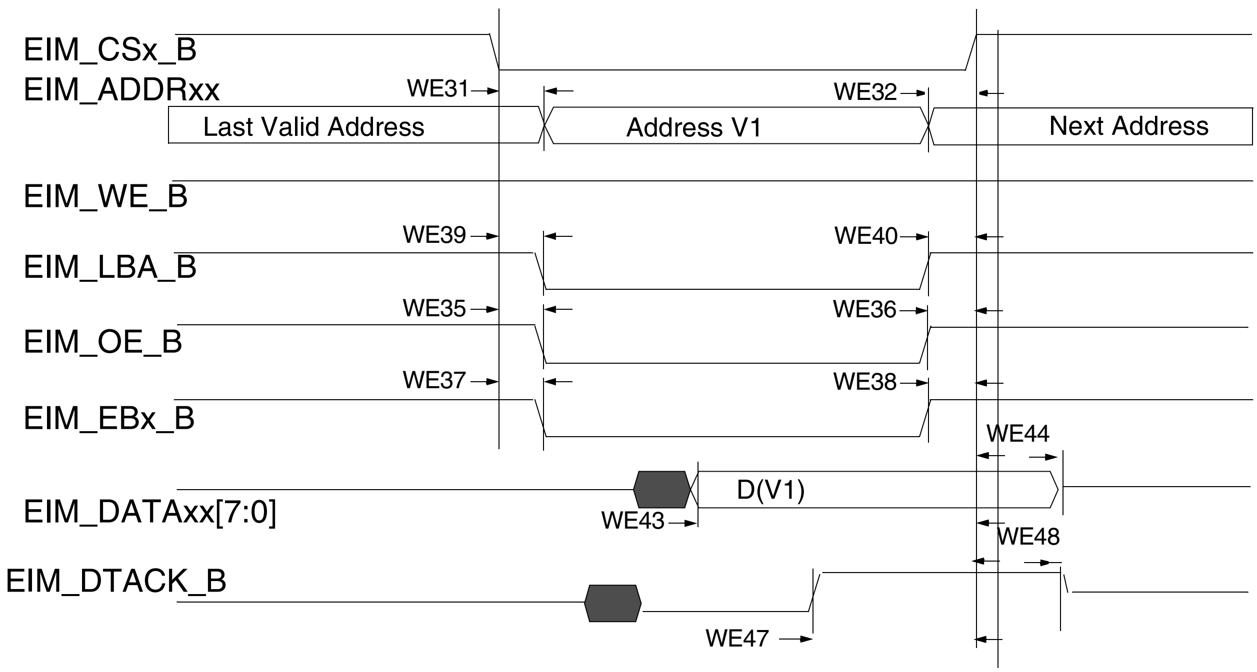


Figure 22. DTACK mode read access (DAP=0)

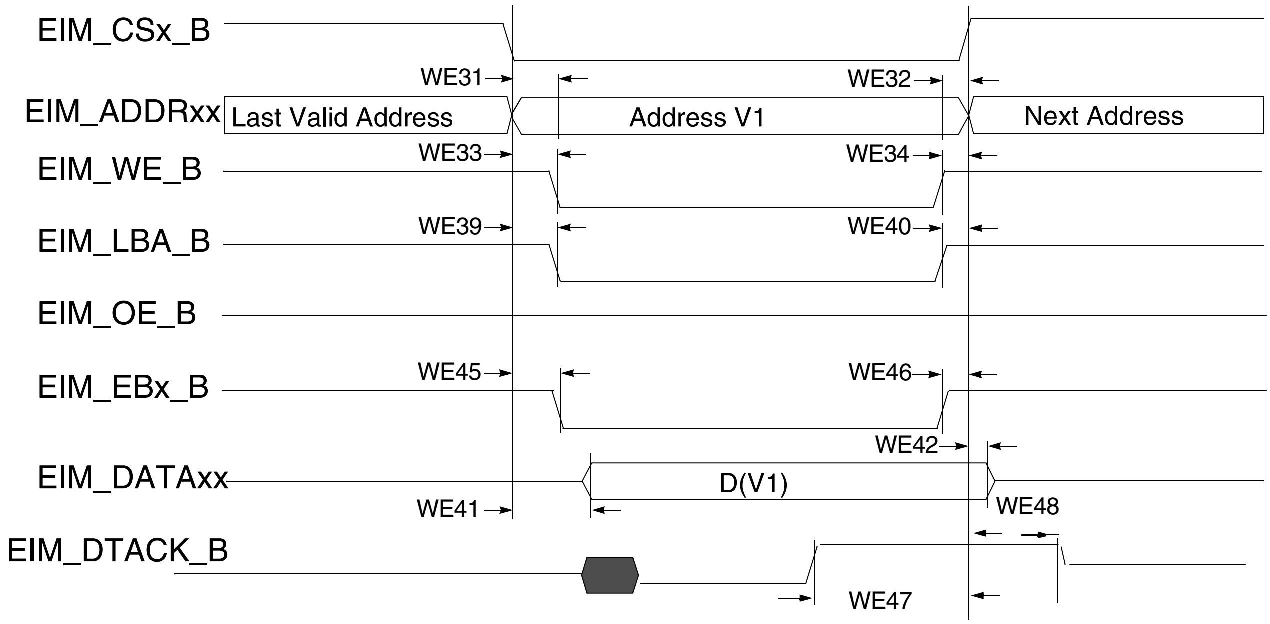


Figure 23. DTACK Mode write access (DAP=0)

Table 39. EIM asynchronous timing parameters table relative chip to select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address Invalid to EIM_CSx_B invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns
WE32A(muxed A/D	EIM_CSx_B valid to Address Invalid	t[4] + WE4 – WE7 + (ADVN[5] + ADVA[6] + 1 – CSA)	–3 + (ADVN + ADVA + 1 – CSA)	—	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8 – WE6 + (WEA – WCSA)	—	3 + (WEA – WCSA)	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7 – WE9 + (WEN – WCSN)	—	3 + (WEN – WCSN)	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 – WE6 + (OEA – RCSA)	—	3 + (OEA – RCSA)	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 – WE6 + (OEA + RADVN + RADVA + ADH + 1 – RCSA)	–3 + (OEA + RADVN+RADVA+ADH+1–RCSA)	3 + (OEA + RADVN+RADVA+ADH+1–RCSA)	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7 – WE11 + (OEN – RCSN)	—	3 – (OEN – RCSN)	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12 – WE6 + (RBEA – RCSA)	—	3 + (RBEA – RCSA)	ns

Table 39. EIM asynchronous timing parameters table relative chip to select(continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7 – WE13 + (RBEN – RCSN)	—	3 – (RBEN– RCSN)	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14 – WE6 + (ADVA – CSA)	—	3 + (ADVA – CSA)	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7 – WE15 – CSN	—	3 – CSN	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14 – WE6 + (ADVN + ADVA + 1 – CSA)	–3 + (ADVN + ADVA + 1 – CSA)	3 + (ADVN + ADVA + 1 – CSA)	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16 – WE6 + (WADVN + WADVA + ADH + 1 – WCSA)	—	3 + (WADVN + WADVA + ADH + 1 – WCSA)	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control FFs to chip outputs	10	—	—	ns
MAXCSO	Output maximum delay from CSx internal driving FFs to CSx out	10	—	—	ns
MAXDI	EIM_DATAxx maximum delay from chip input data to its internal FF	5	—	—	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO – MAXCSO + MAXDI	MAXCO – MAXCSO + MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12 – WE6 + (WBEA – WCSA)	—	3 + (WBEA – WCSA)	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7 – WE13 + (WBEN – WCSN)	—	–3 + (WBEN – WCSN)	ns

Table 39. EIM asynchronous timing parameters table relative chip to select(continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
MAXDTI	MAXIMUM delay from EIM_DTACK_B to its internal FF + 2 cycles for synchronization	10	—	—	ns
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO – MAXCSO + MAXDTI	MAXCO – MAXCSO + MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B Invalid	0	0	—	ns

[1] For more information on configuration parameters mentioned in this table, see the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

[2] In this table, CSA means WCSA when write operation or RCSA when read operation.

[3] In this table, CSN means WCSN when write operation or RCSN when read operation.

[4] t is axi_clk cycle time.

[5] In this table, ADVN means WADVN when write operation or RADVN when read operation.

[6] In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.8.4 DDR SDRAM-specific parameters (DDR3, DDR3L, LPDDR3, and LPDDR2)

4.8.4.1 DDR3/DDR3L parameters

Figure 24 shows the DDR3 basic timing diagram with the timing parameters provided in Table 40.

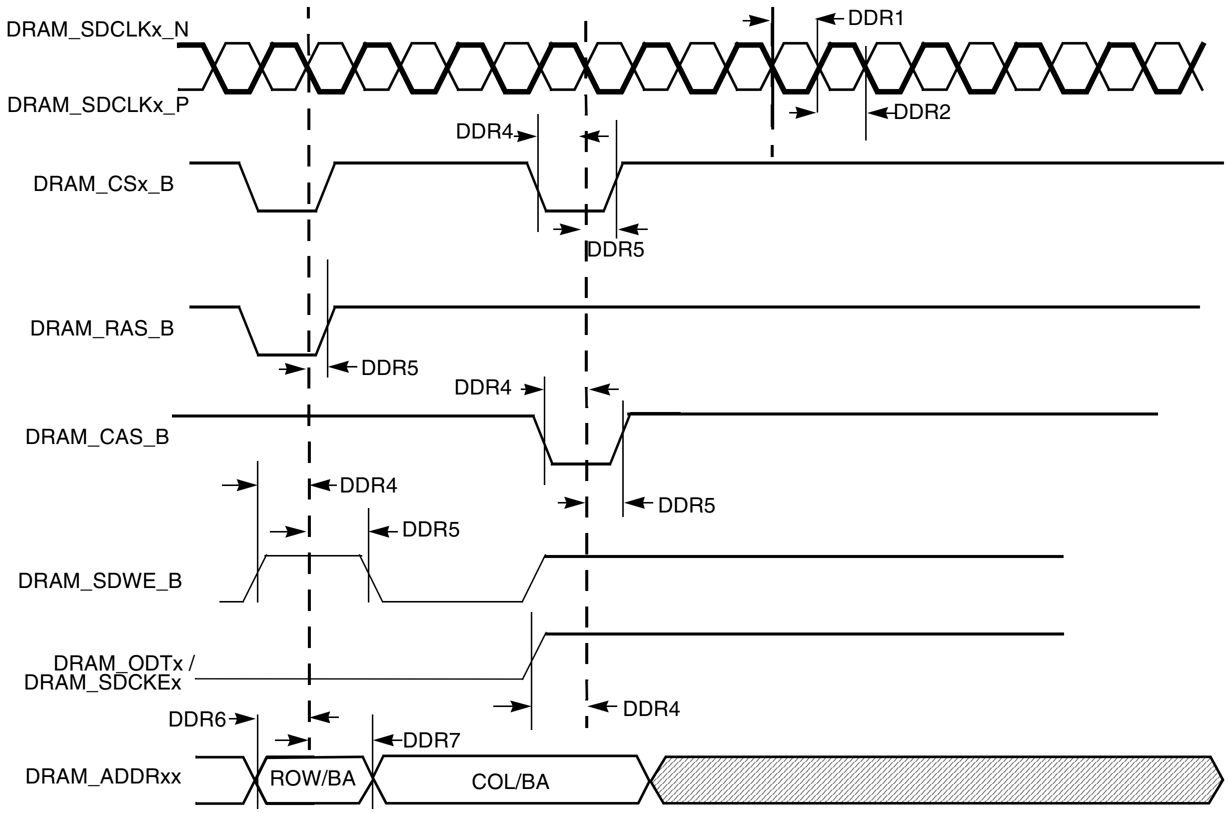


Figure 24. DDR3 Command and Address Timing Diagram

Table 40. DDR3 timing parameters

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
DDR1	DRAM_SDCLKx_P clock high-level width	tCH	0.47	0.53	tCK
DDR2	DRAM_SDCLKx_P clock low-level width	tCL	0.47	0.53	tCK
DDR4	DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKE, DRAM_SDWE_B, DRAM_SDODTx setup time	tIS	425	—	ps
DDR5	DRAM_CSx_B, DRAM_RAS_B, DRAM_CAS_B, DRAM_SDCKE, DRAM_SDWE_B, DRAM_SDODTx hold time	tIH	375	—	ps
DDR6	Address output setup time	tIS	425	—	ps
DDR7	Address output hold time	tIH	375	—	ps

1 All measurements are in reference to Vref level.
2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 25 shows the DDR3 write timing diagram. The timing parameters for this diagram appear in Table 41.

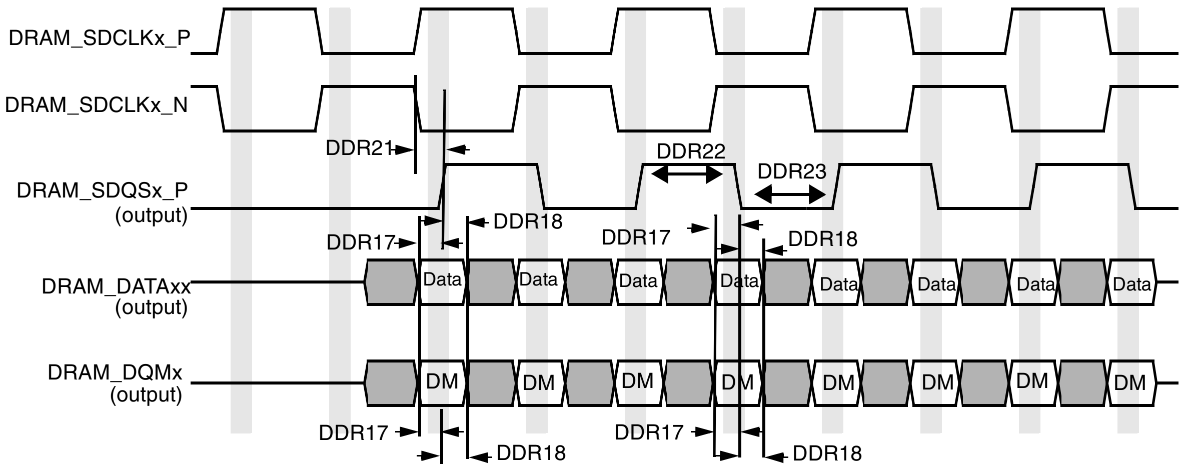


Figure 25. DDR3 write cycle

Table 41. DDR3 write cycle

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
DDR17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	tDS	225	—	ps
DDR18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	tDH	250	—	ps
DDR21	DRAM_SDQSx_P latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DRAM_SDQSx_P high level width	tDQSH	0.45	0.55	tCK
DDR23	DRAM_SDQSx_P low level width	tDQSL	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.
2 All measurements are in reference to Vref level.
3 Measurements were taken using balanced load and 25 Ω resistor from outputs to DDR_VREF.

Figure 26 shows the DDR3 read timing diagram. The timing parameters for this diagram appear in Table 42.

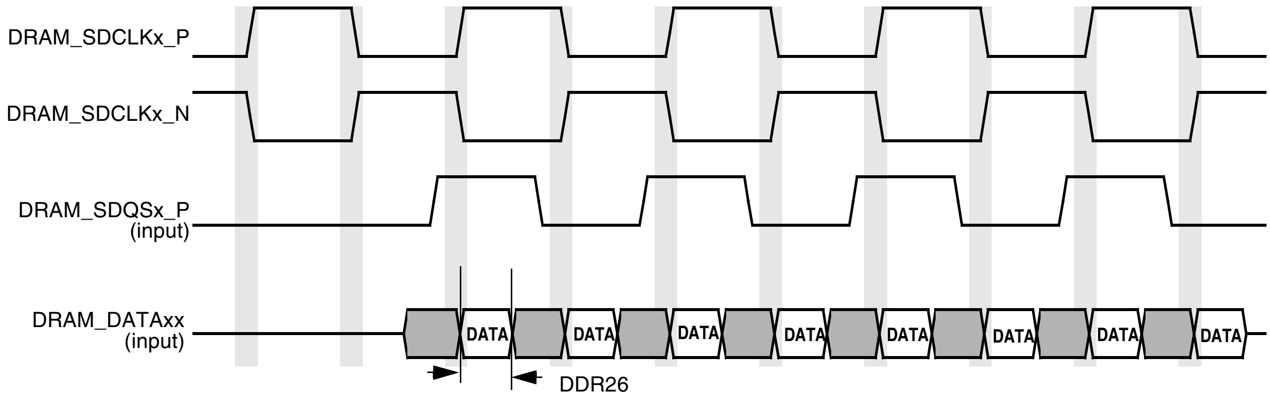


Figure 26. DDR3 read cycle

Table 42. DDR3 read cycle

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
DDR26	Minimum required DRAM_DATAxx valid window width	—	510	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.
2 All measurements are in reference to Vref level.
3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.8.4.2 LPDDR3 parameters

Figure 27 shows the LPDDR3 basic timing diagram. The timing parameters for this diagram appear in Table 43.

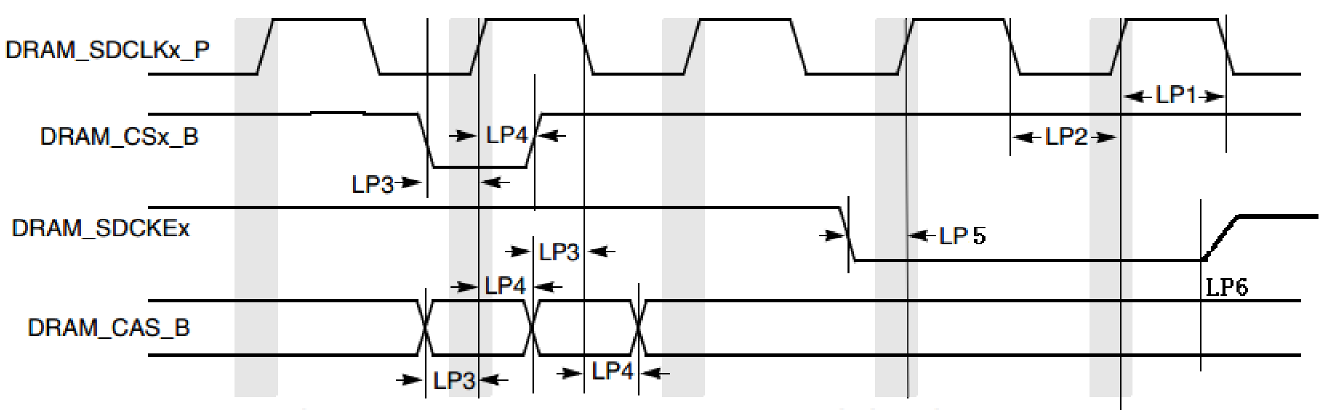


Figure 27. LPDDR3 command and address timing diagram

Table 43. LPDDR3 timing parameters[1,2]

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	DRAM_CSx_B	t_{IS}	390	—	ps
LP4	DRAM_CSx_E	t_{IH}	390	—	ps
LP3	DRAM_CAS_B setup time	t_{IS}	275	—	ps
LP4	DRAM_CAS_B hold time	t_{IH}	275	—	ps

1 All measurements are in reference to V_{ref} level.
2 Measurements were done using balanced load and 25 Ω resistor from outputs to DDR_VREF.

Figure 28 shows the LPDDR3 write timing diagram. The timing parameters for this diagram appear in Table 44.

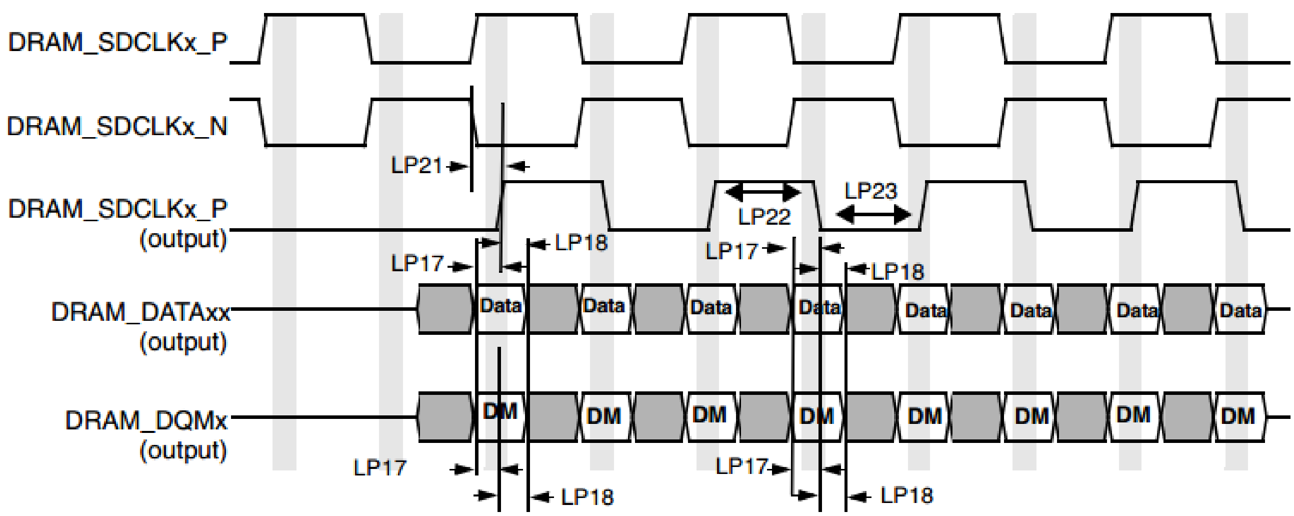


Figure 28. LPDDR3 write cycle

Table 44. LPDDR3 write cycle[1,2,3]

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
LP17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	tDS	275	—	ps
LP18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	tDH	275	—	ps
LP21	DRAM_SDQSx_P latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	t_{CK}
LP22	DRAM_SDQSx_P high level width	tDQSH	0.4	—	t_{CK}
LP23	DRAM_SDQSx_P low level width	tDQSL	0.4	—	t_{CK}

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DRAM_SDQS in the middle of DRAM_DATAxx window.

2 All measurements are in reference to V_{ref} level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to DDR_VREF.

Figure 29 shows the LPDDR3 read timing diagram. The timing parameters for this diagram appear in Table 45.

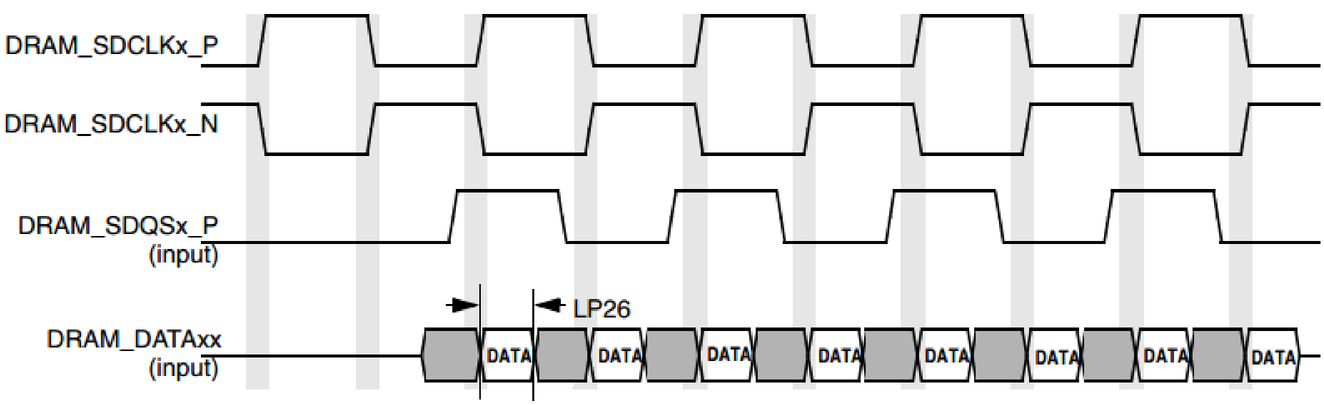


Figure 29. LPDDR3 read cycle

Table 45. LPDDR3 read cycle[1,2,3]

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
LP26	Minimum required DRAM_DATAxx valid window width for LPDDR3	—	460	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DRAM_SDQSx_P in the middle of DRAM_DATA_xx window.

2 All measurements are in reference to V_{ref} level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to DDR_VREF.

4.8.4.3 LPDDR2 parameters

Figure 30 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 46.

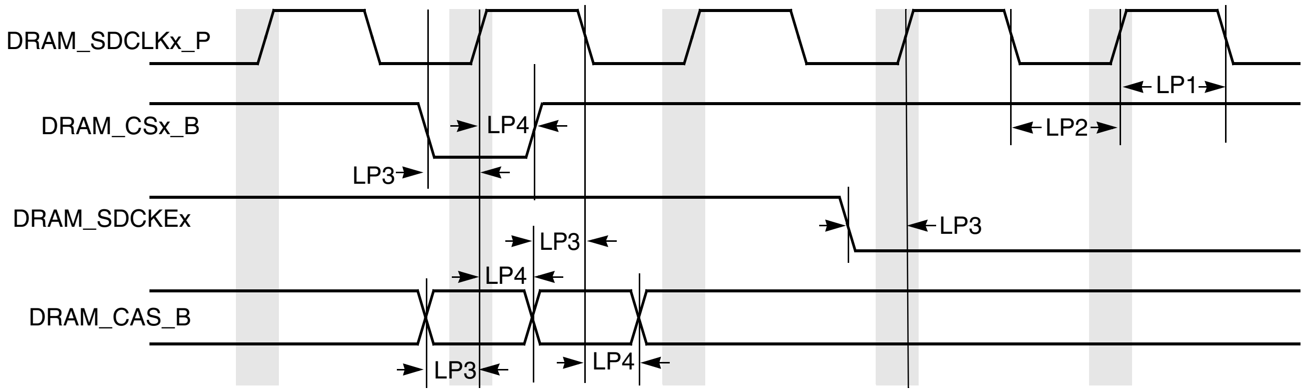


Figure 30. LPDDR2 command and address timing diagram

Table 46. LPDDR2 timing parameters[1,2]

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	tCH	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	tCL	0.45	0.55	t_{CK}
LP3	DRAM_CSx_B, DRAM_SDCKEx setup time	tIS	370	—	ps
LP4	DRAM_CSx_B, DRAM_SDCKEx hold time	tIH	370	—	ps
LP3	DRAM_CAS_B setup time	tIS	770	—	ps
LP4	DRAM_CAS_B hold time	t_{IH}	770	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to DDR_VREF

Figure 31 shows the LPDDR2 write timing diagram. The timing parameters for this diagram appear in Table 47.

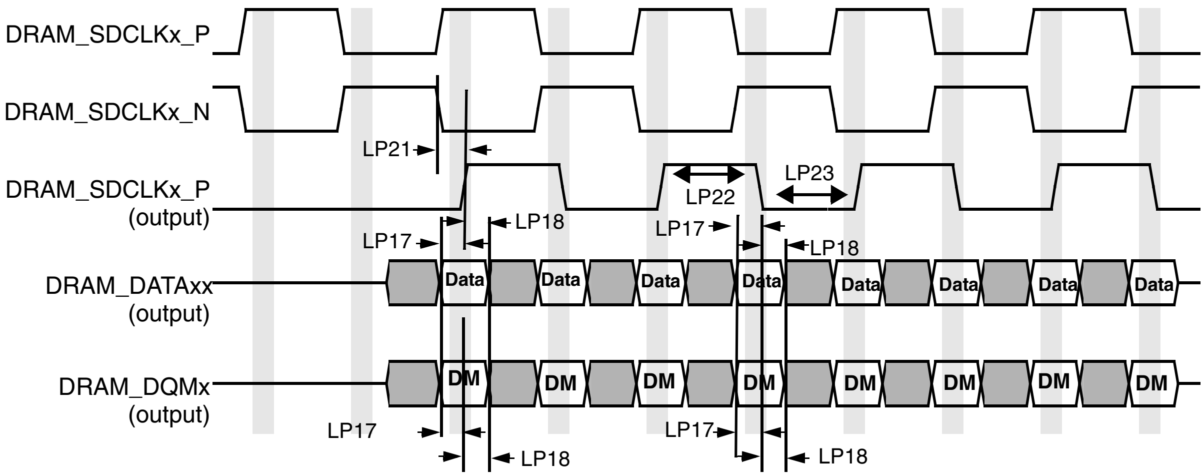


Figure 31. LPDDR2 write cycle

Table 47. LPDDR2 write cycle

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
LP17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	tDS	360	—	ps
LP18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	tDH	360	—	ps
LP21	DRAM_SDQSx_P latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
LP22	DRAM_SDQSx_P high level width	tDQSH	0.4	—	tCK
LP23	DRAM_SDQSx_P low level width	tDQSL	0.4	—	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DRAM_SDQS in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to DDR_VREF.

Figure 32 shows the LPDDR2 read timing diagram. The timing parameters for this diagram appear in Table 48.

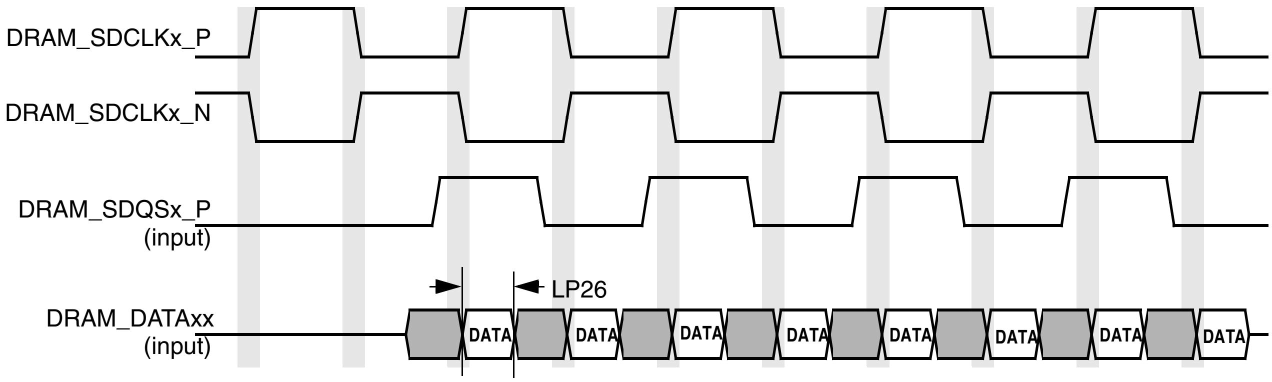


Figure 32. LPDDR2 read cycle

Table 48. LPDDR2 read cycle

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
LP26	Minimum required DRAM_DATAxx valid window width for LPDDR2	—	230	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DRAM_SDQSx_P in the middle of DRAM_DATA_xx window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to DDR_VREF.

4.9 General-purpose media interface (GPMI) timing

The i.MX 7Solo GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous Timing mode, Source Synchronous Timing mode and Toggle Timing mode separately, as described in the following subsections.

4.9.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 33 through Figure 36 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 49 describes the timing parameters (NF1–NF17) that are shown in the figures.

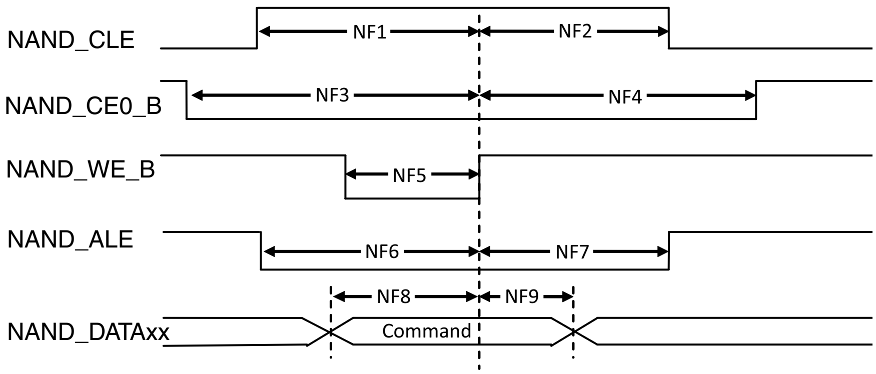


Figure 33. Command Latch cycle timing diagram

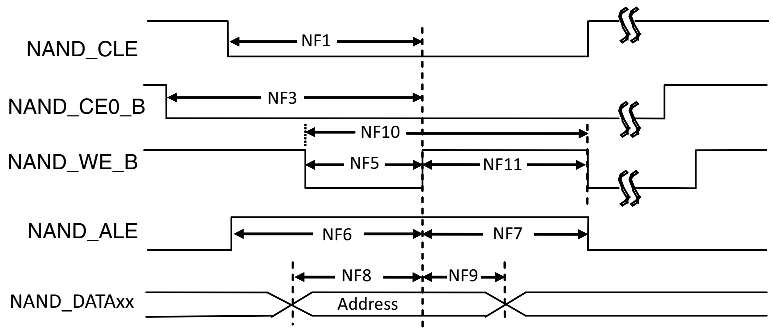


Figure 34. Address Latch cycle timing diagram

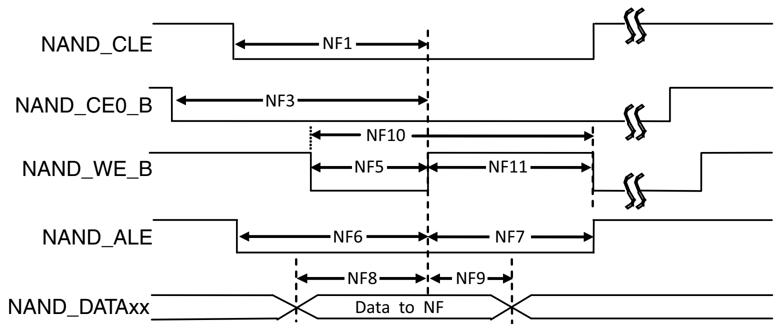


Figure 35. Write Data Latch cycle timing diagram

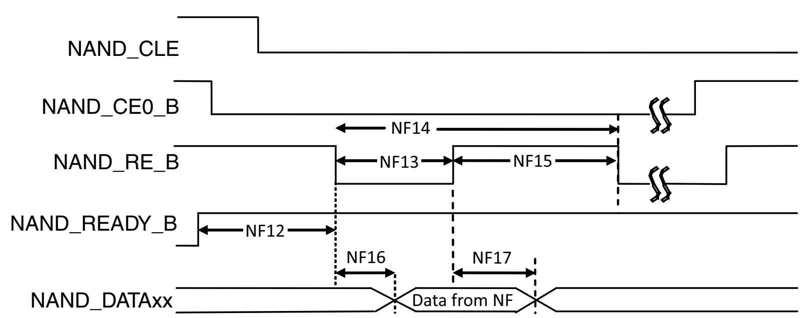


Figure 36. Read Data Latch cycle timing diagram (Non-EDO Mode)

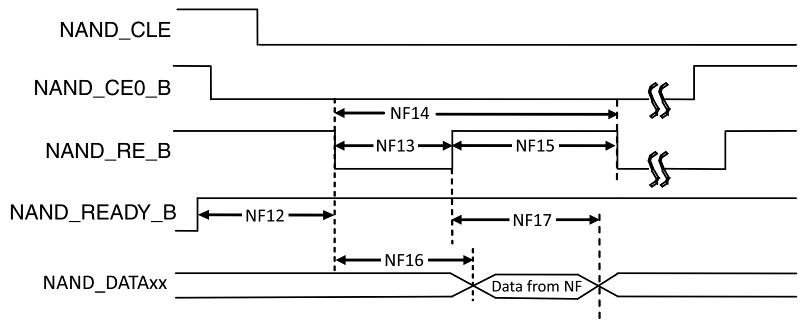


Figure 37. Read Data Latch cycle timing diagram (EDO mode)

Table 49. Asynchronous mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see notes[2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		ns
NF3	NAND_CE0_B setup time	tCS	(AS + DS + 1) × T [see notes[3,2]]		ns
NF4	NAND_CE0_B hold time	tCH	(DH+1) × T - 1 [see note[2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes[3,2]]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see note[2]]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see note[2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see note[2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see note[2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see note[2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see note[2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see note[2]]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see note[2]]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see notes[5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see notes[5,6]]	—	ns

[1] GPMI's Asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

[2] AS minimum value can be 0, while DS/DH minimum value is 1.

[3] T = GPMI clock period -0.075ns (half of maximum p-p jitter).

[4] NF12 is guaranteed by the design.

[5] Non-EDO mode.

[6] EDO mode, GPMI clock ≈ 100 MHz (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 36), NF16/NF17 are different from the definition in non-EDO mode (Figure 35). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 7Dual Application Processor Reference Manual* [IMX7DRM]). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.9.2 Source Synchronous mode AC timing (ONFI 2.x compatible)

Figure 38 to Figure 40 show the write and read timing of Source Synchronous mode.

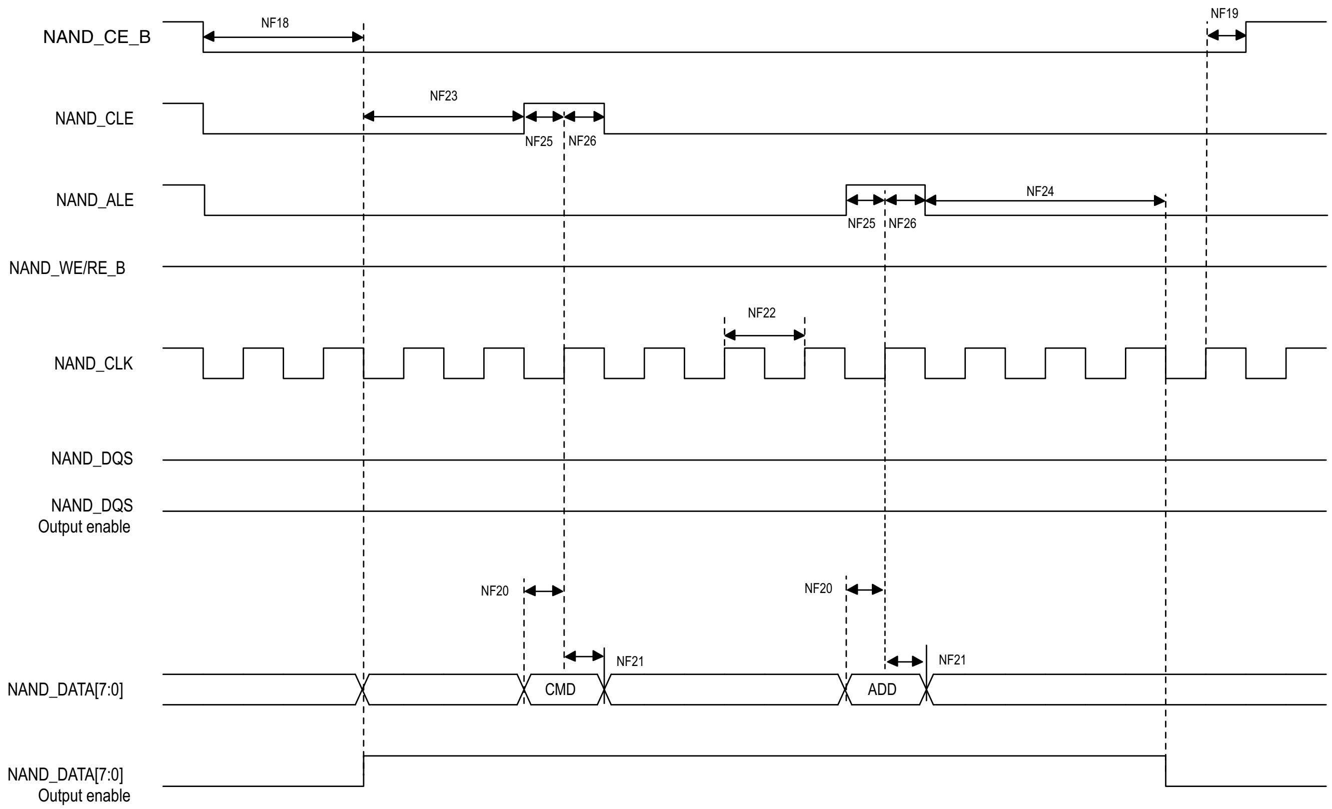


Figure 38. Source Synchronous mode command and address timing diagram

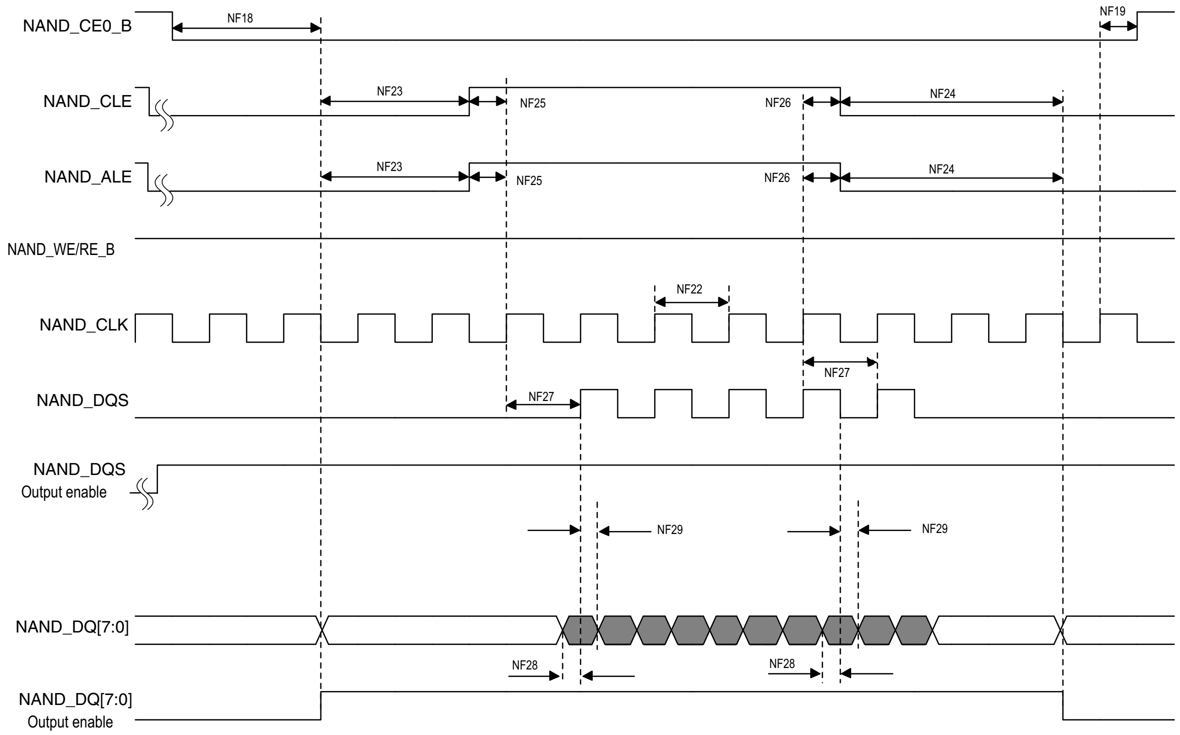


Figure 39. Source Synchronous mode data write timing diagram

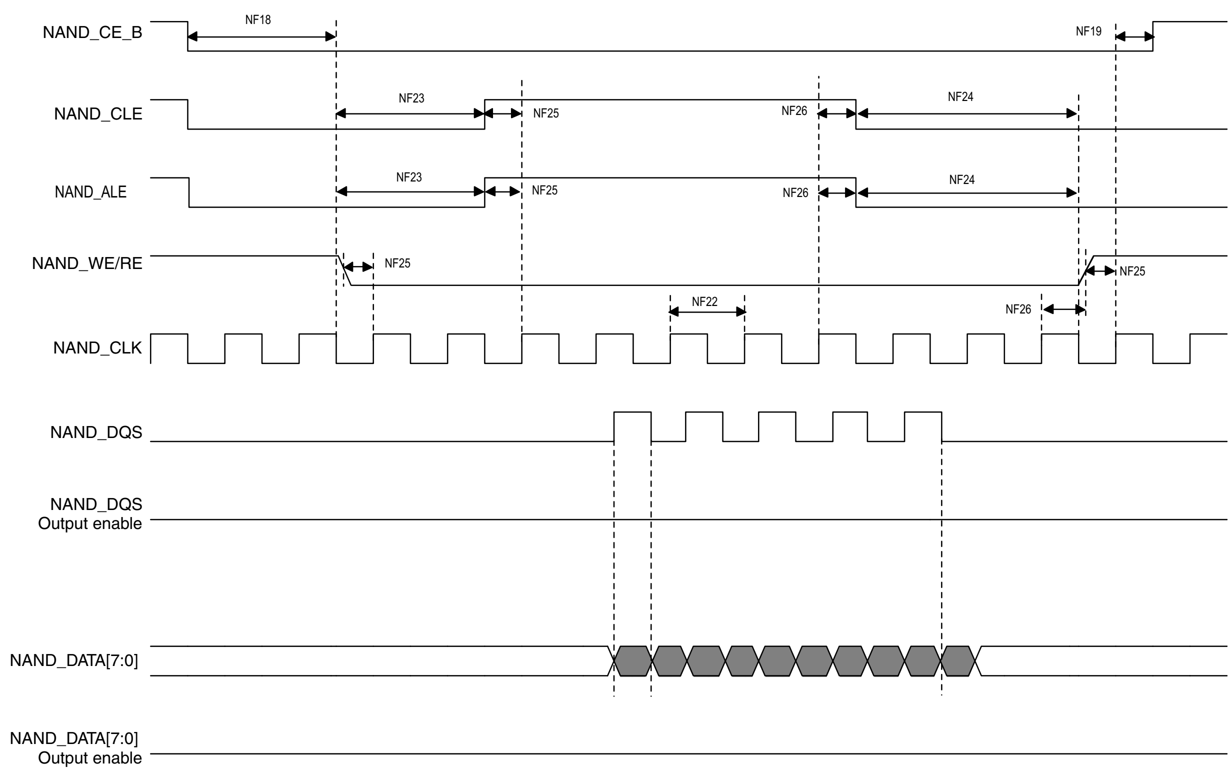


Figure 40. Source Synchronous mode data read timing diagram

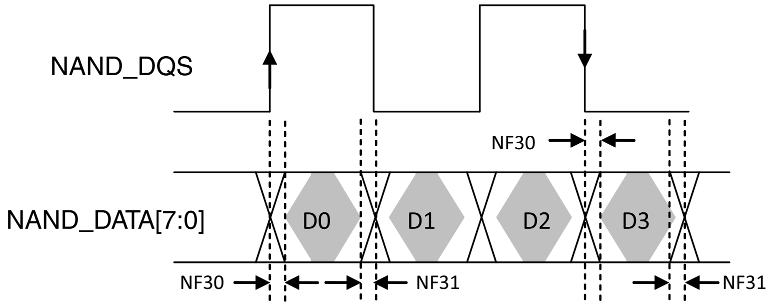


Figure 41. NAND_DQS/NAND_DQ Read Valid window

Table 50. Source Synchronous mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see note[2]]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see note[2]]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see note[2]]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see note[2]]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see note[2]]		ns
NF28	Data write setup		0.25 × tCK - 0.35		
NF29	Data write hold		0.25 × tCK - 0.85		
NF30	NAND_DQS/NAND_DQ read setup skew		—	2.06	
NF31	NAND_DQS/NAND_DQ read hold skew		—	1.95	

[1] GPMI's Source Synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

[2] T = tCK(GPMI clock period) –0.075 ns (half of maximum p-p jitter).

For DDR Source Synchronous mode, Figure 41 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 7Dual Application Processor Reference Manual* [IMX7DRM]). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.9.3 ONFI NV-DDR2 mode (ONFI 3.2 compatible)

4.9.3.1 Command and address timing

ONFI 3.2 mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.9.1, "Asynchronous mode AC timing (ONFI 1.0 compatible)," for details.

4.9.3.2 Read and write timing

ONFI 3.2 mode read and write timing is the same as Toggle mode AC timing. See Section 4.9.4, "Toggle mode AC Timing," for details.

4.9.4 Toggle mode AC Timing

4.9.4.1 Command and address timing

NOTE

Toggle mode command and address timing is the same as ONFI 1.0 compatible Asynchronous mode AC timing. See Section 4.9.1, "Asynchronous mode AC timing (ONFI 1.0 compatible)," for details.

4.9.4.2 Read and write timing

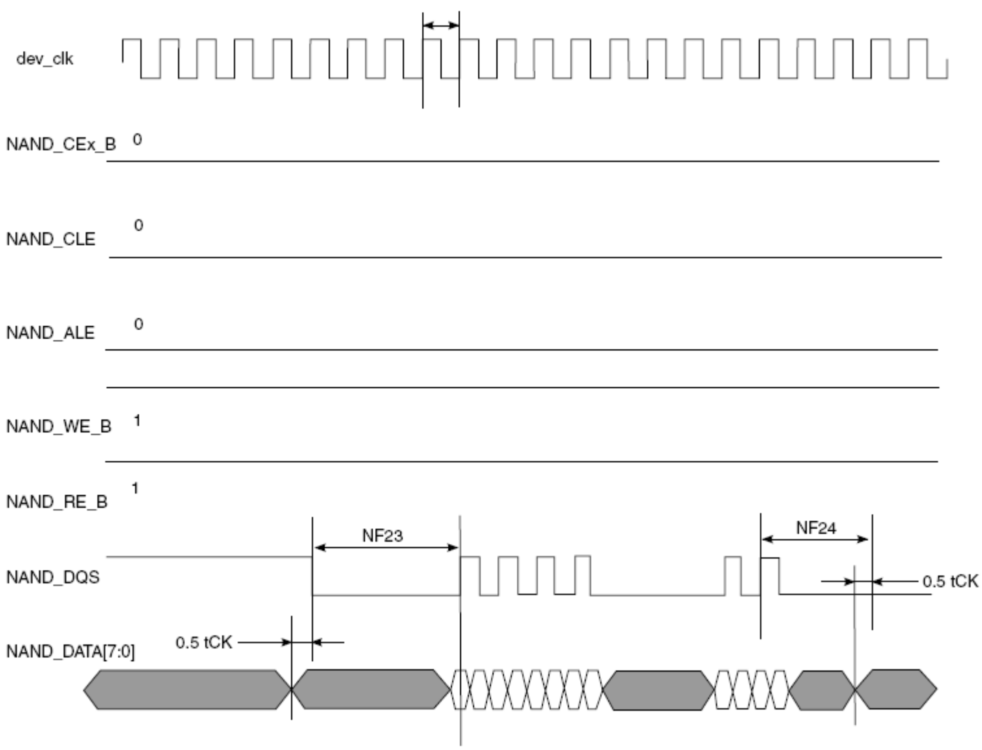


Figure 42. Toggle mode data write timing

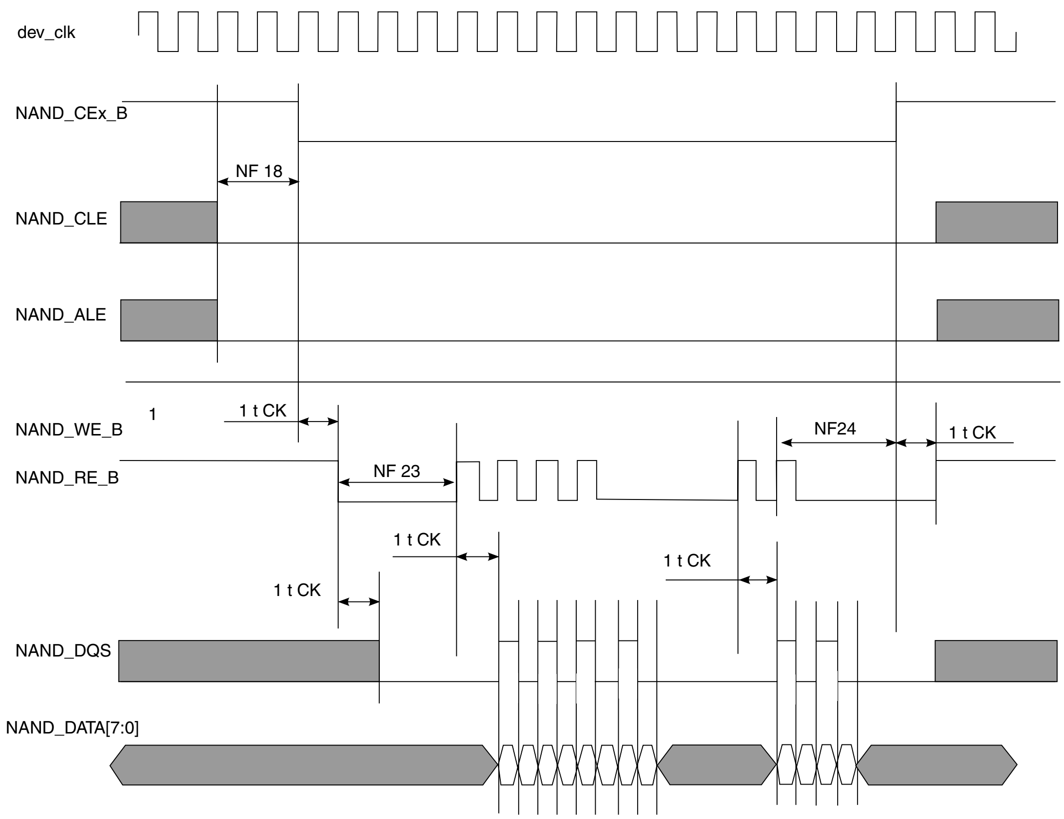


Figure 43. Toggle mode data read timing

Table 51. Toggle mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[2]s,[3]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes,[2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes,[2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes[4,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes[5,2]]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see note[2]]	—	ns

Table 51. Toggle mode timing parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075 ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS)

6 Shown in Figure 42.

7 Shown in Figure 43.

For DDR Toggle mode, Figure 41 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 7Dual Application Processor Reference Manual* [IMX7DRM]). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

4.10.1 ECSPI timing parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.10.1.1 ECSPI Master mode timing

Figure 44 depicts the timing of ECSPI in master mode. Table 52 lists the ECSPI master mode timing characteristics.

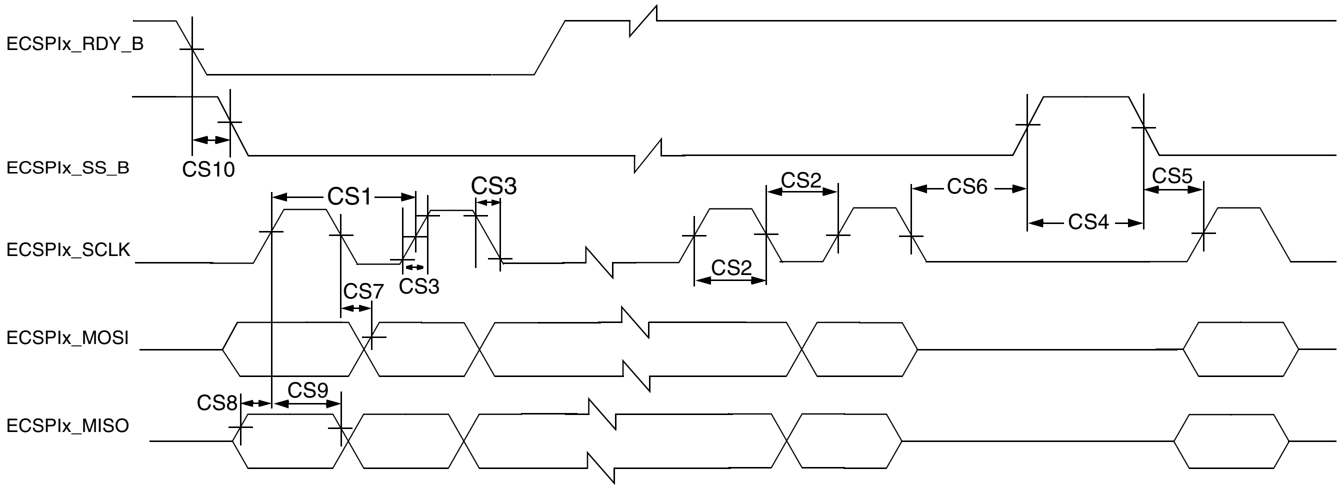


Figure 44. ECSPI Master mode timing diagram

Table 52. ECSPI Master mode timing parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	18	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.6, "I/O AC parameters."

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.10.1.2 ECSPI Slave mode timing

Figure 45 depicts the timing of ECSPI in Slave mode. Table 53 lists the ECSPI Slave mode timing characteristics.

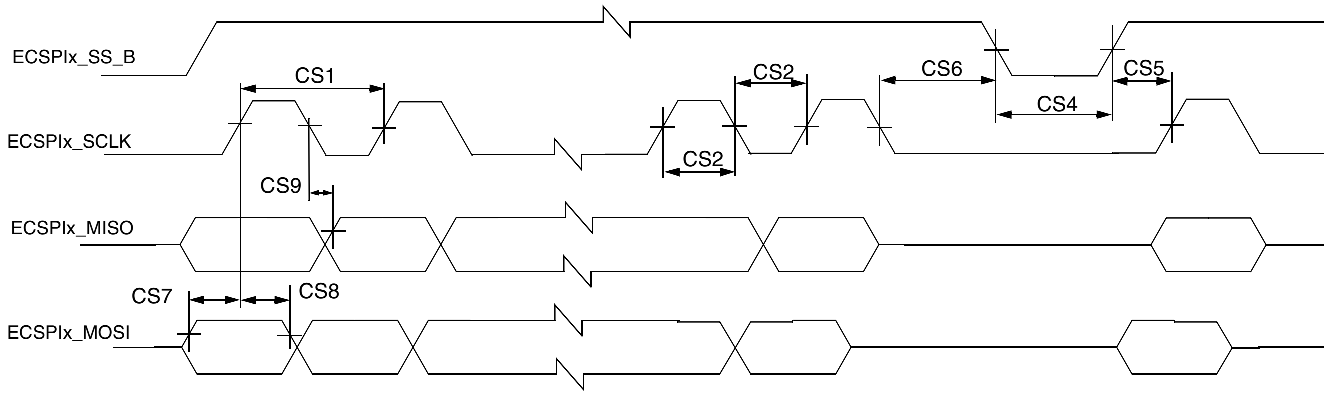


Figure 45. ECSPI Slave mode timing diagram

Table 53. ECSPI Slave mode timing parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

4.10.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (single data rate) timing, eMMC4.4/4.41 (dual data rate) timing and SDR104/50(SD3.0) timing.

4.10.2.1 SD/eMMC4.3 (single data rate) AC timing

Figure 46 depicts the timing of SD/eMMC4.3, and Table 54 lists the SD/eMMC4.3 timing characteristics.

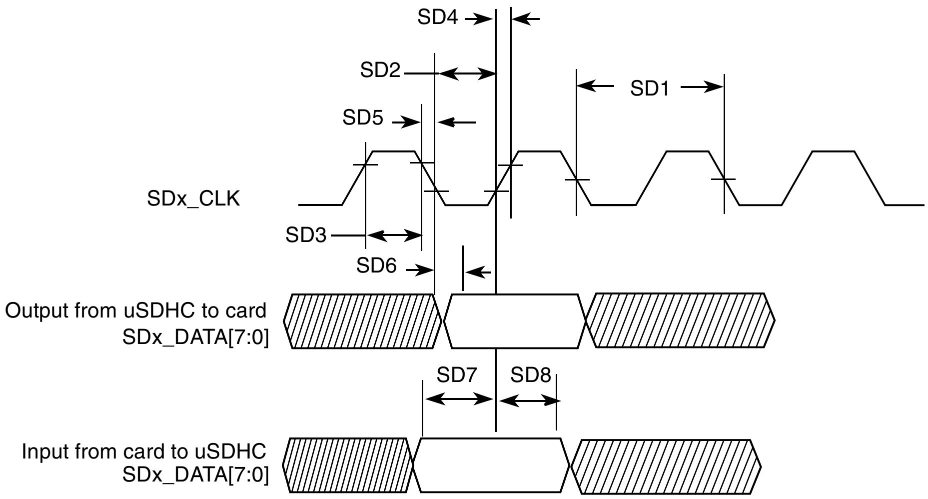


Figure 46. SD/eMMC4.3 Timing

Table 54. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Table 54. SD/eMMC4.3 interface timing specification(continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In High-speed mode, clock frequency can be any value between 0—50 MHz.

3 In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In High-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.10.2.2 eMMC4.4/4.41 (dual data rate) AC timing

Figure 47 depicts the timing of eMMC4.4/4.41. Table 55 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

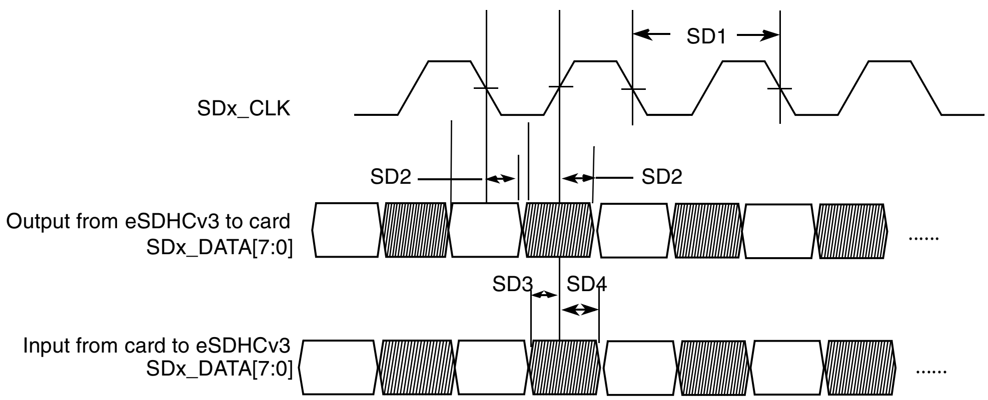


Figure 47. eMMC4.4/4.41 timing

Table 55. eMMC4.4/4.41 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.7	6.9	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					

Table 55. eMMC4.4/4.41 interface timing specification(continued)

ID	Parameter	Symbols	Min	Max	Unit
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.3	—	ns

4.10.2.3 HS400 AC timing—eMMC5.0 only

Figure 48 depicts the timing of HS400. Table 56 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6 and SD7 parameters in Table 58 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

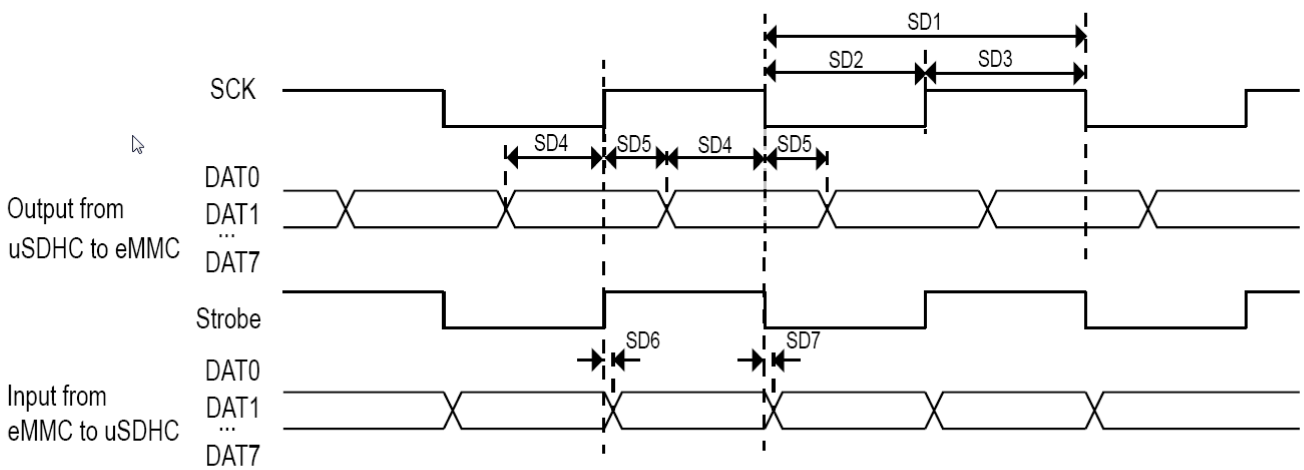


Figure 48. HS400 timing

Table 56. HS400 interface timing specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input clock					
SD1	Clock Frequency	fPP	0	200	Mhz
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card inputs DAT (Reference to SCK)					
SD4	Output Skew from Data of Edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output Skew from Edge of SCK to Data	t_{OSkew2}	0.45	—	ns

Table 56. HS400 interface timing specifications(continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

4.10.2.4 HS200 Mode Timing

Figure 49 depicts the timing of HS200 mode, and Table 57 lists the HS200 timing characteristics.

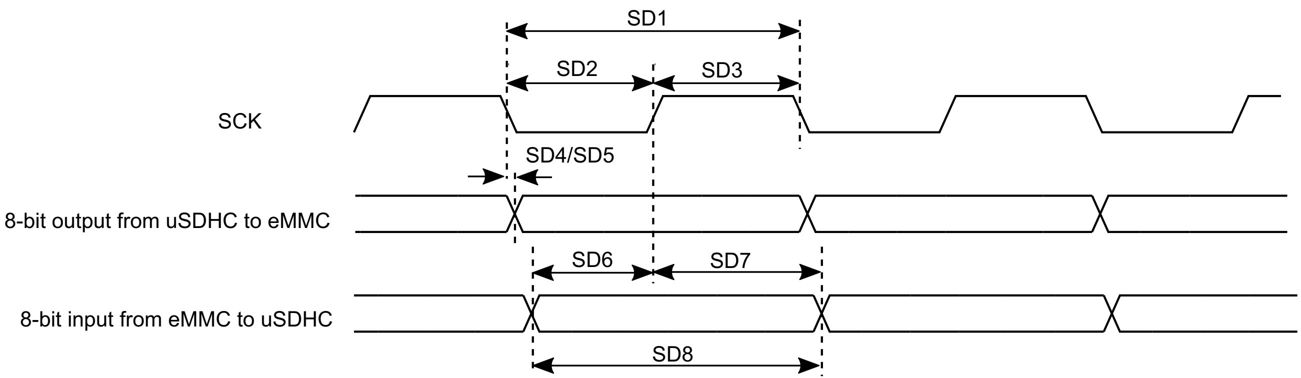


Figure 49. HS200 Mode Timing

Table 57. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.3*t_{CLK}	0.7*t_{CLK}	ns
SD2	Clock High Time	t_{CH}	0.3*t_{CLK}	0.7*t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5*t_{CLK}	—	ns

[1] HS200 is for 8 bits while SDR104 is for 4 bits.

4.10.2.5 SDR50/SDR104 AC timing

Figure 50 depicts the timing of SDR50/SDR104, and Table 58 lists the SDR50/SDR104 timing characteristics.

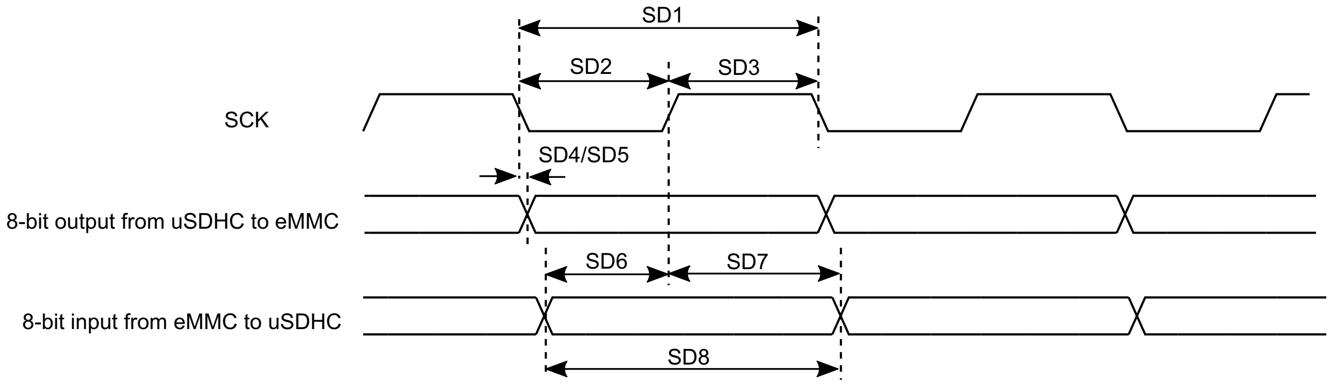


Figure 50. SDR50/SDR104 timing

Table 58. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.4	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5{*}t_{CLK}$	—	ns

[1] Data window in SDR100 mode is variable.

4.10.2.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 22, "GPIO DC Parameters," on page 38.

4.10.3 Ethernet controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.10.3.1 ENET MII mode timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.10.3.1.1 MII receive signal timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 51 shows MII receive signal timings. Table 59 describes the timing parameters (M1–M4) shown in the figure.

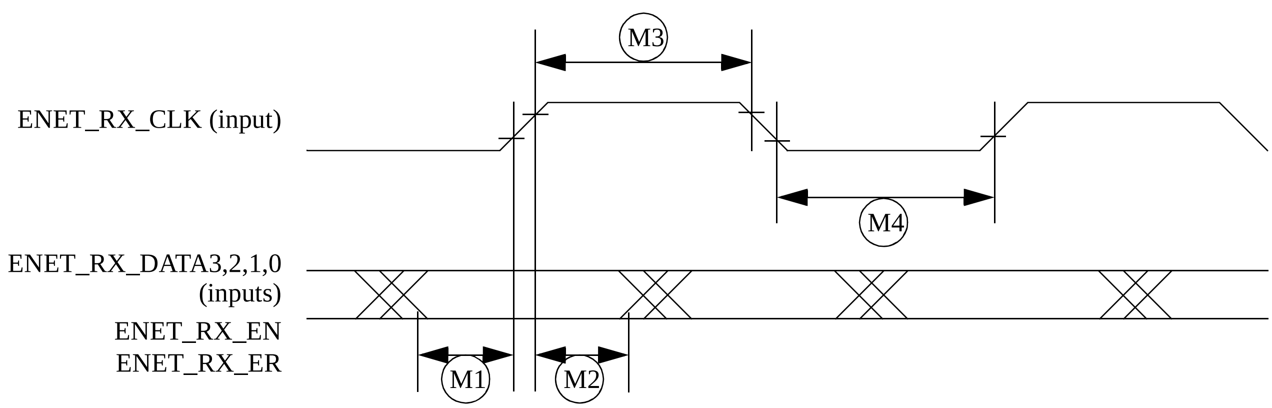


Figure 51. MII receive signal timing diagram

Table 59. MII receive signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.10.3.1.2 MII transmit signal timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 52 shows MII transmit signal timings. Table 60 describes the timing parameters (M5–M8) shown in the figure.

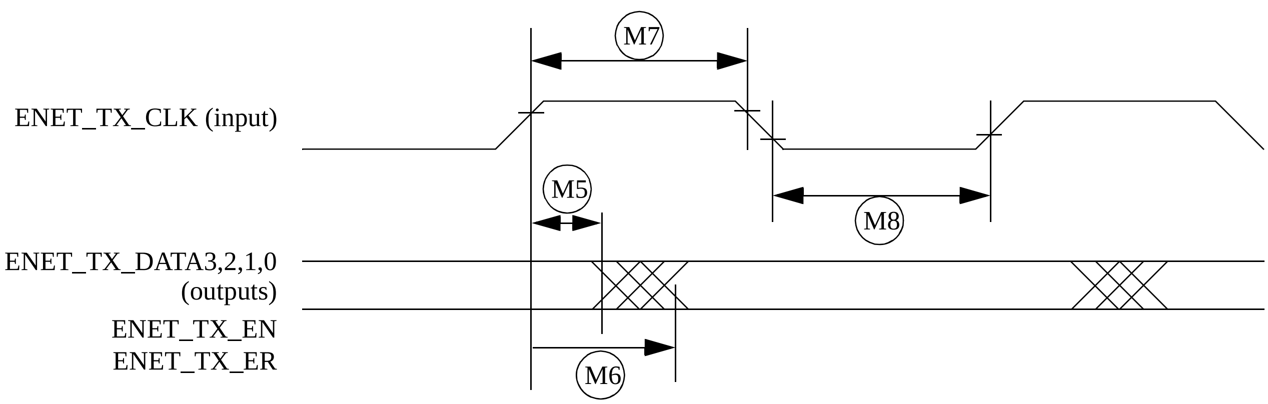


Figure 52. MII transmit signal timing diagram

Table 60. MII transmit signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.10.3.1.3 MII asynchronous inputs signal timing (ENET_CRS and ENET_COL)

Figure 53 shows MII asynchronous input timings. Table 61 describes the timing parameter (M9) shown in the figure.

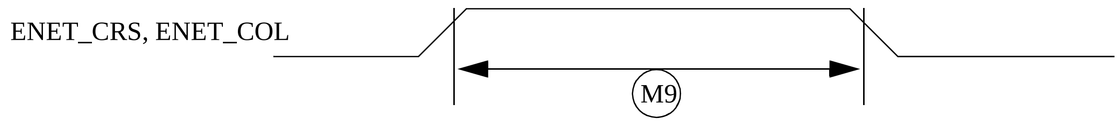


Figure 53. MII async inputs timing diagram

Table 61. MII asynchronous inputs signal timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.10.3.1.4 MII Serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 54 shows MII asynchronous input timings. Table 62 describes the timing parameters (M10–M15) shown in the figure.

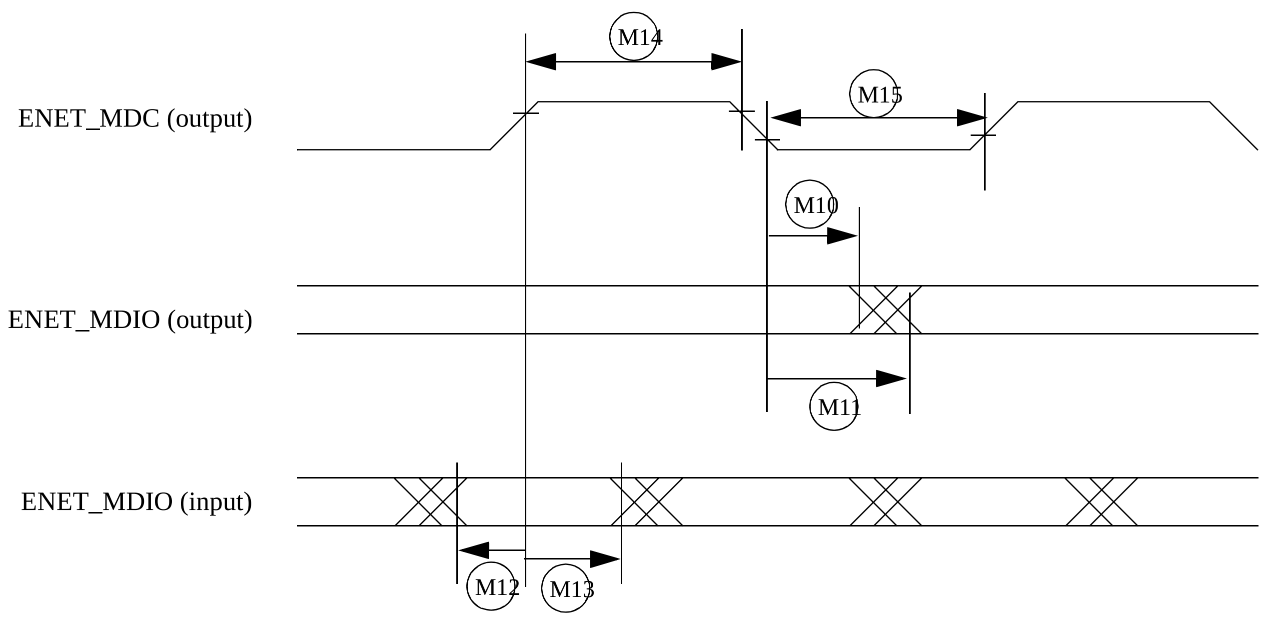


Figure 54. MII serial management channel timing diagram

Table 62. MII serial management channel timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.10.3.2 RMII mode timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

Figure 55 shows RMII mode timings. Table 63 describes the timing parameters (M16–M21) shown in the figure.

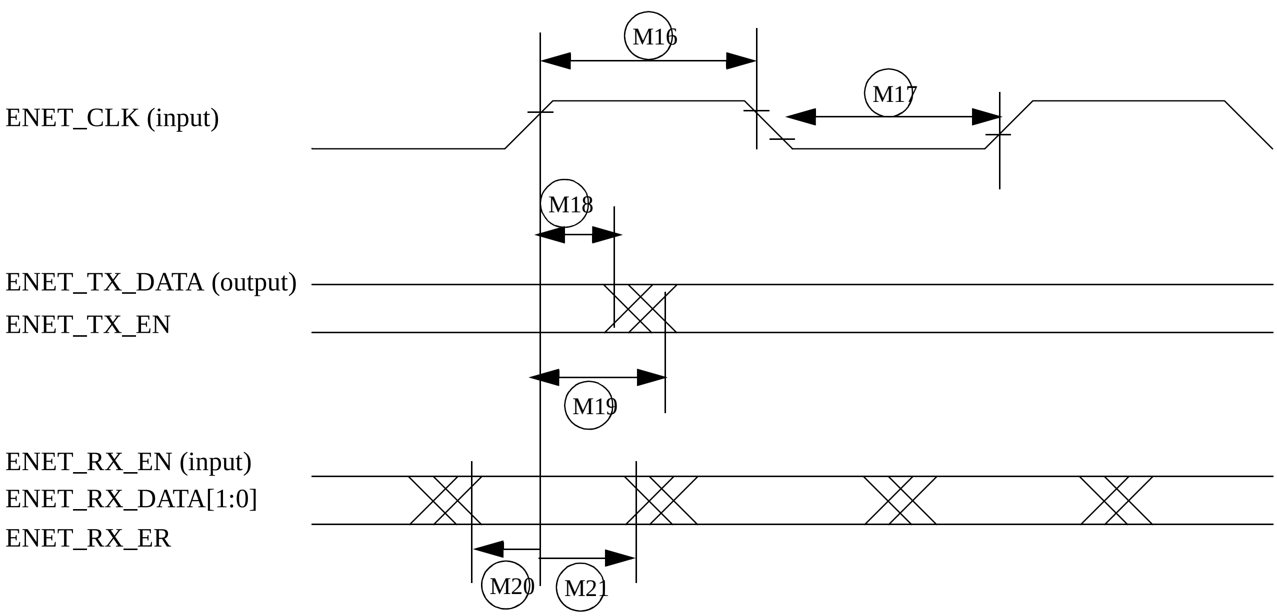


Figure 55. RMII mode signal timing diagram

Table 63. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	15	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.10.3.3 Signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 64. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

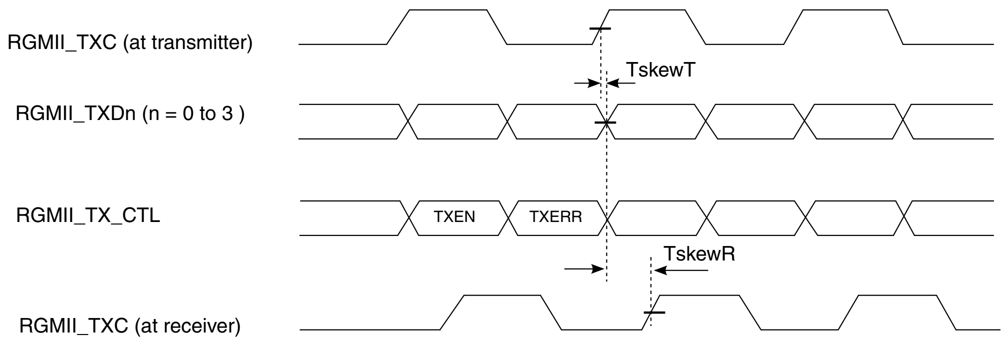


Figure 56. RGMII transmit signal timing diagram original

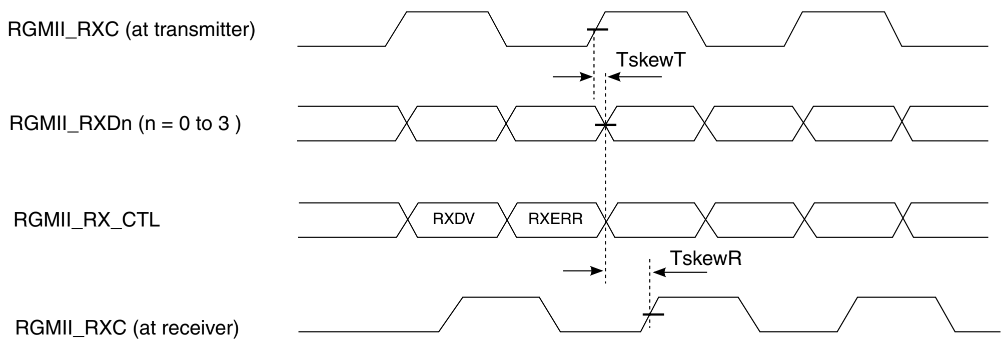


Figure 57. RGMII receive signal timing diagram original

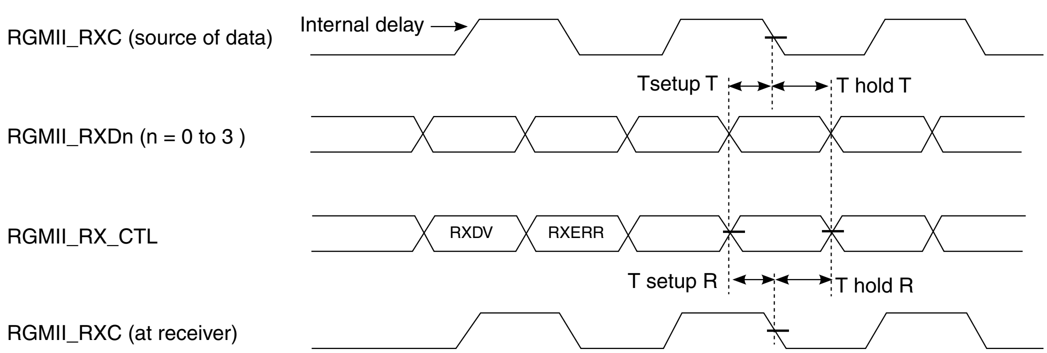


Figure 58. RGMII receive signal timing diagram with internal delay

4.10.4 Flexible controller area network (flexcan) ac electrical specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0 B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.10.5 I²C module timing parameters

This section describes the timing parameters of the I²C module. Figure 59 depicts the timing of I²C module, and Table 65 lists the I²C module timing characteristics.

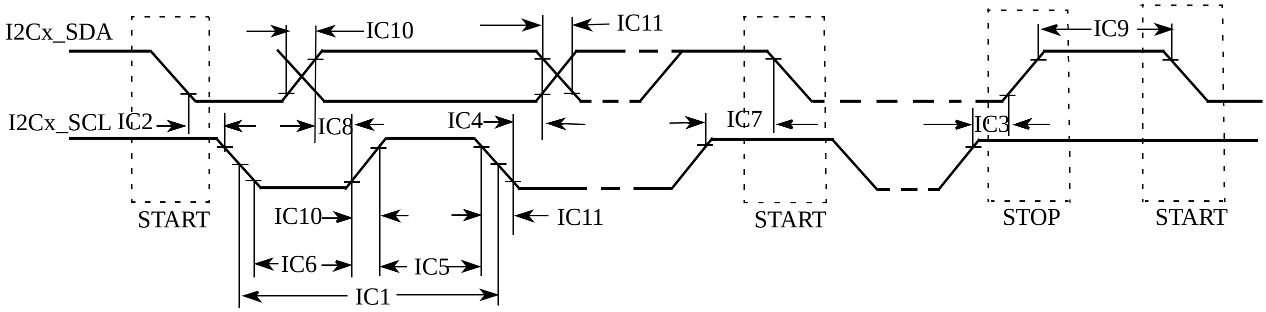


Figure 59. I²C bus timing

Table 65. I²C module timing parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.10.6 LCD controller (LCDIF) timing parameters

Figure 60 shows the LCDIF timing and Table yy lists the timing parameters.

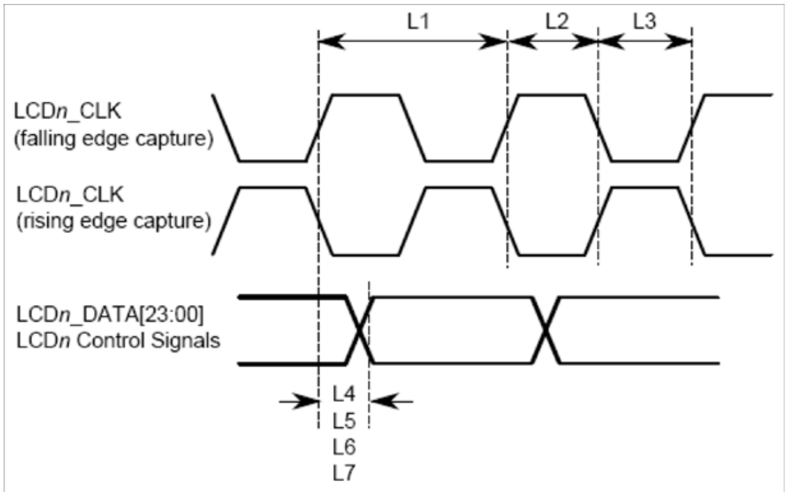


Figure 60. LCD timing

Table 66. LCD timing parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	-	150	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	-	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	-	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signals valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signals valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.10.7 Parallel CMOS sensor interface (CSI) timing parameters

4.10.7.1 Gated clock mode timing

Figure 61 and Figure 62 shows the gated clock mode timings for CSI, and Table 67 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

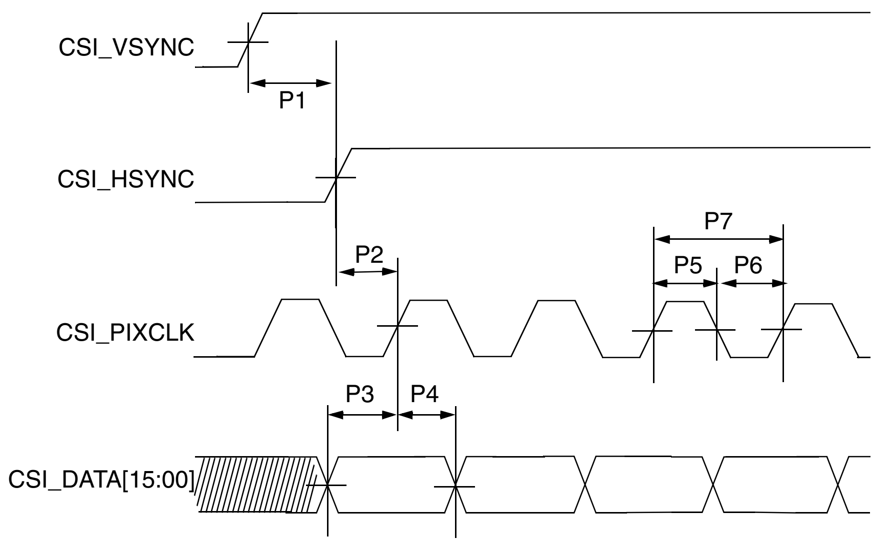


Figure 61. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

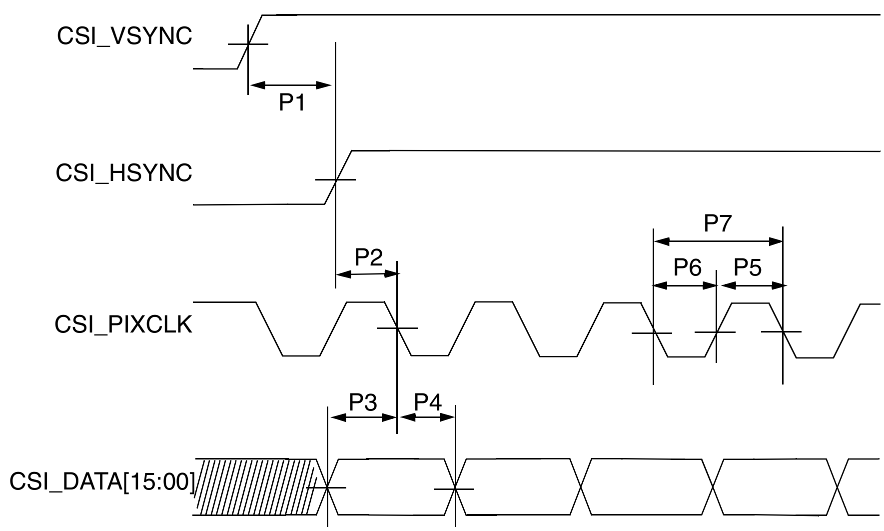


Figure 62. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 67. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns

Table 67. CSI Gated Clock Mode Timing Parameters(continued)

ID	Parameter	Symbol	Min.	Max.	Units
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns
P6	CSI pixel clock low time	tCLKl	3.75	—	ns
P7	CSI pixel clock frequency	fCLK	—	148.5	MHz

4.10.7.2 Ungated clock mode timing

Figure 63 shows the ungated clock mode timings of CSI, and Table 68 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

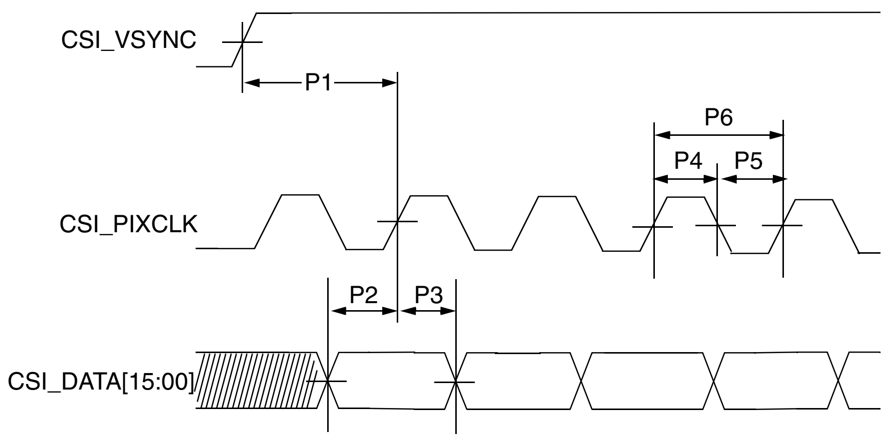


Figure 63. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 68. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	33.5	—	ns
P2	CSI DATA setup time	tDsu	1	—	ns
P3	CSI DATA hold time	tDh	1	—	ns
P4	CSI pixel clock high time	tCLKh	3.75	—	ns
P5	CSI pixel clock low time	tCLKl	3.75	—	ns
P6	CSI pixel clock frequency	fCLK	—	148.5	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.10.8 MIPI PHY timing parameters

This section describes MIPI PHY electrical specifications, which are designed to be compatible with the following:

- MIPI-CSI-2 version 1.0 and PHY specification Rev. 1.0 (for MIPI sensor port x2 lanes)
- MIPI DSI Version 1.01 and PHY specification Rev. 1.0 (as well as DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes)

4.10.8.1 Electrical and Timing Information

Table 69. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Input DC Specifications - Apply to DSI_CLK_P/DSI_CLK_N and DSI_DATA_P/DSI_DATA_N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV
V_{LEAK}	Input leakage current	VGNDSH(min) = VI = VGNDSH(max) + VOH(absmax) Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level	—	—	—	1.45	V
$t_{voh(absmax)}$	Maximum transient time above VOH(absmax)	—	—	—	20	ns
HS Line Drivers DC Specifications						
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω<= RL< = 125 Ω	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω<= RL< = 125 Ω	—	—	10	mV
V_{CMTX}	Steady-state common-mode output voltage.	80 Ω<= RL< = 125 Ω	150	200	250	mV
$\Delta V_{CMTX}(1,0)$	Changes in steady-state common-mode output voltage between logic states	80 Ω<= RL< = 125 Ω	—	—	5	mV
V_{OHHS}	HS output high voltage	80 Ω<= RL< = 125 Ω	—	—	360	mV
Z_{OS}	Single-ended output impedance.	—	40	50	62.5	Ω

Table 69. Electrical and Timing Information(continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
ΔZ_{OS}	Single-ended output impedance mismatch.	—	—	—	10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage	—	-50		50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.	—	110	—	—	Ω
$\Delta Z_{OLP(01-10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$\Delta Z_{OLP(0-11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold	—	—	—	70	mV
V_{IDTL}	Differential input low voltage threshold	—	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	—	460	mV
V_{ILHS}	Single ended input low voltage	—	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	—	70	—	330	mV
Z_{ID}	Differential input impedance	—	80	—	125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

4.10.8.2 MIPI PHY signaling levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 64 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

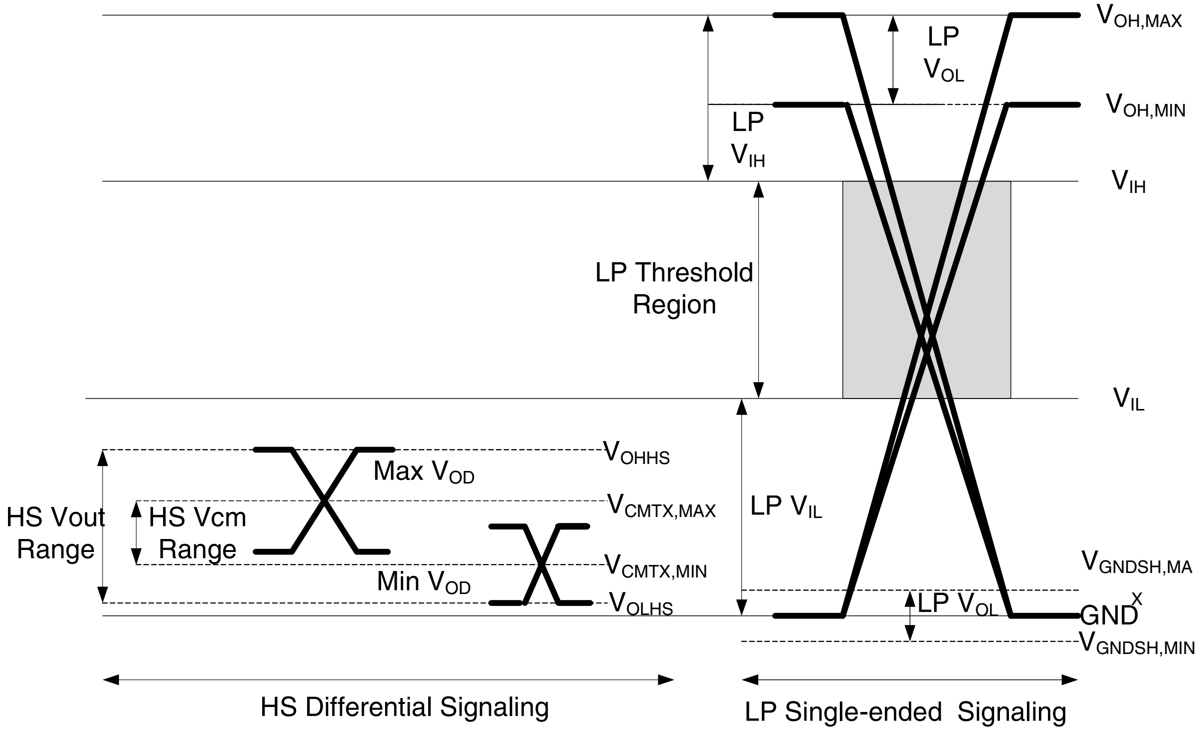


Figure 64. MIPI PHY Signaling Levels

4.10.8.3 MIPI HS line driver characteristics

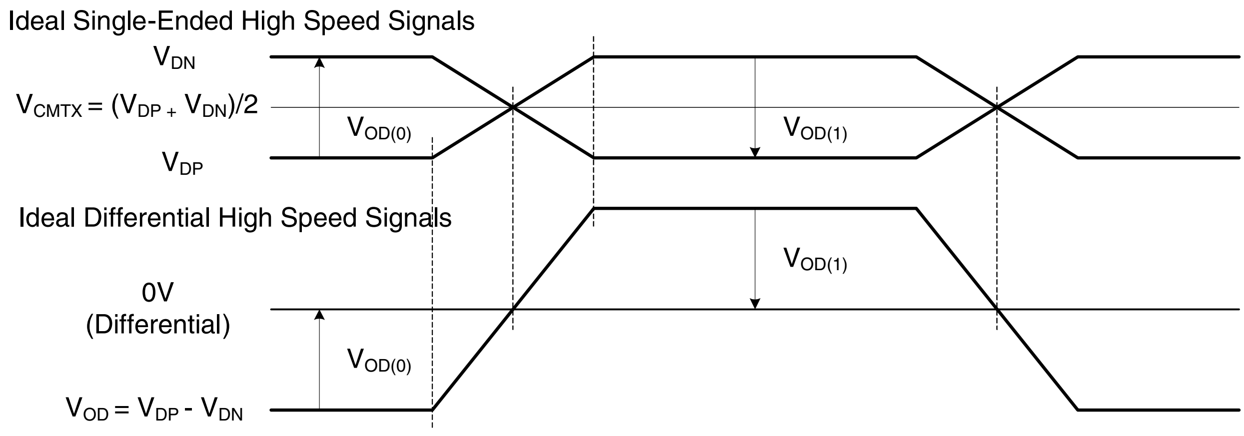


Figure 65. Ideal Single-ended and Resulting Differential HS Signals

4.10.8.4 Possible ∆VCMTX and ∆VOD Distortions of the Single-ended HS Signals

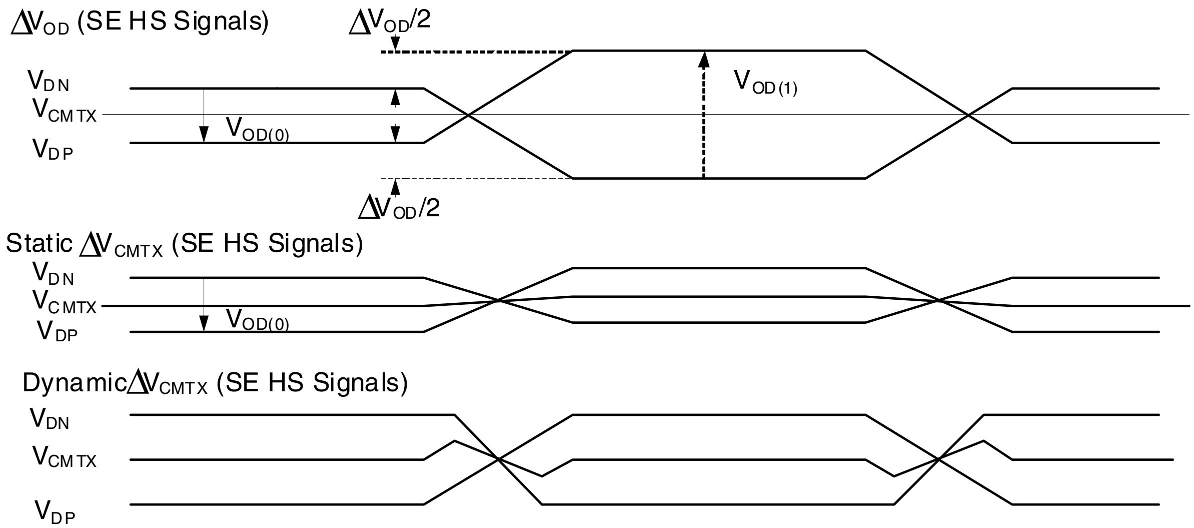


Figure 66. Possible ∆VCMTX and ∆VOD Distortions of the Single-ended HS Signals

4.10.8.5 MIPI PHY switching characteristics

Table 70. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω <= RL <= 125 Ω	80	—	1500	Mbps
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	750	MHz
P_{DDRCLK}	DDR CLK period	80 Ω<= RL< = 125 Ω	1.33	—	25	ns
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time	—	—	1	—	UI
t_{CPL}	DDR CLK low time	—	—	1	—	UI
—	DDR CLK / DATA Jitter	—	—	75	—	ps pk–pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew	—	—	0.075	—	UI
$t_{SKEW[TX]}$	Data to Clock Skew	—	0.350	—	0.650	UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω	—	—	15	mV_{rms}
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω	—	—	25	mV_p

Table 70. Electrical and Timing Information(continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
LP Line Drivers AC Specifications						
t_{rlp},t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}		30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—		—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—		ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.	—	—	—	1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.	—	—	—	2	pF
L_S	Equivalent wire bond series inductance	—	—	—	1.5	nH
R_S	Equivalent wire bond series resistance	—	—	—	0.15	Ω
R_L	Load resistance	—	80	100	125	Ω

4.10.8.6 High-speed clock timing

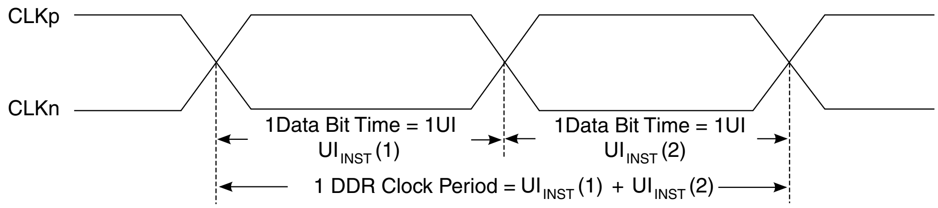


Figure 67. DDR Clock Definition

4.10.8.7 Forward high-speed data transmission timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 68:

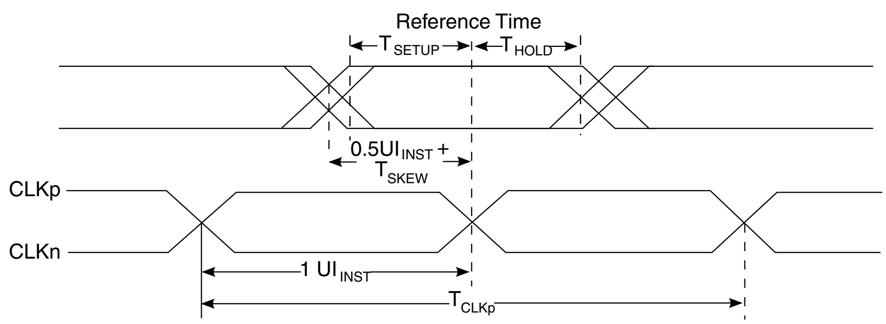


Figure 68. Data to Clock Timing Definitions

4.10.8.8 Reverse high-speed data transmission timing

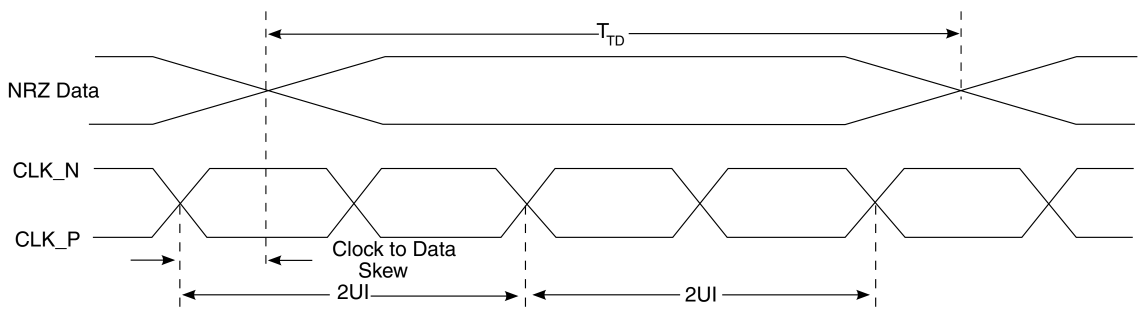
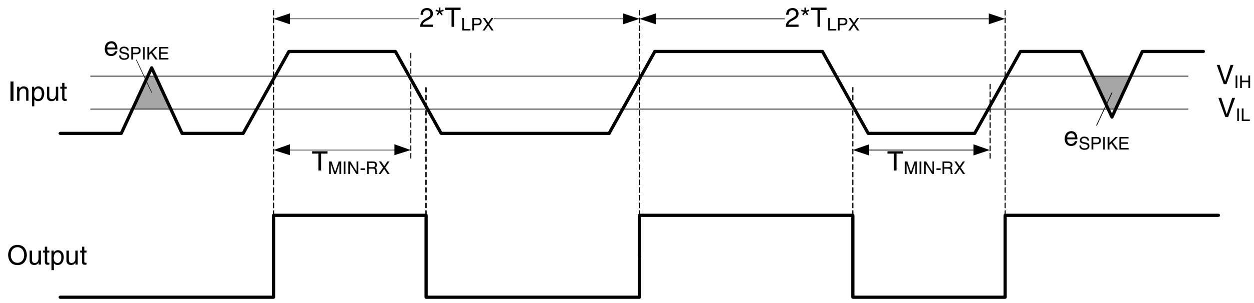


Figure 69. Reverse High-Speed Data Transmission Timing at Slave Side

4.10.8.9 Low-power receiver timing



Input Glitch Rejection of Low-Power Receivers

4.10.9 Pulse width modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 70 depicts the timing of the PWM, and Table 71 lists the PWM timing parameters.

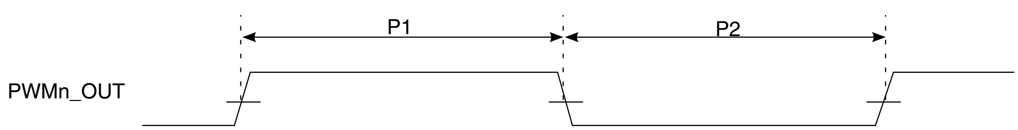


Figure 70. PWM Timing

Table 71. PWM output timing parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15		ns
P2	PWM output pulse width low	15		ns

4.10.10 QUAD SPI (QSPI) Timing Parameters

Measurement conditions are with 35 pF load on SCK and SIO pins and input slew rate of 1 V/ns.

4.10.10.1 SDR Mode

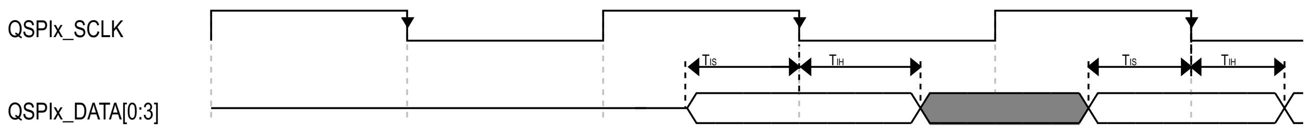


Figure 71. QuadSPI Input/Read Timing (SDR mode with internal sampling)

Table 72. QuadSPI Input Timing (SDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

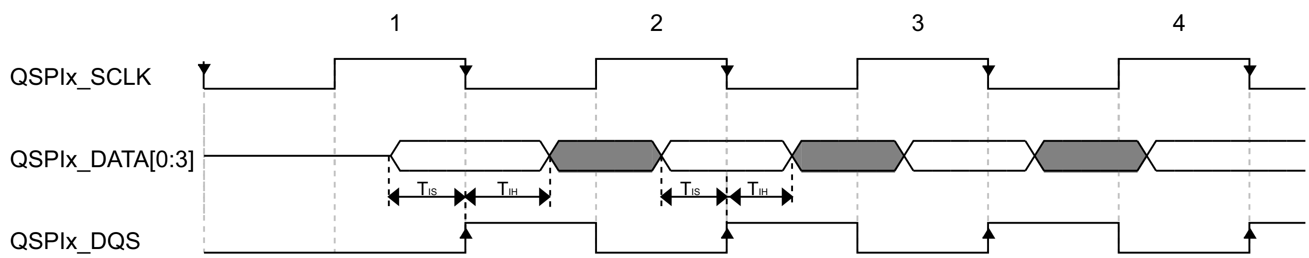


Figure 72. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Table 73. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

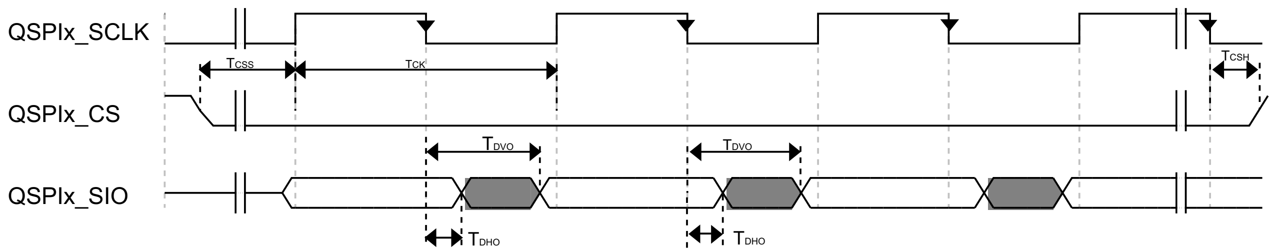


Figure 73. QuadSPI Output/Write Timing (SDR mode)

Table 74. QuadSPI Output/Write Timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	2.5	ns
T_{DHO}	Output data hold time	-0.5	—	ns
T_{CK}	SCK clock period	10	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6SoloX Reference Manual (IMX6ULLRM)* for more details.

4.10.10.2 DDR Mode

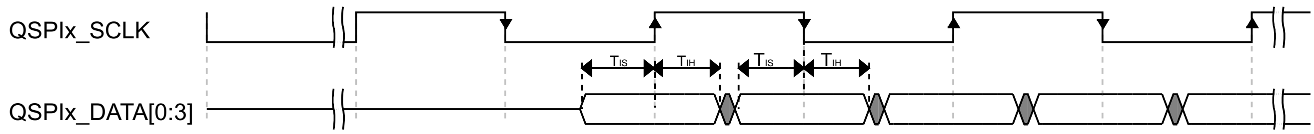


Figure 74. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 75. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

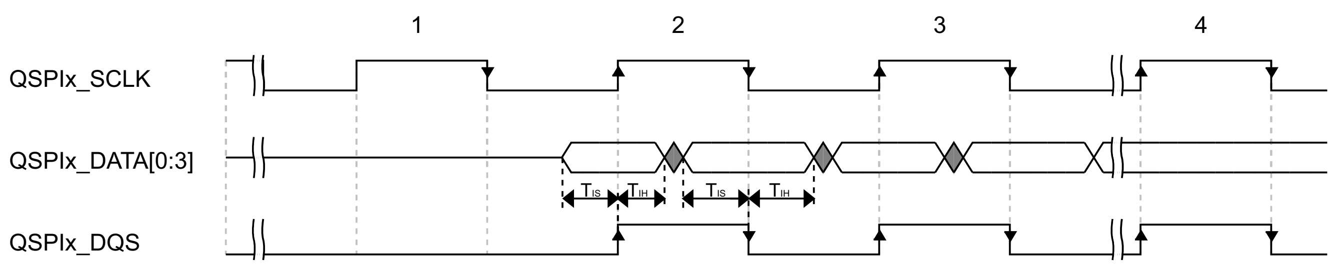


Figure 75. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Table 76. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

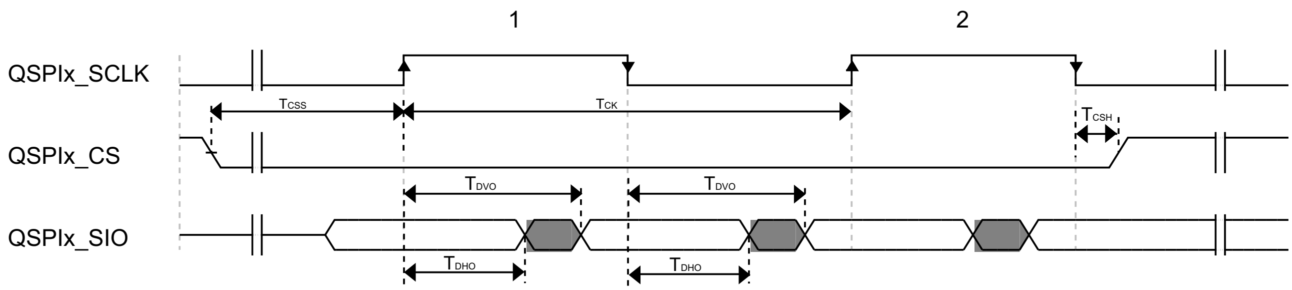


Figure 76. QuadSPI Output/Write Timing (DDR mode)

Table 77. QuadSPI Output/Write Timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	(0.25 x T_{SCLK}) + 2.5	ns
T_{DHO}	Output data hold time	(0.25 x T_{SCLK}) - 0.5	—	ns
T_{CK}	SCK clock period	20	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6SoloX Reference Manual (IMX6ULLRM)* for more details.

4.10.11 *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM)*i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) SAI/I^{2}S switching specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for noninverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and noninverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 78. Master mode SAI timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	20	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns

Table 78. Master mode SAI timing(continued)

Num	Characteristic	Min	Max	Unit
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

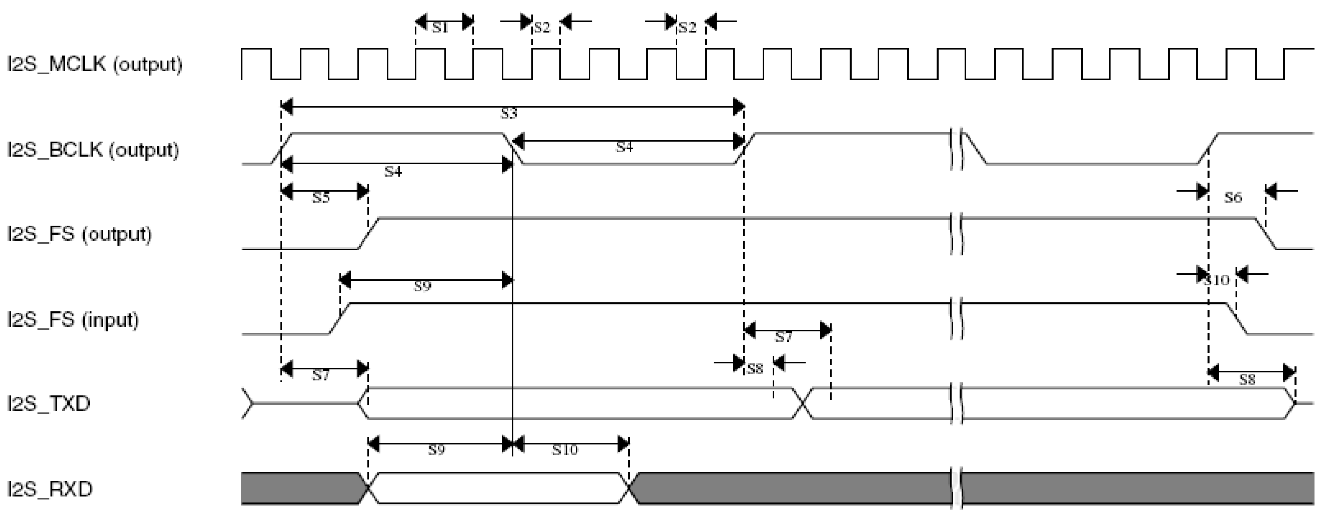


Figure 77. SAI timing — master modes

Table 79. Master mode SAI timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

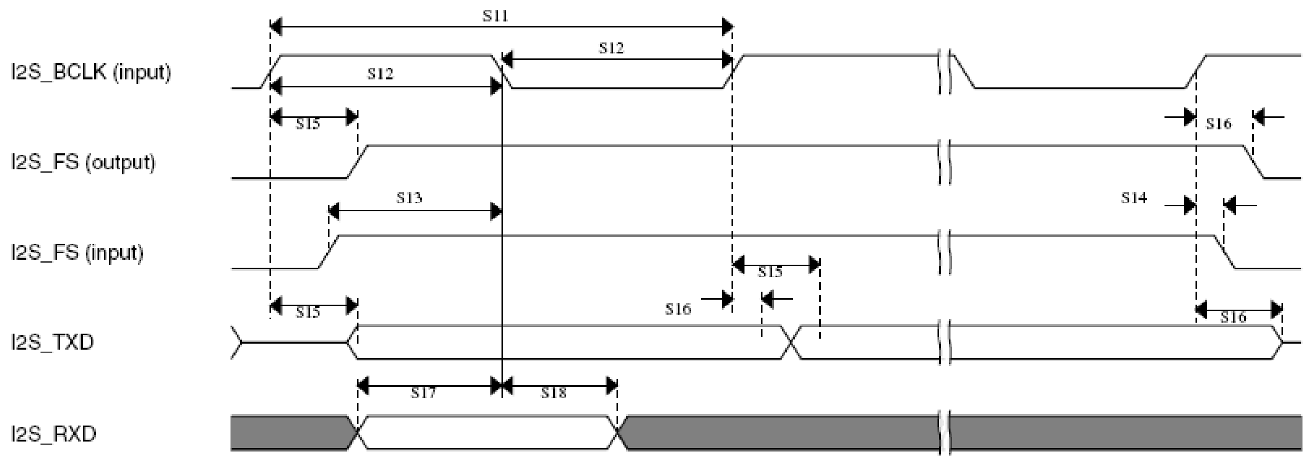


Figure 78. SAI timing — slave modes

4.10.12 SCAN JTAG controller (SJC) timing parameters

Figure 79 depicts the SJC test clock input timing. Figure 80 depicts the SJC boundary scan timing. Figure 81 depicts the SJC test access port. Signal parameters are listed in Table 80.

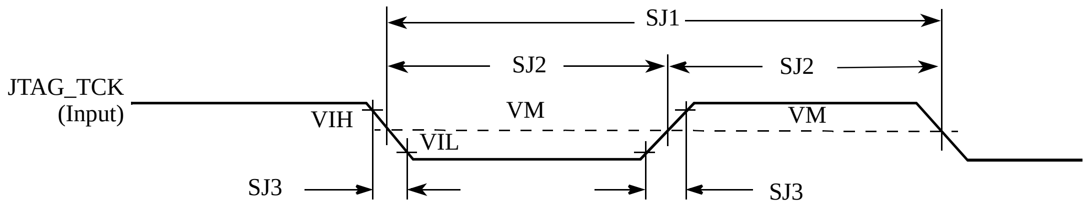


Figure 79. Test clock input timing diagram

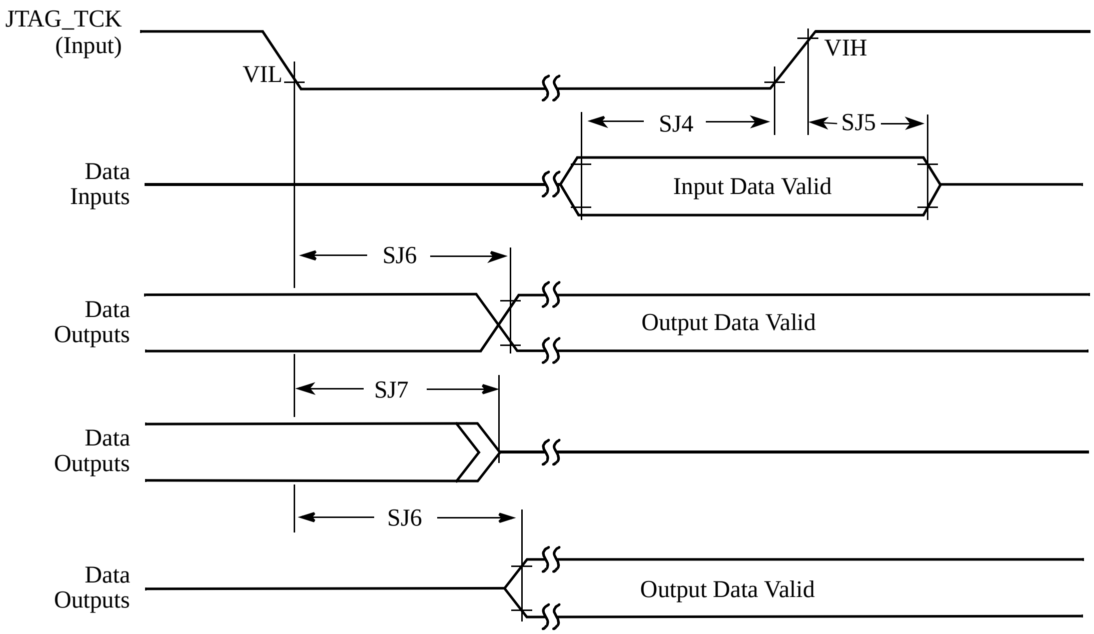


Figure 80. Boundary scan (JTAG) timing diagram

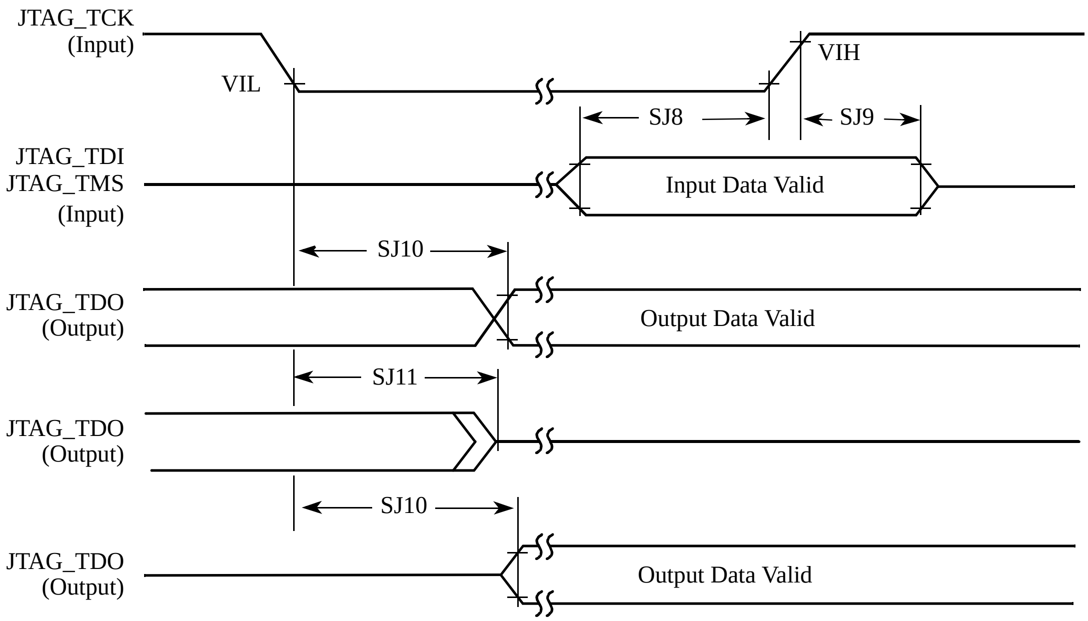


Figure 81. Test access port timing diagram

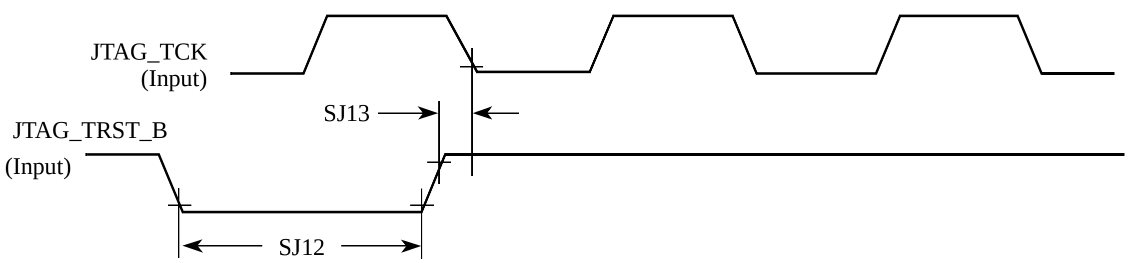


Figure 82. JTAG_TRST_B timing diagram

Table 80. JTAG timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in Crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns

Table 80. JTAG timing(continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.10.13 UART I/O configuration and timing parameters

4.10.13.1 UART RS-232 I/O configuration in different modes

The i.MX 7Solo UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 81 shows the UART I/O configuration based on the enabled mode.

Table 81. UART I/O configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.10.13.2 UART RS-232 Serial mode timing

This section describes the electrical information of the UART module in the RS-232 mode.

4.10.13.2.1 UART transmitter

Figure 83 depicts the transmit timing of UART in the RS-232 Serial mode, with 8 data bit/1 stop bit format. Table 82 lists the UART RS-232 Serial mode transmit timing characteristics.

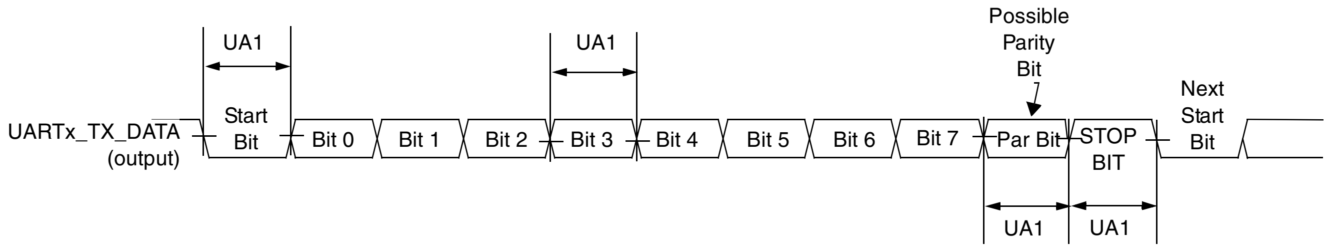


Figure 83. UART RS-232 Serial mode transmit timing diagram

Table 82. RS-232 Serial mode transmit timing parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.
2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.10.13.2.2 UART receiver

Figure 84 depicts the RS-232 Serial mode receive timing with 8 data bit/1 stop bit format. Table 83 lists Serial mode receive timing characteristics.

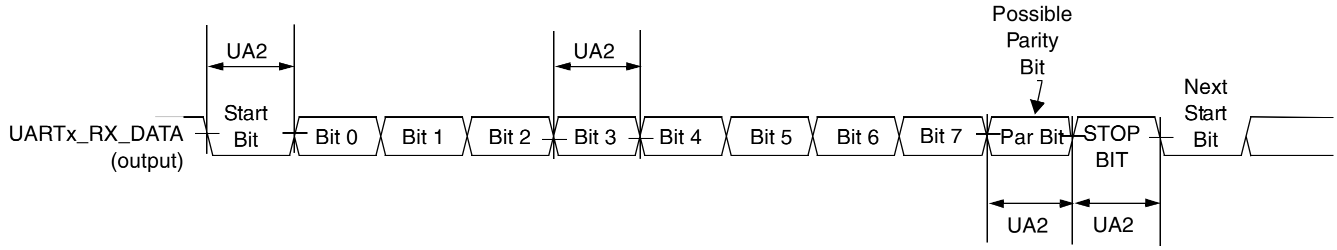


Figure 84. UART RS-232 Serial mode receive timing diagram

Table 83. RS-232 Serial mode receive timing parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - 1/(16 x F_{baud_rate})	$1/F_{baud\_rate}$ + 1/(16 x F_{baud_rate})	—

1 The UART receiver can tolerate 1/(16 x F_{baud_rate}) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16 x F_{baud_rate}).
2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.14 USB HSIC timing

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.10.14.1 Transmit timing

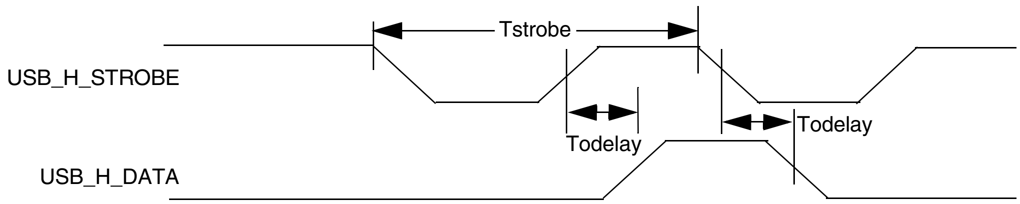


Figure 85. USB HSIC transmit waveform

Table 84. USB HSIC transmit parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.165	4.169	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.10.14.2 Receive timing

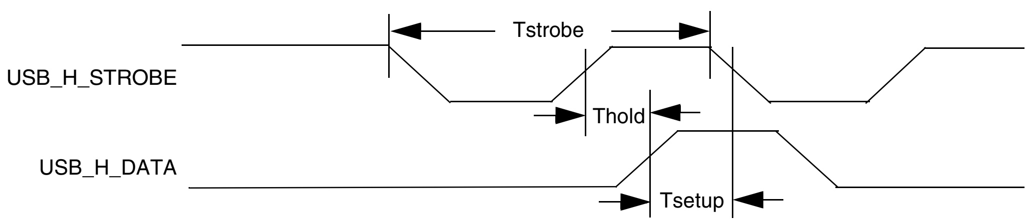


Figure 86. USB HSIC receive waveform

Table 85. USB HSIC receive parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.165	4.169	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.15 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port):

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0, version 1.1a, July 27, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

4.10.15.1 USB_OTG*_REXT reference resistor connection

The bias generation and impedance calibration process for the USB OTG PHYs requires connection of reference resistors 200 Ω 1% precision on each of USB_OTG1_REXT and USB_OTG2_REXT pads to ground.

4.10.15.2 USB_OTG_CHD_B USB battery charger detection external pullup resistor connection

The usage and external resistor connection for the USB_OTG_CHD_B pin are described in Table 3, Table 7, and Section 4.7.3, “USB battery charger detection driver impedance.”

4.11 12-Bit A/D converter (ADC)

Table 86. Recommended operating conditions for 12-bit ADC

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD18	1.7	1.8	1.9	V
	VDDA10	0.95	1	1.05	V
Operating Temp	T_J	–25	—	105	C
Analog Input Channel	—	—	—	16	Channel
Analog Input Range[1]	ADC*x*_IN*x*	AGND	—	VREF	V
Main Clock Frequency	FCLK	300K	—	6M	Hz
Start of conversion clk frequency (FCLK/3)	FSOC	50K	—	1M	Hz
External Input Resistance of ADC[2]	R_{IEXT}	—	50	250	Ω

[1] DO=111111111111 @AIN=AVDD18 & DO=000000000000 @AIN=AVSS18 (Input full-scale voltage = AVDD18)

[2] R_{IEXT} = Output resistance of the ADC driver = Output resistance of signal generator + Series parasitic resistance between signal source and ADC input (for example, PCB and bonding wire resistance and ESD protection resistance)

Table 87. DC Electrical characteristics

Specification	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	—	—	12	12	Bits	—
Differential Non-Linearity	DNL	—	± 2.0	± 2.0	LSB	PD=Low FCLK=6MHz FSOC=1MHz FAIN=10kHz Ramp wave
Integral Non-Linearity	INL	—	± 6.0	± 6.0	LSB	
Top Offset Voltage	EOT	—	±10	± 100	LSB	
Bottom Offset Voltage	EOB	—	±11	± 100	LSB	

Table 88. AC Electrical characteristics

Specification	Symbol	Min	Typ	Max	Unit
Main Clock Duty Ratio	—	45	45	55	%
Analog Input Frequency CH #15-0	FAIN	DC	50k	100K	Hz
Normal Operation Current Consumption[1]	VDDA_ADCx_1P8[2]	—	0.53	1.90	mA
	VDDA_1P0_CAP[2]	—	0.02	0.10	mA

Table 88. AC Electrical characteristics(continued)

Specification	Symbol	Min	Typ	Max	Unit
Power Down Current[2]	IPD[3]	—	3.0	300	µA
Signal to Noise and Distortion Ratio	SNDR	54	60	—	dB

1 Normal operation current consumption includes only the current from the ADC core. It does not include static current from the power pads.

2 Power-down current includes only the current from the ADC core. It does not include static current from the power pads.

3 IOP and IPD are measurable only on the ADC core's test chips. Because AVDD10 is shared with internal logic power, IOP and IPD in the test plan only measure current consumption @ AVDD18, VREF.

5 Boot mode configuration

This section provides information on Boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot mode configuration pins

Table 89 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is ‘0’ (cleared, which is the case for an unblown fuse). For detailed Boot mode options configured by the Boot mode pins, see the “System Boot, Fusemap, and eFuse” chapter in the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM).

Table 89. Fuses and associated pins used for boot

Pin	Direction at Reset	eFuse name	State during reset (POR_B asserted)	State after reset (POR_B deasserted)	Details
BOOT_MODE0	Input	N/A	Hi-Z	Hi-Z	Boot mode selection
BOOT_MODE1	Input	N/A	Hi-Z	Hi-Z	Boot mode selection

Table 89. Fuses and associated pins used for boot(continued)

Pin	Direction at Reset	eFuse name	State during reset (POR_B asserted)	State after reset (POR_B deasserted)	Details
LCD1_DATA00	Input	BT_CFG[0]	100K Pull Down	Keeper	Boot options, pin value overrides fuse settings for BT_FUSE_SEL='0'. Signal configuration as fuse override input at power up. These are special I/O lines that control the boot configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD1_DATA01	Input	BT_CFG[1]	100K Pull Down	Keeper	
LCD1_DATA02	Input	BT_CFG[2]	100K Pull Down	Keeper	
LCD1_DATA03	Input	BT_CFG[3]	100K Pull Down	Keeper	
LCD1_DATA04	Input	BT_CFG[4]	100K Pull Down	Keeper	
LCD1_DATA05	Input	BT_CFG[5]	100K Pull Down	Keeper	
LCD1_DATA06	Input	BT_CFG[6]	100K Pull Down	Keeper	
LCD1_DATA07	Input	BT_CFG[7]	100K Pull Down	Keeper	
LCD1_DATA08	Input	BT_CFG[8]	100K Pull Down	Keeper	
LCD1_DATA09	Input	BT_CFG[9]	100K Pull Down	Keeper	
LCD1_DATA10	Input	BT_CFG[10]	100K Pull Down	Keeper	
LCD1_DATA11	Input	BT_CFG[11]	100K Pull Down	Keeper	
LCD1_DATA12	Input	BT_CFG[12]	100K Pull Down	Keeper	
LCD1_DATA13	Input	BT_CFG[13]	100K Pull Down	Keeper	
LCD1_DATA14	Input	BT_CFG[14]	100K Pull Down	Keeper	
LCD1_DATA15	Input	BT_CFG[15]	100K Pull Down	Keeper	
LCD1_DATA16	Input	BT_CFG[16]	100K Pull Down	Keeper	
LCD1_DATA17	Input	BT_CFG[17]	100K Pull Down	Keeper	
LCD1_DATA18	Input	BT_CFG[18]	100K Pull Down	Keeper	
LCD1_DATA19	Input	BT_CFG[19]	100K Pull Down	Keeper	

5.2 Boot device interface allocation

Table 90 lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 90. Interface allocation during boot

Interface	IP Instance	Allocated Pads During Boot	Comment
QSPI	QSPI	EPDC_D0, EPDC_D1, EPDC_D2, EPDC_D3, EPDC_D4, EPDC_D5, EPDC_D6, EPDC_D7, EPDC_D8, EPDC_D9, EPDC_D10, EPDC_D11, EPDC_D12, EPDC_D13, EPDC_D14, EPDC_D15	
SPI	ECSPI-1	ECSPI1_SCLK, ECSPI1_MOSI, ECSPI1_MISO, ECSPI1_SS0, UART1_RXD, UART1_TXD, UART2_RXD	The chip-select pin used depends on the fuse "CS select (SPI only)"

Table 90. Interface allocation during boot(continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-2	ECSPI2_SCLK, ECSPI2_MOSI, ECSPI2_MISO, ECSPI2_SS0, ENET1_RX_CTL, ENET1_RXC, ENET1_TD0	The chip-select pin used depends on the fuse "CS select (SPI only)"
SPI	ECSPI-3	SAI2_TXFS, SAI2_TXC, SAI2_RXD, SAI2_TXD, SD1_DATA3, SD2_CD_B, SD2_WP	The chip-select pin used depends on the fuse "CS select (SPI only)"
SPI	ECSPI-4	SD1_CD_B, SD1_WP, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_DATA0, SD1_DATA1	The chip-select pin used depends on the fuse "CS select (SPI only)"
EIM	EIM	EPDC_SDCE2, EPDC_SDCE3, EPDC_GDCLK, EPDC_GDOE, EPDC_GDRL, EPDC_GDSP, EPDC_BDR0, LCD_DAT20, LCD_DAT21, LCD_DAT22, LCD_DAT23, EPDC_D8, EPDC_D9, EPDC_D10, EPDC_D12, EPDC_D14, EPDC_PWRSTAT	Used for NOR, OneNAND boot Only CS0 is supported. Allocated pads may differ depending on mux mode. See the “System Boot, Fusemap, and eFuse” chapter of the *i.MX 7Solo Application Processor Reference Manual* (IMX7SRM) for details.
NAND Flash	GPMI	SD3_CLK, SD3_CMD, SD3_DATA0, SD3_DATA1, SD3_DATA2, SD3_DATA3, SD3_DATA4, SD3_DATA5, SD3_DATA6, SD3_DATA7, SD3_STROBE, SD3_RESET_B, SAI1_TXC, SAI1_TXFS, SAI1_TXD	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CD_B, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_DATA0, SD1_DATA1, SD1_DATA2, SD1_DATA3, GPIO1_IO08, ECSPI2_SCLK, ECSPI2_MOSI, ECSPI2_MISO, ECSPI2_SS0	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_RESET_B, SD2_CLK, SD2_CMD, SD2_DATA0, SD2_DATA1, SD2_DATA2, SD2_DATA3, GPIO1_IO12, ECSPI1_SCLK, ECSPI1_MOSI, ECSPI1_MISO, ECSPI1_SS0	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, SD3_RESET_B	1, 4, or 8 bit
USB	USB-OTG PHY		—

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 12 x 12 mm package information

6.1.1 Case 1997-01, 12 x 12, 0.4 mm pitch, ball matrix

The following figure shows the top, bottom, and side views of the 12×12 mm BGA package.

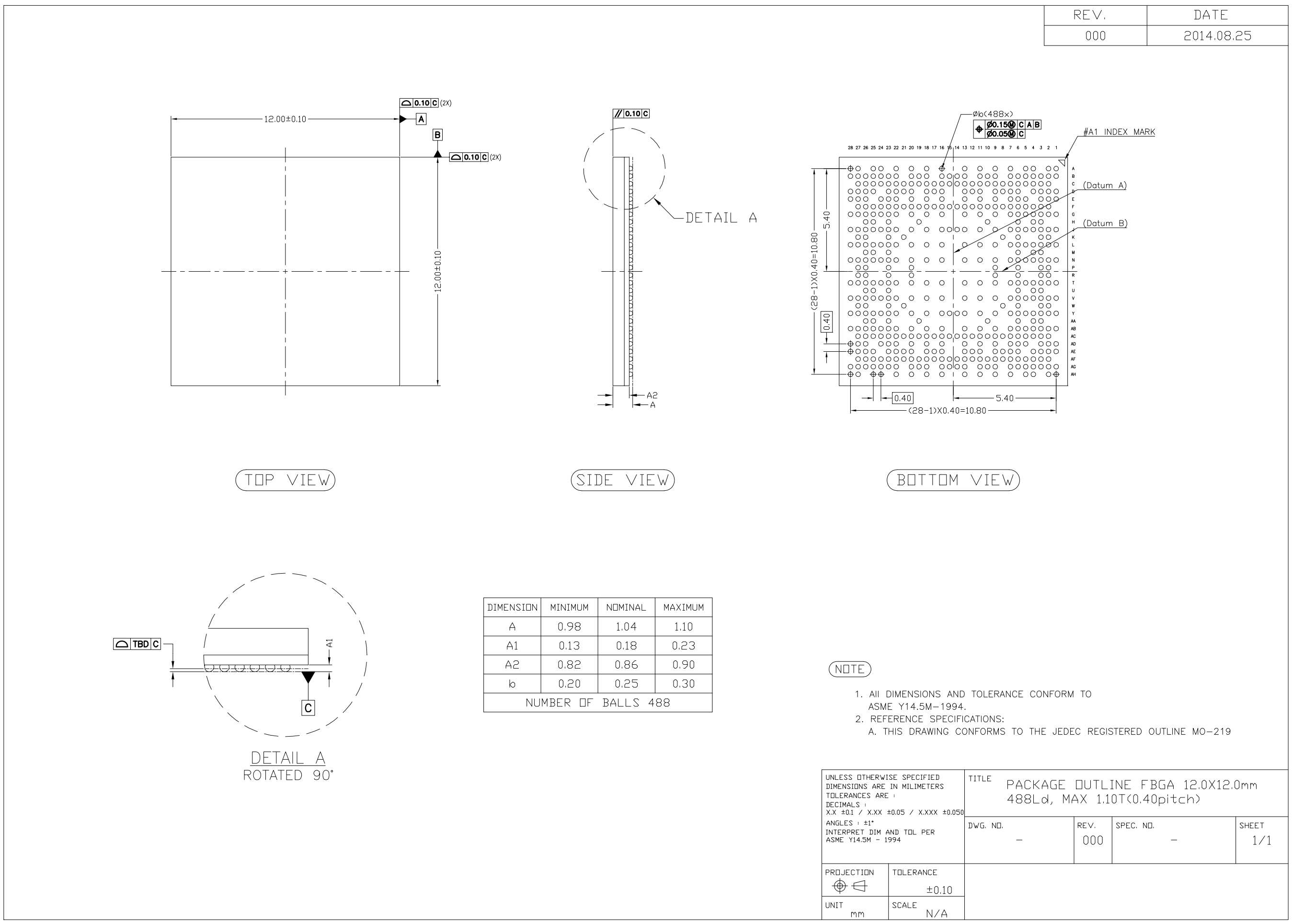


Figure 87. 12 x 12 mm BGA, Case x Package Top, Bottom, and Side Views

6.1.2 12 x 12 mm supplies contact assignments and functional contact assignments

Table 91 shows supplies contact assignments for the 12 x 12 mm package.

Table 91. i.MX 7Solo 12 x 12 mm supplies contact assignments

Supply Rail	Ball(s) position(s)	Remarks
DRAM_VREF	T20	DDR voltage reference input. Connect to a voltage source that is 50% of NVCC_DRAM
DRAM_ZQPAD	Y18	DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss
FUSE_FSOURCE	V09	
GND	A01,A28,B05,B23,B26,C03,C05,C07,C10,C13,C14,C15,C23,C24,C25,C26,D08,D11,D17,D21,E03,E05,E24,E26,F08,F09,F10,F12,F14,F15,F17,F21,H04,H06,H23,H25,L13,L16,M04,M06,M23,M25,N11,N18,T11,T18,U04,U06,U23,U25,V13,V16,W03,W06,Y16,AA04,AA06,AA23,AA25,AC08,AC10,AC12,AC14,AC15,AC17,AC21,AD03,AD05,AD06,AD24,AD26,AE06,AE07,AE08,AE09,AE17,AE21,AF03,AF05,AF08,AF09,AF10,AF11,AF13,AF14,AF15,AF24,AF26,AG10,AH01,AH28	
GPANAIO	AF02	Test signal. Should be left unconnected.
MIPI_VREG_0P4V	B19	
NVCC_DRAM	V27,V28,W21,W23,W26,Y20,AA19,AC19,AF17,AF18,AF19,AG18,AH18	Supply input for the DDR I/O interface
NVCC_DRAM_CKE	V20	
NVCC_ENET1	J18	Supply input for the ENET interfaces
NVCC_EPDC1	P20	Supply for EPDC
NVCC_EPDC2	N20	Supply for EPDC
NVCC_GPIO1	Y09	Supply for GPIO1
NVCC_GPIO2	Y11	Supply for GPIO2
NVCC_I2C	R09	Supply for I2C
NVCC_LCD	L20	Supply for LCD
NVCC_SAI	J13	Supply for SAI
NVCC_SD1	J11	Supply for SD card
NVCC_SD2	L09	Supply for SD card
NVCC_SD3	N09	Supply for SD card
NVCC_SPI	P09	Supply for SPI

Table 91. i.MX 7Solo 12 x 12 mm supplies contact assignments(continued)

Supply Rail	Ball(s) position(s)	Remarks
NVCC_UART	T09	Supply for UART
NC	A9, A11, B10, B11, C11, Y15, C11, AB13, AG11, AG13, AG14, AG15, AG16, AH11, AH13, AH16	NC
PVCC_ENET_CAP	G16	Secondary supply for ENET. Requires external capacitor
PVCC_EPDC_LCD_CAP	R20	Secondary supply for EPDC, LCD. Requires external capacitor
PVCC_GPIO_CAP	AB11	Secondary supply for GPIO. Requires external capacitor
PVCC_I2C_SPI_UART_CAP	W08	Secondary supply for I2C, SPI, UART. Requires external capacitor
PVCC_SAI_SD_CAP	J14	Secondary supply for SAI, SD. Requires external capacitor
USB_OTG1_VBUS	C09	VBUS input for USB_OTG1
VDD_1P2_CAP	AA10	Supply for HSIC
VDD_ARM	A20,B20,C16,C17,C18,C19,C20,C21,C22,F19,H19,J20,K21,K23,K26,L27,L28	Supply voltage for ARM
VDD_LPSR_1P0_CAP	AG06	Secondary supply for LPSR. Requires external capacitor
VDD_LPSR_IN	AG05	Supply to LPSR
VDD_MIPI_1P0	J16	Supply for MIPI
VDD_SNVS_1P8_CAP	AG07	Secondary supply for SNVS. Requires external capacitor
VDD_SNVS_IN	Y13	Supply for SNVS
VDD_SOC	H10,J09,K03,K06,K08,L01,L02,L11,L18,N13,N16,P03,P06,P23,P26,R26,T13,T16,V11,V18,R03,R06,R23	Supply for SOC
VDD_TEMPSENSOR_1P8	AH05	Supply for temp sensor
VDD_USB_H_1P2	C12,G13	Supply input for the USB HSIC interface
VDD_USB_OTG1_1P0_CAP	E09	Secondary supply for OTG1. Requires external capacitor
VDD_USB_OTG1_3P3_IN	D09	Secondary supply for OTG1. Requires external capacitor
VDD_XTAL_1P8	AH02	
VDDA_1P0_CAP	AH07	Secondary supply for 1.0 V. Requires external capacitor
VDDA_1P8_IN	AF04,AG03,AG04	Supply for 1.8 V
VDDA_ADC1_1P8	AH04	Supply for ADC

Table 91. i.MX 7Solo 12 x 12 mm supplies contact assignments(continued)

Supply Rail	Ball(s) position(s)	Remarks
VDDA_MIPI_1P8	J15	Supply for MIPI
VDDA_PHY_1P8	Y14	
VDDD_1P0_CAP	AC13,AE12,AF12	Secondary supply for 1.0 V. Requires external capacitor

Table 92 shows an alpha-sorted list of functional contact assignments for the 12 x 12 mm package.

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
AB07	ADC1_IN0	ADC1_VDDA_1P8			ADC1_IN0	
AC07	ADC1_IN1	ADC1_VDDA_1P8			ADC1_IN1	
AD07	ADC1_IN2	ADC1_VDDA_1P8			ADC1_IN2	
AD09	ADC1_IN3	ADC1_VDDA_1P8			ADC1_IN3	
Y01	BOOT_MODE0	NVCC_GPIO1		ALT0	BOOT_MODE0	100K PD
Y02	BOOT_MODE1	NVCC_GPIO1		ALT0	BOOT_MODE1	100K PD
AE04	CCM_CLK1_N	VDDA_1P8			CCM_CLK1_N	
AE03	CCM_CLK1_P	VDDA_1P8			CCM_CLK1_P	
AE02	CCM_CLK2	VDDA_1P8			CCM_CLK2	
AC24	DRAM_ADDR00	NVCC_DRAM	DDR		DRAM_ADDR00	
AC25	DRAM_ADDR01	NVCC_DRAM	DDR		DRAM_ADDR01	
AC26	DRAM_ADDR02	NVCC_DRAM	DDR		DRAM_ADDR02	
AB25	DRAM_ADDR03	NVCC_DRAM	DDR		DRAM_ADDR03	
AB24	DRAM_ADDR04	NVCC_DRAM	DDR		DRAM_ADDR04	
AE23	DRAM_ADDR05	NVCC_DRAM	DDR		DRAM_ADDR05	
AF23	DRAM_ADDR06	NVCC_DRAM	DDR		DRAM_ADDR06	
AE22	DRAM_ADDR07	NVCC_DRAM	DDR		DRAM_ADDR07	
AD22	DRAM_ADDR08	NVCC_DRAM	DDR		DRAM_ADDR08	
AC22	DRAM_ADDR09	NVCC_DRAM	DDR		DRAM_ADDR09	
AD23	DRAM_ADDR10	NVCC_DRAM	DDR		DRAM_ADDR10	
AG27	DRAM_ADDR11	NVCC_DRAM	DDR		DRAM_ADDR11	
AE27	DRAM_ADDR12	NVCC_DRAM	DDR		DRAM_ADDR12	
AG28	DRAM_ADDR13	NVCC_DRAM	DDR		DRAM_ADDR13	
AE20	DRAM_ADDR14	NVCC_DRAM	DDR		DRAM_ADDR14	

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
AG26	DRAM_ADDR15	NVCC_DRAM	DDR		DRAM_ADDR15	
AG25	DRAM_CAS_B	NVCC_DRAM	DDR		DRAM_CAS_B	
AE26	DRAM_CS0_B	NVCC_DRAM	DDR		DRAM_CS0_B	
AC23	DRAM_CS1_B	NVCC_DRAM	DDR		DRAM_CS1_B	
AH22	DRAM_DATA00	NVCC_DRAM	DDR		DRAM_DATA00	
AG19	DRAM_DATA01	NVCC_DRAM	DDR		DRAM_DATA01	
AG20	DRAM_DATA02	NVCC_DRAM	DDR		DRAM_DATA02	
AF22	DRAM_DATA03	NVCC_DRAM	DDR		DRAM_DATA03	
AF20	DRAM_DATA04	NVCC_DRAM	DDR		DRAM_DATA04	
AG22	DRAM_DATA05	NVCC_DRAM	DDR		DRAM_DATA05	
AF21	DRAM_DATA06	NVCC_DRAM	DDR		DRAM_DATA06	
AH20	DRAM_DATA07	NVCC_DRAM	DDR		DRAM_DATA07	
AC18	DRAM_DATA08	NVCC_DRAM	DDR		DRAM_DATA08	
AB18	DRAM_DATA09	NVCC_DRAM	DDR		DRAM_DATA09	
AD16	DRAM_DATA10	NVCC_DRAM	DDR		DRAM_DATA10	
AC16	DRAM_DATA11	NVCC_DRAM	DDR		DRAM_DATA11	
AD18	DRAM_DATA12	NVCC_DRAM	DDR		DRAM_DATA12	
AE18	DRAM_DATA13	NVCC_DRAM	DDR		DRAM_DATA13	
AB16	DRAM_DATA14	NVCC_DRAM	DDR		DRAM_DATA14	
AE16	DRAM_DATA15	NVCC_DRAM	DDR		DRAM_DATA15	
W27	DRAM_DATA16	NVCC_DRAM	DDR		DRAM_DATA16	
Y27	DRAM_DATA17	NVCC_DRAM	DDR		DRAM_DATA17	
Y26	DRAM_DATA18	NVCC_DRAM	DDR		DRAM_DATA18	
Y28	DRAM_DATA19	NVCC_DRAM	DDR		DRAM_DATA19	
AA26	DRAM_DATA20	NVCC_DRAM	DDR		DRAM_DATA20	
AB26	DRAM_DATA21	NVCC_DRAM	DDR		DRAM_DATA21	
AB27	DRAM_DATA22	NVCC_DRAM	DDR		DRAM_DATA22	
AB28	DRAM_DATA23	NVCC_DRAM	DDR		DRAM_DATA23	
V23	DRAM_DATA24	NVCC_DRAM	DDR		DRAM_DATA24	
V22	DRAM_DATA25	NVCC_DRAM	DDR		DRAM_DATA25	
T23	DRAM_DATA26	NVCC_DRAM	DDR		DRAM_DATA26	
T22	DRAM_DATA27	NVCC_DRAM	DDR		DRAM_DATA27	

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
V24	DRAM_DATA28	NVCC_DRAM	DDR		DRAM_DATA28	
V25	DRAM_DATA29	NVCC_DRAM	DDR		DRAM_DATA29	
T25	DRAM_DATA30	NVCC_DRAM	DDR		DRAM_DATA30	
T24	DRAM_DATA31	NVCC_DRAM	DDR		DRAM_DATA31	
AH24	DRAM_DQM0	NVCC_DRAM	DDR		DRAM_DQM0	
AD20	DRAM_DQM1	NVCC_DRAM	DDR		DRAM_DQM1	
AD28	DRAM_DQM2	NVCC_DRAM	DDR		DRAM_DQM2	
Y25	DRAM_DQM3	NVCC_DRAM	DDR		DRAM_DQM3	
AF16	DRAM_ODT0	NVCC_DRAM	DDR		DRAM_ODT0	
AH25	DRAM_RAS_B	NVCC_DRAM	DDR		DRAM_RAS_B	
V26	DRAM_RESET	NVCC_DRAM_CKE	DDR		DRAM_RESET	
AE28	DRAM_SDBA0	NVCC_DRAM	DDR		DRAM_SDBA0	
AB22	DRAM_SDBA1	NVCC_DRAM	DDR		DRAM_SDBA1	
AF27	DRAM_SDBA2	NVCC_DRAM	DDR		DRAM_SDBA2	
Y22	DRAM_SDCKE0	NVCC_DRAM_CKE	DDR		DRAM_SDCKE0	
AB23	DRAM_SDCKE1	NVCC_DRAM_CKE	DDR		DRAM_SDCKE1	
AF25	DRAM_SDCLK0_N	NVCC_DRAM	DDRCLK		DRAM_SDCLK0_N	
AE25	DRAM_SDCLK0_P	NVCC_DRAM	DDRCLK		DRAM_SDCLK0_P	
AG23	DRAM_SDQS0_N	NVCC_DRAM	DDRCLK		DRAM_SDQS0_N	
AG24	DRAM_SDQS0_P	NVCC_DRAM	DDRCLK		DRAM_SDQS0_P	
AC20	DRAM_SDQS1_N	NVCC_DRAM	DDRCLK		DRAM_SDQS1_N	
AB20	DRAM_SDQS1_P	NVCC_DRAM	DDRCLK		DRAM_SDQS1_P	
AD27	DRAM_SDQS2_N	NVCC_DRAM	DDRCLK		DRAM_SDQS2_N	
AC27	DRAM_SDQS2_P	NVCC_DRAM	DDRCLK		DRAM_SDQS2_P	
Y24	DRAM_SDQS3_N	NVCC_DRAM	DDRCLK		DRAM_SDQS3_N	
Y23	DRAM_SDQS3_P	NVCC_DRAM	DDRCLK		DRAM_SDQS3_P	
AH27	DRAM_SDWE_B	NVCC_DRAM	DDR		DRAM_SDWE_B	
M03	ECSPI1_MISO	NVCC_SPI	GPIO	ALT5	GPIO4_IO[18]	100K PD
L03	ECSPI1_MOSI	NVCC_SPI	GPIO	ALT5	GPIO4_IO[17]	100K PD
K02	ECSPI1_SCLK	NVCC_SPI	GPIO	ALT5	GPIO4_IO[16]	100K PD
N03	ECSPI1_SS0	NVCC_SPI	GPIO	ALT5	GPIO4_IO[19]	100K PD
P02	ECSPI2_MISO	NVCC_SPI	GPIO	ALT5	GPIO4_IO[22]	100K PD

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
N02	ECSPI2_MOSI	NVCC_SPI	GPIO	ALT5	GPIO4_IO[21]	100K PD
N01	ECSPI2_SCLK	NVCC_SPI	GPIO	ALT5	GPIO4_IO[20]	100K PD
R02	ECSPI2_SS0	NVCC_SPI	GPIO	ALT5	GPIO4_IO[23]	100K PD
G18	ENET1_COL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[15]	
F18	ENET1_CRS	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[14]	
F07	ENET1_RD0	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[0]	
E07	ENET1_RD1	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[1]	
D07	ENET1_RD2	NVCC_ENET1	GPIO	ALT5	GPIO_IO[2]	
D16	ENET1_RD3	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[3]	
C06	ENET1_RX_CLK	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[13]	
E11	ENET1_RX_CTL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[4]	
F11	ENET1_RXC	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[5]	
E13	ENET1_TD0	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[6]	
D13	ENET1_TD1	NVCC_ENET1	GPIO	ALT5	GPIO_IO[7]	
E16	ENET1_TD2	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[8]	
F16	ENET1_TD3	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[9]	
F13	ENET1_TX_CLK	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[12]	
G11	ENET1_TX_CTL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[10]	
G09	ENET1_TXC	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[11]	
L23	EPDC_BDR0	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[28]	
L22	EPDC_BDR1	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[29]	
T27	EPDC_D00	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[0]	
U26	EPDC_D01	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[1]	
T26	EPDC_D02	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[10]	
R27	EPDC_D03	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[11]	
N23	EPDC_D04	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[12]	
T28	EPDC_D05	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[13]	
P27	EPDC_D06	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[14]	
N28	EPDC_D07	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[15]	
N27	EPDC_D08	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[2]	
N26	EPDC_D09	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[3]	
N25	EPDC_D10	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[4]	

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
N24	EPDC_D11	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[5]	
M26	EPDC_D12	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[6]	
L26	EPDC_D13	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[7]	
L25	EPDC_D14	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[8]	
N22	EPDC_D15	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[9]	
J23	EPDC_GDCLK	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[24]	
J22	EPDC_GDOE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[25]	
L24	EPDC_GDRL	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[26]	
K27	EPDC_GDSP	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[27]	
J27	EPDC_PWRCOM	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[30]	
J26	EPDC_PWRSTAT	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[31]	
J25	EPDC_SDCE0	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[20]	
J24	EPDC_SDCE1	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[21]	
G22	EPDC_SDCE2	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[22]	
G23	EPDC_SDCE3	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[23]	
G24	EPDC_SDCLK	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[16]	
J28	EPDC_SDLE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[17]	
G25	EPDC_SDOE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[18]	
F26	EPDC_SDSHR	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[19]	
V04	GPIO1_IO00	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO00	100K PU
V05	GPIO1_IO01	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO01	100K PD
Y07	GPIO1_IO02	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO02	100K PD
Y06	GPIO1_IO03	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO03	100K PD
Y05	GPIO1_IO04	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO04	100K PD
Y04	GPIO1_IO05	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO05	100K PD
V06	GPIO1_IO06	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO06	100K PD
V07	GPIO1_IO07	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO07	100K PD
AB03	GPIO1_IO08	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO08	100K PD
AB04	GPIO1_IO09	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO09	100K PD
AB05	GPIO1_IO10	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO10	100K PD
AB06	GPIO1_IO11	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO11	100K PD
AC06	GPIO1_IO12	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO12	100K PD

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
AC05	GPIO1_IO13	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO13	100K PD
AC04	GPIO1_IO14	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO14	100K PD
AC03	GPIO1_IO15	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO15	100K PD
N04	I2C1_SCL	NVCC_I2C	GPIO	ALT5	GPIO4_IO[8]	100K PD
N05	I2C1_SDA	NVCC_I2C	GPIO	ALT5	GPIO4_IO[9]	100K PD
N06	I2C2_SCL	NVCC_I2C	GPIO	ALT5	GPIO4_IO[10]	100K PD
N07	I2C2_SDA	NVCC_I2C	GPIO	ALT5	GPIO4_IO[11]	100K PD
T06	I2C3_SCL	NVCC_I2C	GPIO	ALT5	GPIO4_IO[12]	100K PD
T07	I2C3_SDA	NVCC_I2C	GPIO	ALT5	GPIO4_IO[13]	100K PD
T05	I2C4_SCL	NVCC_I2C	GPIO	ALT5	GPIO4_IO[14]	100K PD
T04	I2C4_SDA	NVCC_I2C	GPIO	ALT5	GPIO4_IO[15]	100K PD
AB01	JTAG_MOD	NVCC_GPIO2	GPIO	ALT0	JTAG_MOD	100K PU
AD01	JTAG_TCK	NVCC_GPIO2	GPIO	ALT0	JTAG_TCK	47K PU
AC02	JTAG_TDI	NVCC_GPIO2	GPIO	ALT0	JTAG_TDI	47K PU
AE01	JTAG_TDO	NVCC_GPIO2	GPIO	ALT0	JTAG_TDO	100K PU
AD02	JTAG_TMS	NVCC_GPIO2	GPIO	ALT0	JTAG_TMS	47K PU
AB02	JTAG_TRST_B	NVCC_GPIO2	GPIO	ALT0	JTAG_TRST_B	47K PU
D20	LCD_CLK	NVCC_LCD	GPIO	ALT5	GPIO3_IO[0]	
F22	LCD_DATA00	NVCC_LCD	GPIO	ALT5	GPIO3_IO[5]	
F23	LCD_DATA01	NVCC_LCD	GPIO	ALT5	GPIO3_IO[6]	
E23	LCD_DATA02	NVCC_LCD	GPIO	ALT5	GPIO3_IO[7]	
E22	LCD_DATA03	NVCC_LCD	GPIO	ALT5	GPIO3_IO[8]	
D22	LCD_DATA04	NVCC_LCD	GPIO	ALT5	GPIO3_IO[9]	
D23	LCD_DATA05	NVCC_LCD	GPIO	ALT5	GPIO3_IO[10]	
E18	LCD_DATA06	NVCC_LCD	GPIO	ALT5	GPIO3_IO[11]	
D18	LCD_DATA07	NVCC_LCD	GPIO	ALT5	GPIO3_IO[12]	
F20	LCD_DATA08	NVCC_LCD	GPIO	ALT5	GPIO3_IO[13]	
G20	LCD_DATA09	NVCC_LCD	GPIO	ALT5	GPIO3_IO[14]	
A27	LCD_DATA10	NVCC_LCD	GPIO	ALT5	GPIO3_IO[15]	
E27	LCD_DATA11	NVCC_LCD	GPIO	ALT5	GPIO3_IO[16]	
F27	LCD_DATA12	NVCC_LCD	GPIO	ALT5	GPIO3_IO[17]	
E28	LCD_DATA13	NVCC_LCD	GPIO	ALT5	GPIO3_IO[18]	

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
G27	LCD_DATA14	NVCC_LCD	GPIO	ALT5	GPIO3_IO[19]	
B28	LCD_DATA15	NVCC_LCD	GPIO	ALT5	GPIO3_IO[20]	
C27	LCD_DATA16	NVCC_LCD	GPIO	ALT5	GPIO3_IO[21]	
D26	LCD_DATA17	NVCC_LCD	GPIO	ALT5	GPIO3_IO[22]	
D27	LCD_DATA18	NVCC_LCD	GPIO	ALT5	GPIO3_IO[23]	
D28	LCD_DATA19	NVCC_LCD	GPIO	ALT5	GPIO3_IO[24]	
G26	LCD_DATA20	NVCC_LCD	GPIO	ALT5	GPIO3_IO[25]	
H26	LCD_DATA21	NVCC_LCD	GPIO	ALT5	GPIO3_IO[26]	
B27	LCD_DATA22	NVCC_LCD	GPIO	ALT5	GPIO3_IO[27]	
D25	LCD_DATA23	NVCC_LCD	GPIO	ALT5	GPIO3_IO[28]	
G28	LCD_ENABLE	NVCC_LCD	GPIO	ALT5	GPIO3_IO[1]	
F25	LCD_HSYNC	NVCC_LCD	GPIO	ALT5	GPIO3_IO[2]	
E20	LCD_RESET	NVCC_LCD	GPIO	ALT5	GPIO3_IO[4]	
F24	LCD_VSYNC	NVCC_LCD	GPIO	ALT5	GPIO3_IO[3]	
B16	MIPI_CSI_CLK_N	MIPI_VDDA_1P8			MIPI_CSI_CLK_N	
A16	MIPI_CSI_CLK_P	MIPI_VDDA_1P8			MIPI_CSI_CLK_P	
B18	MIPI_CSI_D0_N	MIPI_VDDA_1P8			MIPI_CSI_D0_N	
A18	MIPI_CSI_D0_P	MIPI_VDDA_1P8			MIPI_CSI_D0_P	
B15	MIPI_CSI_D1_N	MIPI_VDDA_1P8			MIPI_CSI_D1_N	
B14	MIPI_CSI_D1_P	MIPI_VDDA_1P8			MIPI_CSI_D1_P	
B24	MIPI_DSI_CLK_N	MIPI_VDDA_1P8			MIPI_DSI_CLK_N	
A24	MIPI_DSI_CLK_P	MIPI_VDDA_1P8			MIPI_DSI_CLK_P	
B25	MIPI_DSI_D0_N	MIPI_VDDA_1P8			MIPI_DSI_D0_N	
A25	MIPI_DSI_D0_P	MIPI_VDDA_1P8			MIPI_DSI_D0_P	
A22	MIPI_DSI_D1_N	MIPI_VDDA_1P8			MIPI_DSI_D1_N	
B22	MIPI_DSI_D1_P	MIPI_VDDA_1P8			MIPI_DSI_D1_P	
AD13	ONOFF	VDD_SNVS_IN			ONOFF	
AG13	NC	NC			NC	
AH13	NC	NC			NC	
AG11	NC	NC			NC	
AH11	NC	NC			NC	
AG16	NC	NC			NC	

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
AH16	NC	NC			NC	
AG14	NC	NC			NC	
AG15	NC	NC			NC	
AD11	CCM_PMIC_STBY_REQ	VDD_SNVS_IN			CCM_PMIC_STBY_REQ	
Y03	POR_B	NVCC_GPIO1	GPIO	ALT0	POR_B	100K PU
AG09	RTC_XTALI	VDD_SNVS_1P8_CAP			RTC_XTALI	
AH09	RTC_XTALO	VDD_SNVS_1P8_CAP			RTC_XTALO	
D03	SAI1_MCLK	NVCC_SAI	GPIO	ALT5	GPIO6_IO[18]	
G04	SAI1_RXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[17]	
F03	SAI1_RXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[12]	
C04	SAI1_RXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[16]	
F04	SAI1_TXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[13]	
G05	SAI1_TXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[15]	
F05	SAI1_TXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[14]	
E06	SAI2_RXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[21]	
D04	SAI2_TXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[20]	
D06	SAI2_TXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[22]	
F06	SAI2_TXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[19]	
A05	SD1_CD_B	NVCC_SD1	GPIO	ALT5	GPIO5_IO[0]	
B03	SD1_CLK	NVCC_SD1	GPIO	ALT5	GPIO5_IO[3]	
A02	SD1_CMD	NVCC_SD1	GPIO	ALT5	GPIO5_IO[4]	
B04	SD1_DATA0	NVCC_SD1	GPIO	ALT5	GPIO5_IO[5]	
A04	SD1_DATA1	NVCC_SD1	GPIO	ALT5	GPIO5_IO[6]	
B02	SD1_DATA2	NVCC_SD1	GPIO	ALT5	GPIO5_IO[7]	
B01	SD1_DATA3	NVCC_SD1	GPIO	ALT5	GPIO5_IO[8]	
C02	SD1_RESET_B	NVCC_SD1	GPIO	ALT5	GPIO5_IO[2]	
D02	SD1_WP	NVCC_SD1	GPIO	ALT5	GPIO5_IO[1]	
E01	SD2_CD_B	NVCC_SD2	GPIO	ALT5	GPIO5_IO[9]	
G01	SD2_CLK	NVCC_SD2	GPIO	ALT5	GPIO5_IO[12]	
G02	SD2_CMD	NVCC_SD2	GPIO	ALT5	GPIO5_IO[13]	
F02	SD2_DATA0	NVCC_SD2	GPIO	ALT5	GPIO5_IO[14]	
E02	SD2_DATA1	NVCC_SD2	GPIO	ALT5	GPIO5_IO[15]	

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
H03	SD2_DATA2	NVCC_SD2	GPIO	ALT5	GPIO5_IO[16]	
G03	SD2_DATA3	NVCC_SD2	GPIO	ALT5	GPIO5_IO[17]	
J03	SD2_RESET_B	NVCC_SD2	GPIO	ALT5	GPIO5_IO[11]	
D01	SD2_WP	NVCC_SD2	GPIO	ALT5	GPIO5_IO[10]	
J06	SD3_CLK	NVCC_SD3	GPIO	ALT5	GPIO6_IO[0]	
L04	SD3_CMD	NVCC_SD3	GPIO	ALT5	GPIO6_IO[1]	
G06	SD3_DATA0	NVCC_SD3	GPIO	ALT5	GPIO6_IO[2]	
G07	SD3_DATA1	NVCC_SD3	GPIO	ALT5	GPIO6_IO[3]	
L07	SD3_DATA2	NVCC_SD3	GPIO	ALT5	GPIO6_IO[4]	
L06	SD3_DATA3	NVCC_SD3	GPIO	ALT5	GPIO6_IO[5]	
L05	SD3_DATA4	NVCC_SD3	GPIO	ALT5	GPIO6_IO[6]	
J07	SD3_DATA5	NVCC_SD3	GPIO	ALT5	GPIO6_IO[7]	
J05	SD3_DATA6	NVCC_SD3	GPIO	ALT5	GPIO6_IO[8]	
J04	SD3_DATA7	NVCC_SD3	GPIO	ALT5	GPIO6_IO[9]	
J02	SD3_RESET_B	NVCC_SD3	GPIO	ALT5	GPIO6_IO[11]	
J01	SD3_STROBE	NVCC_SD3	GPIO	ALT5	GPIO6_IO[10]	
AE13	SNVS_PMIC_ON_REQ	VDD_SNVS_IN			SNVS_PMIC_ON_REQ	
AE11	SNVS_TAMPER0	VDDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER0	
AC11	SNVS_TAMPER1	VDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER1	
AC09	SNVS_TAMPER2	VDDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER2	
AB09	SNVS_TAMPER9	VDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER9	
AF06	TEMPSENSOR_RESERVE	VDD_TEMPSENSOR_1P8				
AF07	TEMPSENSOR_REXT	VDD_TEMPSENSOR_1P8			TEMPSENSOR_REXT	
AA03	TEST_MODE	NVCC_GPIO1	GPIO	ALT0	TEST_MODE	
T01	UART1_RXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[0]	
V01	UART1_TXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[1]	
T02	UART2_RXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[2]	
T03	UART2_TXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[3]	
V03	UART3_CTS	NVCC_UART	GPIO	ALT5	GPIO4_IO[7]	
W02	UART3_RTS	NVCC_UART	GPIO	ALT5	GPIO4_IO[6]	
V02	UART3_RXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[4]	
U03	UART3_TXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[5]	

Table 92. i.MX 7Solo 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
A13	USB_H_DATA	USB_H_VDD_1P2			USB_H_DATA	
B13	USB_H_STROBE	USB_H_VDD_1P2			USB_H_STROBE	
B06	USB_OTG1_CHD_B	USB_OTG1_VDDA_3P3			USB_OTG1_CHD_B	
B07	USB_OTG1_DN	USB_OTG1_VDDA_3P3			USB_OTG1_DN	
A07	USB_OTG1_DP	USB_OTG1_VDDA_3P3			USB_OTG1_DP	
B09	USB_OTG1_ID	USB_OTG1_VDDA_3P3			USB_OTG1_ID	
C08	USB_OTG1_REXT	USB_OTG1_VDDA_3P3			USB_OTG1_REXT	
B11	NC	NC			NC	
A11	NC	NC			NC	
B10	NC	NC			NC	
A09	NC	NC			NC	
AG02	XTALI	VDDA_1P8			XTALI	
AG01	XTALO	VDDA_1P8			XTALO	

1 The state immediately after RESET and before ROM firmware or software has executed.

6.1.3 i.MX 7Solo 12 x 12 mm 0.4 mm Pitch Ball Map

The following table shows the i.MX 7Solo 12 x 12 mm 0.4 mm pitch ball map.

Table 93. i.MX 7Solo 12 x 12 mm 0.4 mm pitch ball map

.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.
A	VSS	SD1_CMD		SD1_DATA1	SD1_CD_B		USB_OTG1_DP		NC		NC		USB_H_DATA			MIPI_CSI_CLK_P		MIPI_CSI_D0_P		VDD_ARM		MIPI_DSI_D1_N		MIPI_DSI_CLK_P	MIPI_DSI_D0_P		LCD1_DATA10	VSS	A
B	SD1_DATA3	SD1_DATA2	SD1_CLK	SD1_DATA0	VSS	USB_OTG1_CHD_B	USB_OTG1_DN		USB_OTG1_ID	NC	NC		USB_H_STROBE	MIPI_CSI_D1_P	MIPI_CSI_D1_N	MIPI_CSI_CLK_N		MIPI_CSI_D0_N	MIPI_VREG_0P4V	VDD_ARM		MIPI_DSI_D1_P	VSS	MIPI_DSI_CLK_N	MIPI_DSI_D0_N	VSS	LCD1_DATA22	LCD1_DATA15	B
C		SD1_RESET_B	VSS	SAI1_RXFS	VSS	ENET1_RX_CLK	VSS	USB_OTG1_REXT	USB_OTG1_VBUS	VSS	NC	VDD_USB_H_1P2	VSS	VSS	VSS	VDD_ARM	VDD_ARM	VDD_ARM	VDD_ARM	VDD_ARM	VDD_ARM	VDD_ARM	VSS	VSS	VSS	VSS	LCD1_DATA16		C
D	SD2_WP	SD1_WP	SAI1_MCLK	SAI2_TXC		SAI2_TXD	ENET1_RDATA2	VSS	VDD_USB_OTG1_3P3_IN		VSS	VSS	ENET1_TDATA1			ENET1_RDATA3	VSS	LCD1_DATA07		LCD1_CLK	VSS	LCD1_DATA04	LCD1_DATA05		LCD1_DATA23	LCD1_DATA17	LCD1_DATA18	LCD1_DATA19	D
E	SD2_CD_B	SD2_DATA1	VSS		VSS	SAI2_RXD	ENET1_RDATA1		VDD_USB_OTG1_1P0_CAP		ENET1_RX_CTL		ENET1_TDATA0			ENET1_TDATA2		LCD1_DATA06		LCD1_RESET		LCD1_DATA03	LCD1_DATA02	VSS		VSS	LCD1_DATA11	LCD1_DATA13	E
.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.

Table 93. i.MX 7Solo 12 x 12 mm 0.4 mm pitch ball map(continued)

.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.
F		SD2_DATA0	SAI1_RXD	SAI1_TXC	SAI1_TXFS	SAI2_TXFS	ENET1_RDATA0	VSS	VSS	VSS	ENET1_RXC	VSS	ENET1_TX_CLK	VSS	VSS	ENET1_TDATA3	VSS	ENET1_CRS	VDD_ARM	LCD1_DATA08	VSS	LCD1_DATA00	LCD1_DATA01	LCD1_VSYNC	LCD1_HSYNC	EPDC1_SDSHR	LCD1_DATA12		F
G	SD2_CLK	SD2_CMD	SD2_DATA3	SAI1_RXC	SAI1_TXD	SD3_DATA0	SD3_DATA1		ENET1_TXC		ENET1_TX_CTL		VDD_USB_H_1P2			PVCC_ENET_CAP		ENET1_COL		LCD1_DATA09		EPDC1_SDCE2	EPDC1_SDCE3	EPDC1_SDCLK	EPDC1_SDOE	LCD1_DATA20	LCD1_DATA14	LCD1_ENABLE	G
H			SD2_DATA2	VSS		VSS				VDD_SOC									VDD_ARM				VSS		VSS	LCD1_DATA21			H
J	SD3_STROBE	SD3_RESET_B	SD2_RESET_B	SD3_DATA7	SD3_DATA6	SD3_CLK	SD3_DATA5		VDD_SOC		NVCC_SD1		NVCC_SAI	PVCC_SAI_SD_CAP	VDDA_MIPI_1P8	VDD_MIPI_1P0		NVCC_ENET1		VDD_ARM		EPDC1_GDOE	EPDC1_GDCLK	EPDC1_SDCE1	EPDC1_SDCE0	EPDC1_PWRSTAT	EPDC1_PWRCOM	EPDC1_SDLE	J
K		ECSPI1_SCLK	VDD_SOC			VDD_SOC		VDD_SOC													VDD_ARM		VDD_ARM			VDD_ARM	EPDC1_GDSP		K
L	VDD_SOC	VDD_SOC	ECSPI1_MOSI	SD3_CMD	SD3_DATA4	SD3_DATA3	SD3_DATA2		NVCC_SD2		VDD_SOC		VSS			VSS		VDD_SOC		NVCC_LCD		EPDC1_BDR1	EPDC1_BDR0	EPDC1_GDRL	EPDC1_DATA14	EPDC1_DATA13	VDD_ARM	VDD_ARM	L
M			ECSPI1_MISO	VSS		VSS																	VSS		VSS	EPDC1_DATA12			M
.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.

Table 93. i.MX 7Solo 12 x 12 mm 0.4 mm pitch ball map(continued)

.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.
N	ECSPI2_SCLK	ECSPI2_MOSI	ECSPI1_SS0	I2C1_SCL	I2C1_SDA	I2C2_SCL	I2C2_SDA		NVCC_SD3		VSS		VDD_SOC			VDD_SOC		VSS		NVCC_EPDC2		EPDC1_DATA15	EPDC1_DATA04	EPDC1_DATA11	EPDC1_DATA10	EPDC1_DATA09	EPDC1_DATA08	EPDC1_DATA07	N
P		ECSPI2_MISO	VDD_SOC			VDD_SOC			NVCC_SPI											NVCC_EPDC1			VDD_SOC			VDD_SOC	EPDC1_DATA06		P
R		ECSPI2_SS0	VDD_SOC			VDD_SOC			NVCC_I2C											PVCC_EPDC_LCD_CAP			VDD_SOC			VDD_SOC	EPDC1_DATA03		R
T	UART1_RXD	UART2_RXD	UART2_TXD	I2C4_SDA	I2C4_SCL	I2C3_SCL	I2C3_SDA		NVCC_UART		VSS		VDD_SOC			VDD_SOC		VSS		DRAM_VREF		DRAM_DATA27	DRAM_DATA26	DRAM_DATA31	DRAM_DATA30	EPDC1_DATA02	EPDC1_DATA00	EPDC1_DATA05	T
U			UART3_TXD	VSS		VSS																	VSS		VSS	EPDC1_DATA01			U
V	UART1_TXD	UART3_RXD	UART3_CTS	GPIO1_IO00	GPIO1_IO01	GPIO1_IO06	GPIO1_IO07		FUSE_FSOURCE		VDD_SOC		VSS			VSS		VDD_SOC		NVCC_DRAM_CKE		DRAM_DATA25	DRAM_DATA24	DRAM_DATA28	DRAM_DATA29	DRAM_RESET	NVCC_DRAM	NVCC_DRAM	V
.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.

Table 93. i.MX 7Solo 12 x 12 mm 0.4 mm pitch ball map(continued)

.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.
W		UART3_RTS	VSS			VSS		PVCC_I2C_SPI_UART_CAP													NVCC_DRAM		NVCC_DRAM			NVCC_DRAM	DRAM_DATA16		W
Y	BOOT_MODE0	BOOT_MODE1	POR_B	GPIO1_IO05	GPIO1_IO04	GPIO1_IO03	GPIO1_IO02		NVCC_GPIO1		NVCC_GPIO2		VDD_SNVS_IN	VDDA_PHY_1P8	NC	VSS		DRAM_ZQPAD		NVCC_DRAM		DRAM_SDCKE0	DRAM_SDQS3_P	DRAM_SDQS3_N	DRAM_DQM3	DRAM_DATA18	DRAM_DATA17	DRAM_DATA19	Y
AA			TEST_MODE	VSS		VSS				VDD_1P2_CAP									NVCC_DRAM				VSS		VSS	DRAM_DATA20			AA
AB	JTAG_MOD	JTAG_TRST_B	GPIO1_IO08	GPIO1_IO09	GPIO1_IO10	GPIO1_IO11	ADC1_IN0		SNVS_TAMPER09		PVCC_GPIO_CAP		NC			DRAM_DATA14		DRAM_DATA09		DRAM_SDQS1_P		DRAM_SDBA1	DRAM_SDCKE1	DRAM_ADDR04	DRAM_ADDR03	DRAM_DATA21	DRAM_DATA22	DRAM_DATA23	AB
AC		JTAG_TDI	GPIO1_IO15	GPIO1_IO14	GPIO1_IO13	GPIO1_IO12	ADC1_IN1	VSS	SNVS_TAMPER02	VSS	SNVS_TAMPER01	VSS	VDDD_1P0_CAP	VSS	VSS	DRAM_DATA11	VSS	DRAM_DATA08	NVCC_DRAM	DRAM_SDQS1_N	VSS	DRAM_ADDR09	DRAM_CS1_B	DRAM_ADDR00	DRAM_ADDR01	DRAM_ADDR02	DRAM_SDQS2_P		AC
AD	JTAG_TCK	JTAG_TMS	VSS		VSS	VSS	ADC1_IN2		ADC1_IN3		PMIC_STBY_REQ		ONOFF			DRAM_DATA10		DRAM_DATA12		DRAM_DQM1		DRAM_ADDR08	DRAM_ADDR10	VSS		VSS	DRAM_SDQS2_N	DRAM_DQM2	AD
.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.

Table 93. i.MX 7Solo 12 x 12 mm 0.4 mm pitch ball map(continued)

.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.
AE	JTAG_TDO	CCM_CLK2	CCM_CLK1_P	CCM_CLK1_N		VSS	VSS	VSS	VSS		SNVS_TAMPER00	VDDD_1P0_CAP	SNVS_PMIC_ON_REQ			DRAM_DATA15	VSS	DRAM_DATA13		DRAM_ADDR14	VSS	DRAM_ADDR07	DRAM_ADDR05		DRAM_SDCLK0_P	DRAM_CS0_B	DRAM_ADDR12	DRAM_SDBA0	AE
AF		GPANAIO	VSS	VDDA_1P8_IN	VSS	TEMPSENSOR_RESERVE	TEMPSENSOR_REXT	VSS	VSS	VSS	VSS	VDDD_1P0_CAP	VSS	VSS	VSS	DRAM_ODT0	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	DRAM_DATA04	DRAM_DATA06	DRAM_DATA03	DRAM_ADDR06	VSS	DRAM_SDCLK0_N	VSS	DRAM_SDBA2		AF
AG	XTALO	XTALI	VDDA_1P8_IN	VDDA_1P8_IN	VDD_LPSR_IN	VDD_LPSR_1P0_CAP	VDD_SNVS_1P8_CAP		RTC_XTALI	VSS	NC		NC	NC	NC	NC		NVCC_DRAM	DRAM_DATA01	DRAM_DATA02		DRAM_DATA05	DRAM_SDQS0_N	DRAM_SDQS0_P	DRAM_CAS_B	DRAM_ADDR15	DRAM_ADDR11	DRAM_ADDR13	AG
AH	VSS	VDD_XTAL_1P8		VDDA_ADC1_1P8	VDD_TEMPSENSOR_1P8		VDDA_1P0_CAP		RTC_XTALO		NC		NC			NC		NVCC_DRAM		DRAM_DATA07		DRAM_DATA00		DRAM_DQM0	DRAM_RAS_B		DRAM_SDWE_B	VSS	AH
.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	.

6.2 19 x 19 mm package information

6.2.1 Case “Y”, 19 x 19 mm, 0.75 mm pitch, ball matrix

Figure 88 shows the top, bottom, and side views of the 19×19 mm BGA package.

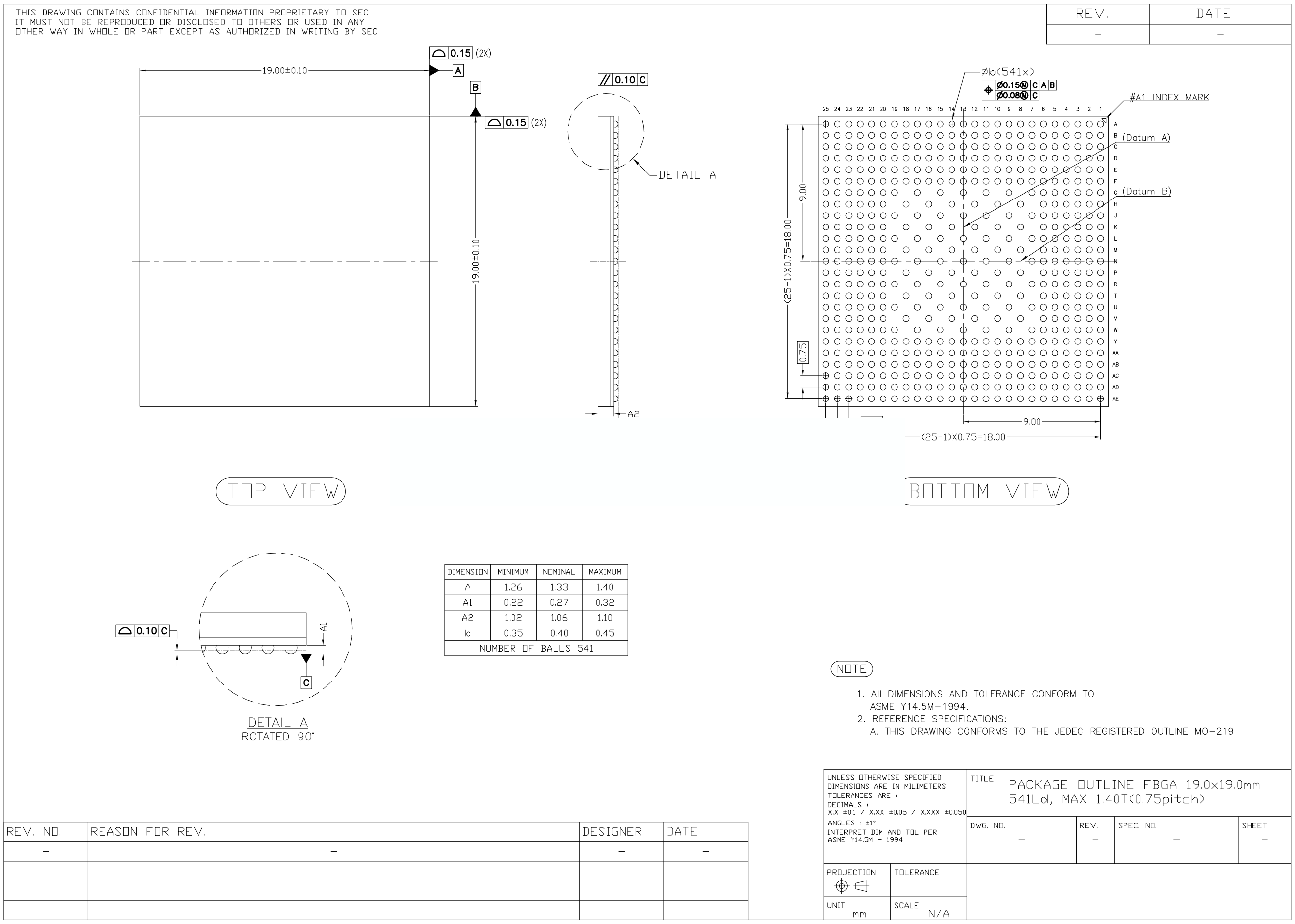


Figure 88. 19 x 19 mm BGA, Case x Package Top, Bottom, and Side Views

6.2.2 19 x 19 mm supplies contact assignments and functional contact assignments

Table 94 shows supplies contact assignments for the 19 x 19 mm package.

Table 94. i.MX 7Solo 19 x 19 mm supplies contact assignments

Rail	Pins	Comments
ADC2_VDDA_1P8	AB03	
DRAM_VREF	AC13	
DRAM_ZQPAD	AB13	DDR output buffer driver calibration reference voltage input. Connect DRAM_ZQPAD to an external 240 ohm 1% resistor to Vss
FUSE_FSOURCE0	V08	
GND	A01,A03,A06,A09,A13,A17,A21,A25,B03,B06,B09,B13,B17,B21,C09,C13,C15,C16,C18,C19,D01,D02,D04,D07,D10,D22,F07,F08,F09,F11,F13,G07,G04,G09,G11,G13,G15,G17,G19,G22,H01,H02,J07,J11,J19,K04,K10,K12,K14,K16,K22,L07,L11,L13,L15,L19,M10,M12,M14,M16,M24,M25,N04,N07,N11,N13,N15,N19,P10,P12,P14,P16,R07,R11,R13,R15,R19,R20,R21,R23,T04,T10,T12,T14,T16,T20,U07,U11,U19,U20,U23,V20,W01,W02,W04,W07,W09,W11,W13,W15,W17,W19,W20,W23,Y06,Y13,Y14,Y15,Y16,Y17,Y18,Y19,AA01,AA02,AA06,AA08,AA13,AA15,AA23,AB04,AB05,AB07,AB09,AB12,AC06,AC09,AC12,AC15,AC17,AC19,AC21,AC23,AD02,AD07,AD09,AD12,AE01,AE05,AE07,AE09,AE12,AE24,AE25	Ground
GPANIO	V04	Test signal. Should be left unconnected.
MIPI_VREG_0P4V	H18	
NC	A10, A11, B10, B11, C10, Y10, Y11, Y12, AA10, AA11, AA12, AB10, AB11, AC10, AC11, AD10, AD11, AE10, AE11	Do not connect
NVCC_DRAM	T21,U21,V21,W21,Y21,AA16,AA17,AA18,AA19,AA20,AA21	
NVCC_DRAM_CKE	Y20	
NVCC_ENET1	H16	Supply for ENET interface
NVCC_EPDC1	M18	Supply for EPDC interface
NVCC_EPDC2	L17	Supply for EPDC interface
NVCC_GPIO1	P08	Supply for GPIO1 interface
NVCC_GPIO2	T08	Supply for GPIO2 interface
NVCC_I2C	M08	Supply for I2C interface

Table 94. i.MX 7Solo 19 x 19 mm supplies contact assignments (continued)

Rail	Pins	Comments
NVCC_LCD	K18	Supply for LCD interface
NVCC_SAI	F12	Supply for SAI interface
NVCC_SD1	E07	Supply for SD card interface
NVCC_SD2	H08	Supply for SD card interface
NVCC_SD3	K08	Supply for SD card interface
NVCC_SPI	L09	Supply for SPI interface
NVCC_UART	N09	Supply for UART interface
PVCC_ENET_CAP	H14	Secondary supply for ENET (internal regulator output). Requires external capacitors
PVCC_EPDC_LCD_CAP	N17	Secondary supply for EPDC_LCD (internal regulator output). Requires external capacitors
PVCC_GPIO_CAP	V10	Secondary supply for GPIO (internal regulator output). Requires external capacitors
PVCC_I2C_SPI_UART_CAP	R09	Secondary supply for I2C_SPI_UART (internal regulator output). Requires external capacitors
PVCC_SAI_SD_CAP	J09	Secondary supply for SAI_SD (internal regulator output). Requires external capacitors
USB_OTG1_VBUS	C08	
USB_OTG1_VDDA_3P3_IN	F10	
VDD_1P2_CAP	U09	Supply for HSIC
VDD_ARM	C17,C20,D17,D20,F22,F23,J22,J23	Supply for ARM
VDD_LPSR_1P0_CAP	AC05	Secondary supply for LPSR (internal regulator output). Requires external capacitors
VDD_LPSR_IN	W06	Supply for LPSR
VDD_SNVS_1P8_CAP	AE08	Secondary supply for SNVS (internal regulator output). Requires external capacitors
VDD_SNVS_IN	AD08	Primary supply for the SNVS regulator
VDD_SOC	C14,D14,F03,F04,F18,F19,J03,J04,M03,M04,P18,R03,R04,R17,T18,U13,U15,U17,V12,V14,V16,V18	Supply for SOC
VDD_TEMPSENSOR_1P8	AC04	Supply for VDDe PHY
VDD_USB_H_1P2	H12	Supply input for the USB HSIC Interface
VDD_USB_OTG1_1P0_CAP	H10	Secondary supply for USB OTG (internal regulator output). Requires external capacitors
VDD_XTAL_1P8	V05	
VDDA_1P0_CAP	V03	Secondary supply for 1P0 (internal regulator output). Requires external capacitors

Table 94. i.MX 7Solo 19 x 19 mm supplies contact assignments (continued)

Rail	Pins	Comments
VDDA_1P8_IN	V06,W05	
VDDA_ADC1_1P8	AC03	Supply for ADC
VDDA_PHY_1P8	Y09	
VDDD_1P0_CAP	AA09	Secondary supply for 1P0 (internal regulator output). Requires external capacitors

Table 95 shows an alpha-sorted list of functional contact assignments for the 19 x 19 mm package.

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
AD01	ADC1_IN0	ADC1_VDDA_1P8			ADC1_IN0	
AD03	ADC1_IN1	ADC1_VDDA_1P8			ADC1_IN1	
AE02	ADC1_IN2	ADC1_VDDA_1P8			ADC1_IN2	
AE03	ADC1_IN3	ADC1_VDDA_1P8			ADC1_IN3	
AC01	ADC2_IN0	ADC2_VDDA_1P8			ADC2_IN0	
AC02	ADC2_IN1	ADC2_VDDA_1P8			ADC2_IN1	
AB01	ADC2_IN2	ADC2_VDDA_1P8			ADC2_IN2	
AB02	ADC2_IN3	ADC2_VDDA_1P8			ADC2_IN3	
P04	BOOT_MODE0	NVCC_GPIO1	GPIO	ALT0	BOOT_MODE0	100K PD
P05	BOOT_MODE1	NVCC_GPIO1	GPIO	ALT0	BOOT_MODE1	100K PD
Y01	CCM_CLK1_N	VDDA_1P8			CCM_CLK1_N	
Y02	CCM_CLK1_P	VDDA_1P8			CCM_CLK1_P	
W03	CCM_CLK2	VDDA_1P8			CCM_CLK2	
AC07	CCM_PMIC_STBY_REQ	VDD_SNVS_IN			CCM_PMIC_STBY_REQ	
AB19	DRAM_ADDR00	NVCC_DRAM	DDR		DRAM_ADDR00	
AB16	DRAM_ADDR01	NVCC_DRAM	DDR		DRAM_ADDR01	
AC18	DRAM_ADDR02	NVCC_DRAM	DDR		DRAM_ADDR02	
AC20	DRAM_ADDR03	NVCC_DRAM	DDR		DRAM_ADDR03	
AB21	DRAM_ADDR04	NVCC_DRAM	DDR		DRAM_ADDR04	
Y23	DRAM_ADDR05	NVCC_DRAM	DDR		DRAM_ADDR05	
V22	DRAM_ADDR06	NVCC_DRAM	DDR		DRAM_ADDR06	
Y22	DRAM_ADDR07	NVCC_DRAM	DDR		DRAM_ADDR07	
W22	DRAM_ADDR08	NVCC_DRAM	DDR		DRAM_ADDR08	

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
V23	DRAM_ADDR09	NVCC_DRAM	DDR		DRAM_ADDR09	
T23	DRAM_ADDR10		DDR		DRAM_ADDR10	
U22	DRAM_ADDR11	NVCC_DRAM	DDR		DRAM_ADDR11	
T22	DRAM_ADDR12	NVCC_DRAM	DDR		DRAM_ADDR12	
P23	DRAM_ADDR13	NVCC_DRAM	DDR		DRAM_ADDR13	
AB18	DRAM_ADDR14	NVCC_DRAM	DDR		DRAM_ADDR14	
AB20	DRAM_ADDR15	NVCC_DRAM	DDR		DRAM_ADDR15	
AC14	DRAM_CAS_B	NVCC_DRAM	DDR		DRAM_CAS_B	
AB23	DRAM_CS0_B	NVCC_DRAM	DDR		DRAM_CS0_B	
AA22	DRAM_CS1_B	NVCC_DRAM	DDR		DRAM_CS1_B	
AD22	DRAM_DATA00	NVCC_DRAM	DDR		DRAM_DATA00	
AD23	DRAM_DATA01	NVCC_DRAM	DDR		DRAM_DATA01	
AE20	DRAM_DATA02	NVCC_DRAM	DDR		DRAM_DATA02	
AE23	DRAM_DATA03	NVCC_DRAM	DDR		DRAM_DATA03	
AE22	DRAM_DATA04	NVCC_DRAM	DDR		DRAM_DATA04	
AD19	DRAM_DATA05	NVCC_DRAM	DDR		DRAM_DATA05	
AD18	DRAM_DATA06	NVCC_DRAM	DDR		DRAM_DATA06	
AE19	DRAM_DATA07	NVCC_DRAM	DDR		DRAM_DATA07	
AE14	DRAM_DATA08	NVCC_DRAM	DDR		DRAM_DATA08	
AE18	DRAM_DATA09	NVCC_DRAM	DDR		DRAM_DATA09	
AE17	DRAM_DATA10	NVCC_DRAM	DDR		DRAM_DATA10	
AD16	DRAM_DATA11	NVCC_DRAM	DDR		DRAM_DATA11	
AE16	DRAM_DATA12	NVCC_DRAM	DDR		DRAM_DATA12	
AD14	DRAM_DATA13	NVCC_DRAM	DDR		DRAM_DATA13	
AD13	DRAM_DATA14	NVCC_DRAM	DDR		DRAM_DATA14	
AE13	DRAM_DATA15	NVCC_DRAM	DDR		DRAM_DATA15	
AA25	DRAM_DATA16	NVCC_DRAM	DDR		DRAM_DATA16	
W24	DRAM_DATA17	NVCC_DRAM	DDR		DRAM_DATA17	
V25	DRAM_DATA18	NVCC_DRAM	DDR		DRAM_DATA18	
W25	DRAM_DATA19	NVCC_DRAM	DDR		DRAM_DATA19	
AC25	DRAM_DATA20	NVCC_DRAM	DDR		DRAM_DATA20	
AB25	DRAM_DATA21	NVCC_DRAM	DDR		DRAM_DATA21	

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
AB24	DRAM_DATA22	NVCC_DRAM	DDR		DRAM_DATA22	
AC24	DRAM_DATA23	NVCC_DRAM	DDR		DRAM_DATA23	
R25	DRAM_DATA24	NVCC_DRAM	DDR		DRAM_DATA24	
N24	DRAM_DATA25	NVCC_DRAM	DDR		DRAM_DATA25	
P25	DRAM_DATA26	NVCC_DRAM	DDR		DRAM_DATA26	
N25	DRAM_DATA27	NVCC_DRAM	DDR		DRAM_DATA27	
U25	DRAM_DATA28	NVCC_DRAM	DDR		DRAM_DATA28	
R24	DRAM_DATA29	NVCC_DRAM	DDR		DRAM_DATA29	
U24	DRAM_DATA30	NVCC_DRAM	DDR		DRAM_DATA30	
V24	DRAM_DATA31	NVCC_DRAM	DDR		DRAM_DATA31	
AD20	DRAM_DQM0	NVCC_DRAM	DDR		DRAM_DQM0	
AD17	DRAM_DQM1	NVCC_DRAM	DDR		DRAM_DQM1	
AA24	DRAM_DQM2	NVCC_DRAM	DDR		DRAM_DQM2	
P24	DRAM_DQM3	NVCC_DRAM	DDR		DRAM_DQM3	
AC16	DRAM_ODT0	NVCC_DRAM	DDR		DRAM_ODT0	
AA14	DRAM_ODT1	NVCC_DRAM	DDR		DRAM_ODT1	
AB15	DRAM_RAS_B	NVCC_DRAM	DDR		DRAM_RAS_B	
AC22	DRAM_RESET	NVCC_DRAM_CKE	DDR		DRAM_RESET	
R22	DRAM_SDBA0	NVCC_DRAM	DDR		DRAM_SDBA0	
P22	DRAM_SDBA1	NVCC_DRAM	DDR		DRAM_SDBA1	
N23	DRAM_SDBA2	NVCC_DRAM	DDR		DRAM_SDBA2	
AB17	DRAM_SDCKE0	NVCC_DRAM_CKE	DDR		DRAM_SDCKE0	
AB22	DRAM_SDCKE1	NVCC_DRAM_CKE	DDR		DRAM_SDCKE1	
AD25	DRAM_SDCLK0_N	NVCC_DRAM	DDRCLK		DRAM_SDCLK0_N	
AD24	DRAM_SDCLK0_P	NVCC_DRAM	DDRCLK		DRAM_SDCLK0_P	
AD21	DRAM_SDQS0_N	NVCC_DRAM	DDRCLK		DRAM_SDQS0_N	
AE21	DRAM_SDQS0_P	NVCC_DRAM	DDRCLK		DRAM_SDQS0_P	
AE15	DRAM_SDQS1_N	NVCC_DRAM	DDRCLK		DRAM_SDQS1_N	
AD15	DRAM_SDQS1_P	NVCC_DRAM	DDRCLK		DRAM_SDQS1_P	
Y25	DRAM_SDQS2_N	NVCC_DRAM	DDRCLK		DRAM_SDQS2_N	
Y24	DRAM_SDQS2_P	NVCC_DRAM	DDRCLK		DRAM_SDQS2_P	
T25	DRAM_SDQS3_N	NVCC_DRAM	DDRCLK		DRAM_SDQS3_N	

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
T24	DRAM_SDQS3_P	NVCC_DRAM	DDRCLK		DRAM_SDQS3_P	
AB14	DRAM_SDWE_B	NVCC_DRAM	DDR		DRAM_SDWE_B	
H04	ECSPI1_MISO	NVCC_SPI	GPIO	ALT5	GPIO4_IO[18]	100K PD
G05	ECSPI1_MOSI	NVCC_SPI	GPIO	ALT5	GPIO4_IO[17]	100K PD
H03	ECSPI1_SCLK	NVCC_SPI	GPIO	ALT5	GPIO4_IO[16]	100K PD
H05	ECSPI1_SS0	NVCC_SPI	GPIO	ALT5	GPIO4_IO[19]	100K PD
H06	ECSPI2_MISO	NVCC_SPI	GPIO	ALT5	GPIO4_IO[22]	100K PD
G06	ECSPI2_MOSI	NVCC_SPI	GPIO	ALT5	GPIO4_IO[21]	100K PD
J05	ECSPI2_SCLK	NVCC_SPI	GPIO	ALT5	GPIO4_IO[20]	100K PD
J06	ECSPI2_SS0	NVCC_SPI	GPIO	ALT5	GPIO4_IO[23]	100K PD
D19	ENET1_COL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[15]	100K PD
E19	ENET1_CRS	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[14]	100K PD
E14	ENET1_RD0	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[0]	100K PD
F14	ENET1_RD1	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[1]	100K PD
D13	ENET1_RD2	NVCC_ENET1	GPIO	ALT5	GPIO_IO[2]	100K PD
E13	ENET1_RD3	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[3]	100K PD
D15	ENET1_RX_CLK	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[13]	100K PD
E15	ENET1_RX_CTL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[4]	100K PD
F15	ENET1_RXC	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[5]	100K PD
F17	ENET1_TD0	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[6]	100K PD
E17	ENET1_TD1	NVCC_ENET1	GPIO	ALT5	GPIO_IO[7]	100K PD
E18	ENET1_TD2	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[8]	100K PD
D18	ENET1_TD3	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[9]	100K PD
D16	ENET1_TX_CLK	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[12]	100K PD
E16	ENET1_TX_CTL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[10]	100K PD
F16	ENET1_TXC	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[11]	100K PD
K24	EPDC_BDR0	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[28]	100K PD
K23	EPDC_BDR1	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[29]	100K PD
P20	EPDC_D00	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[0]	100K PD
P21	EPDC_D01	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[1]	100K PD
N20	EPDC_D02	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[10]	100K PD
N21	EPDC_D03	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[11]	100K PD

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
N22	EPDC_D04	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[12]	100K PD
M20	EPDC_D05	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[13]	100K PD
M21	EPDC_D06	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[14]	100K PD
M22	EPDC_D07	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[15]	100K PD
M23	EPDC_D08	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[2]	100K PD
L25	EPDC_D09	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[3]	100K PD
L24	EPDC_D10	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[4]	100K PD
L23	EPDC_D11	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[5]	100K PD
L22	EPDC_D12	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[6]	100K PD
L21	EPDC_D13	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[7]	100K PD
L20	EPDC_D14	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[8]	100K PD
K25	EPDC_D15	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[9]	100K PD
J25	EPDC_GDCLK	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[24]	100K PD
J24	EPDC_GDOE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[25]	100K PD
K21	EPDC_GDRL	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[26]	100K PD
H25	EPDC_GDSP	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[27]	100K PD
H24	EPDC_PWRCOM	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[30]	100K PD
K20	EPDC_PWRSTAT	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[31]	100K PD
G25	EPDC_SDCE0	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[20]	100K PD
G24	EPDC_SDCE1	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[21]	100K PD
H23	EPDC_SDCE2	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[22]	100K PD
H22	EPDC_SDCE3	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[23]	100K PD
J21	EPDC_SDCLK	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[16]	100K PD
J20	EPDC_SDLE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[17]	100K PD
H21	EPDC_SDOE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[18]	100K PD
H20	EPDC_SDSHR	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[19]	100K PD
N01	GPIO1_IO00	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO00	100K PU
N02	GPIO1_IO01	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO01	100K PD
N03	GPIO1_IO02	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO02	100K PD
N05	GPIO1_IO03	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO03	100K PD
N06	GPIO1_IO04	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO04	100K PD
P01	GPIO1_IO05	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO05	100K PD

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
P02	GPIO1_IO06	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO06	100K PD
P03	GPIO1_IO07	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO07	100K PD
R01	GPIO1_IO08	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO08	100K PD
R02	GPIO1_IO09	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO09	100K PD
R05	GPIO1_IO10	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO10	100K PD
T01	GPIO1_IO11	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO11	100K PD
T02	GPIO1_IO12	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO12	100K PD
T03	GPIO1_IO13	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO13	100K PD
T05	GPIO1_IO14	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO14	100K PD
T06	GPIO1_IO15	NVCC_GPIO2	GPIO	ALT0	GPIO1_IO15	100K PD
J02	I2C1_SCL	NVCC_I2C	GPIO	ALT5	GPIO4_IO[8]	100K PD
K01	I2C1_SDA	NVCC_I2C	GPIO	ALT5	GPIO4_IO[9]	100K PD
K02	I2C2_SCL	NVCC_I2C	GPIO	ALT5	GPIO4_IO[10]	100K PD
K03	I2C2_SDA	NVCC_I2C	GPIO	ALT5	GPIO4_IO[11]	100K PD
K05	I2C3_SCL	NVCC_I2C	GPIO	ALT5	GPIO4_IO[12]	100K PD
K06	I2C3_SDA	NVCC_I2C	GPIO	ALT5	GPIO4_IO[13]	100K PD
L01	I2C4_SCL	NVCC_I2C	GPIO	ALT5	GPIO4_IO[14]	100K PD
L02	I2C4_SDA	NVCC_I2C	GPIO	ALT5	GPIO4_IO[15]	100K PD
U01	JTAG_MOD	NVCC_GPIO2	GPIO	ALT0	JTAG_MOD	100K PU
U05	JTAG_TCK	NVCC_GPIO2	GPIO	ALT0	JTAG_TCK	47K PU
U03	JTAG_TDI	NVCC_GPIO2	GPIO	ALT0	JTAG_TDI	47K PU
U06	JTAG_TDO	NVCC_GPIO2	GPIO	ALT0	JTAG_TDO	100K PU
U04	JTAG_TMS	NVCC_GPIO2	GPIO	ALT0	JTAG_TMS	47K PU
U02	JTAG_TRST_B	NVCC_GPIO2	GPIO	ALT0	JTAG_TRST_B	47K PU
E20	LCD_CLK	NVCC_LCD	GPIO	ALT5	GPIO3_IO[0]	100K PD
D21	LCD_DATA00	NVCC_LCD	GPIO	ALT5	GPIO3_IO[5]	100K PD
A22	LCD_DATA01	NVCC_LCD	GPIO	ALT5	GPIO3_IO[6]	100K PD
B22	LCD_DATA02	NVCC_LCD	GPIO	ALT5	GPIO3_IO[7]	100K PD
A23	LCD_DATA03	NVCC_LCD	GPIO	ALT5	GPIO3_IO[8]	100K PD
C22	LCD_DATA04	NVCC_LCD	GPIO	ALT5	GPIO3_IO[9]	100K PD
B23	LCD_DATA05	NVCC_LCD	GPIO	ALT5	GPIO3_IO[10]	100K PD
A24	LCD_DATA06	NVCC_LCD	GPIO	ALT5	GPIO3_IO[11]	100K PD

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
F20	LCD_DATA07	NVCC_LCD	GPIO	ALT5	GPIO3_IO[12]	100K PD
E21	LCD_DATA08	NVCC_LCD	GPIO	ALT5	GPIO3_IO[13]	100K PD
C23	LCD_DATA09	NVCC_LCD	GPIO	ALT5	GPIO3_IO[14]	100K PD
B24	LCD_DATA10	NVCC_LCD	GPIO	ALT5	GPIO3_IO[15]	100K PD
G20	LCD_DATA11	NVCC_LCD	GPIO	ALT5	GPIO3_IO[16]	100K PD
F21	LCD_DATA12	NVCC_LCD	GPIO	ALT5	GPIO3_IO[17]	100K PD
E22	LCD_DATA13	NVCC_LCD	GPIO	ALT5	GPIO3_IO[18]	100K PD
D23	LCD_DATA14	NVCC_LCD	GPIO	ALT5	GPIO3_IO[19]	100K PD
C24	LCD_DATA15	NVCC_LCD	GPIO	ALT5	GPIO3_IO[20]	100K PD
B25	LCD_DATA16	NVCC_LCD	GPIO	ALT5	GPIO3_IO[21]	100K PD
G21	LCD_DATA17	NVCC_LCD	GPIO	ALT5	GPIO3_IO[22]	100K PD
E23	LCD_DATA18	NVCC_LCD	GPIO	ALT5	GPIO3_IO[23]	100K PD
D24	LCD_DATA19	NVCC_LCD	GPIO	ALT5	GPIO3_IO[24]	100K PD
C25	LCD_DATA20	NVCC_LCD	GPIO	ALT5	GPIO3_IO[25]	100K PD
E24	LCD_DATA21	NVCC_LCD	GPIO	ALT5	GPIO3_IO[26]	100K PD
D25	LCD_DATA22	NVCC_LCD	GPIO	ALT5	GPIO3_IO[27]	100K PD
G23	LCD_DATA23	NVCC_LCD	GPIO	ALT5	GPIO3_IO[28]	100K PD
F25	LCD_ENABLE	NVCC_LCD	GPIO	ALT5	GPIO3_IO[1]	100K PD
E25	LCD_HSYNC	NVCC_LCD	GPIO	ALT5	GPIO3_IO[2]	100K PD
C21	LCD_RESET	NVCC_LCD	GPIO	ALT5	GPIO3_IO[4]	100K PD
F24	LCD_VSYNC	NVCC_LCD	GPIO	ALT5	GPIO3_IO[3]	100K PD
A15	MIPI_CSI_CLK_N	MIPI_VDDA_1P8			MIPI_CSI_CLK_N	
B15	MIPI_CSI_CLK_P	MIPI_VDDA_1P8			MIPI_CSI_CLK_P	
A16	MIPI_CSI_D0_N	MIPI_VDDA_1P8			MIPI_CSI_D0_N	
B16	MIPI_CSI_D0_P	MIPI_VDDA_1P8			MIPI_CSI_D0_P	
A14	MIPI_CSI_D1_N	MIPI_VDDA_1P8			MIPI_CSI_D1_N	
B14	MIPI_CSI_D1_P	MIPI_VDDA_1P8			MIPI_CSI_D1_P	
A19	MIPI_DSI_CLK_N	MIPI_VDDA_1P8			MIPI_DSI_CLK_N	
B19	MIPI_DSI_CLK_P	MIPI_VDDA_1P8			MIPI_DSI_CLK_P	
A20	MIPI_DSI_D0_N	MIPI_VDDA_1P8			MIPI_DSI_D0_N	
B20	MIPI_DSI_D0_P	MIPI_VDDA_1P8			MIPI_DSI_D0_P	
A18	MIPI_DSI_D1_N	MIPI_VDDA_1P8			MIPI_DSI_D1_N	

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
B18	MIPI_DSI_D1_P	MIPI_VDDA_1P8			MIPI_DSI_D1_P	
J13	MIPI_VDDA_1P8	MIPI_VDDA_1P8			MIPI_VDDA_1P8	
J15	MIPI_VDDD_1P0	MIPI_VDDD_1P0			MIPI_VDDD_1P0	
J17	MIPI_VDDD_1P0	MIPI_VDDD_1P0			MIPI_VDDD_1P0	
AC08	ONOFF	VDD_SNVS_IN			ONOFF	
AE10	NC	NC			NC	
AD10	NC	NC			NC	
AC10	NC	NC			NC	
AB10	NC	NC			NC	
AE11	NC	NC			NC	
AD11	NC	NC			NC	
AC11	NC	NC			NC	
AB11	NC	NC			NC	
AA10	NC	NC			NC	
AA12	NC	NC			NC	
AA11	NC	NC			NC	
Y10	NC	NC			NC	
Y12	NC	NC			NC	
Y11	NC	NC			NC	
R06	POR_B	NVCC_GPIO1	GPIO	ALT0	POR_B	100K PU
AE06	RTC_XTALI	VDD_SNVS_1P8_CAP			RTC_XTALI	
AD06	RTC_XTALO	VDD_SNVS_1P8_CAP			RTC_XTALO	
E10	SAI1_MCLK	NVCC_SAI	GPIO	ALT5	GPIO6_IO[18]	100K PD
D12	SAI1_RXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[17]	100K PD
E12	SAI1_RXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[12]	100K PD
C12	SAI1_RXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[16]	100K PD
C11	SAI1_TXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[13]	100K PD
E11	SAI1_TXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[15]	100K PD
D11	SAI1_TXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[14]	100K PD
E09	SAI2_RXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[21]	100K PD
D08	SAI2_TXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[20]	100K PD
E08	SAI2_TXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[22]	100K PD

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
D09	SAI2_TXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[19]	100K PD
C06	SD1_CD_B	NVCC_SD1	GPIO	ALT5	GPIO5_IO[0]	100K PD
B05	SD1_CLK	NVCC_SD1	GPIO	ALT5	GPIO5_IO[3]	100K PD
C05	SD1_CMD	NVCC_SD1	GPIO	ALT5	GPIO5_IO[4]	100K PD
A05	SD1_DATA0	NVCC_SD1	GPIO	ALT5	GPIO5_IO[5]	100K PD
D06	SD1_DATA1	NVCC_SD1	GPIO	ALT5	GPIO5_IO[6]	100K PD
A04	SD1_DATA2	NVCC_SD1	GPIO	ALT5	GPIO5_IO[7]	100K PD
D05	SD1_DATA3	NVCC_SD1	GPIO	ALT5	GPIO5_IO[8]	100K PD
B04	SD1_RESET_B	NVCC_SD1	GPIO	ALT5	GPIO5_IO[2]	100K PD
C04	SD1_WP	NVCC_SD1	GPIO	ALT5	GPIO5_IO[1]	100K PD
E03	SD2_CLK	NVCC_SD2	GPIO	ALT5	GPIO5_IO[12]	100K PD
F06	SD2_CMD	NVCC_SD2	GPIO	ALT5	GPIO5_IO[13]	100K PD
E04	SD2_DATA0	NVCC_SD2	GPIO	ALT5	GPIO5_IO[14]	100K PD
E05	SD2_DATA1	NVCC_SD2	GPIO	ALT5	GPIO5_IO[15]	100K PD
F05	SD2_DATA2	NVCC_SD2	GPIO	ALT5	GPIO5_IO[16]	100K PD
E06	SD2_DATA3	NVCC_SD2	GPIO	ALT5	GPIO5_IO[17]	100K PD
G03	SD2_RESET_B	NVCC_SD2	GPIO	ALT5	GPIO5_IO[11]	100K PD
C03	SD2_WP	NVCC_SD2	GPIO	ALT5	GPIO5_IO[10]	100K PD
C01	SD3_CLK	NVCC_SD3	GPIO	ALT5	GPIO6_IO[0]	100K PD
E01	SD3_CMD	NVCC_SD3	GPIO	ALT5	GPIO6_IO[1]	100K PD
B02	SD3_DATA0	NVCC_SD3	GPIO	ALT5	GPIO6_IO[2]	100K PD
A02	SD3_DATA1	NVCC_SD3	GPIO	ALT5	GPIO6_IO[3]	100K PD
G02	SD3_DATA2	NVCC_SD3	GPIO	ALT5	GPIO6_IO[4]	100K PD
F01	SD3_DATA3	NVCC_SD3	GPIO	ALT5	GPIO6_IO[5]	100K PD
F02	SD3_DATA4	NVCC_SD3	GPIO	ALT5	GPIO6_IO[6]	100K PD
E02	SD3_DATA5	NVCC_SD3	GPIO	ALT5	GPIO6_IO[7]	100K PD
C02	SD3_DATA6	NVCC_SD3	GPIO	ALT5	GPIO6_IO[8]	100K PD
B01	SD3_DATA7	NVCC_SD3	GPIO	ALT5	GPIO6_IO[9]	100K PD
G01	SD3_RESET_B	NVCC_SD3	GPIO	ALT5	GPIO6_IO[11]	100K PD
J01	SD3_STROBE	NVCC_SD3	GPIO	ALT5	GPIO6_IO[10]	100K PD
AB08	SNVS_PMIC_ON_REQ	VDD_SNVS_IN			SNVS_PMIC_ON_REQ	
AA07	SNVS_TAMPER0	VDDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER0	

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
Y08	SNVS_TAMPER1	VDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER1	
AB06	SNVS_TAMPER2	VDDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER2	
Y07	SNVS_TAMPER3	VDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER3	
AA05	SNVS_TAMPER4	VDDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER4	
Y05	SNVS_TAMPER5	VDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER5	
AA04	SNVS_TAMPER6	VDDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER6	
Y04	SNVS_TAMPER7	VDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER7	
AA03	SNVS_TAMPER8	VDDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER8	
Y03	SNVS_TAMPER9	VDD_SNVS_1P8_CAP	Analog		SNVS_TAMPER9	
AE04	TEMPSENSOR_REXT	VDD_TEMPSENSOR_1P8			TEMPSENSOR_REXT	
AD04	TEMPSENSOR_TEST_OUT	VDD_TEMPSENSOR_1P8			TEMPSENSOR_TEST_OUT	
P06	TEST_MODE	NVCC_GPIO1	GPIO	ALT0	TEST_MODE	100K PD
L03	UART1_RXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[0]	100K PD
L04	UART1_TXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[1]	100K PD
L05	UART2_RXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[2]	100K PD
L06	UART2_TXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[3]	100K PD
M06	UART3_CTS	NVCC_UART	GPIO	ALT5	GPIO4_IO[7]	100K PD
M05	UART3_RTS	NVCC_UART	GPIO	ALT5	GPIO4_IO[6]	100K PD
M01	UART3_RXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[4]	100K PD
M02	UART3_TXD	NVCC_UART	GPIO	ALT5	GPIO4_IO[5]	100K PD
A12	USB_H_DATA	USB_H_VDD_1P2			USB_H_DATA	
B12	USB_H_STROBE	USB_H_VDD_1P2			USB_H_STROBE	
C07	USB_OTG1_CHD_B	USB_OTG1_VDDA_3P3			USB_OTG1_CHD_B	
A08	USB_OTG1_DN	USB_OTG1_VDDA_3P3			USB_OTG1_DN	
B08	USB_OTG1_DP	USB_OTG1_VDDA_3P3			USB_OTG1_DP	
B07	USB_OTG1_ID	USB_OTG1_VDDA_3P3			USB_OTG1_ID	
A07	USB_OTG1_REXT	USB_OTG1_VDDA_3P3			USB_OTG1_REXT	
A10	NC	NC			NC	
B10	NC	NC			NC	
B11	NC	NC			NC	
A11	NC	NC			NC	

Table 95. i.MX 7Solo 19 x 19 mm functional contact assignments (continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
V01	XTALI	VDDA_1P8			XTALI	
V02	XTALO	VDDA_1P8			XTALO	

[1] The state immediately after RESET and before ROM firmware or software has executed.

6.2.3 Case “Y”, i.MX 7Solo 19 × 19 mm 0.75 mm pitch ball map

The following table shows the i.MX 7Solo 19 × 19 mm, 0.75 mm pitch ball map.

Table 96. i.MX 7Solo 19 × 19 mm, 0.75 mm pitch ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	VSS	SD3_DATA1	VSS	SD1_DATA2	SD1_DATA0	VSS	USB_OTG1_REXT	USB_OTG1_DN	VSS	NC	NC	USB_H_DATA	VSS	MIPI_CSI_D1_N	MIPI_CSI_CLK_N	MIPI_CSI_D0_N	VSS	MIPI_DSI_D1_N	MIPI_DSI_CLK_N	MIPI_DSI_D0_N	VSS	LCD1_DATA01	LCD1_DATA03	LCD1_DATA06	VSS	A
B	SD3_DATA7	SD3_DATA0	VSS	SD1_RESET_B	SD1_CLK	VSS	USB_OTG1_ID	USB_OTG1_DP	VSS	NC	NC	USB_H_STROBE	VSS	MIPI_CSI_D1_P	MIPI_CSI_CLK_P	MIPI_CSI_D0_P	VSS	MIPI_DSI_D1_P	MIPI_DSI_CLK_P	MIPI_DSI_D0_P	VSS	LCD1_DATA02	LCD1_DATA05	LCD1_DATA10	LCD1_DATA16	B
C	SD3_CLK	SD3_DATA6	SD2_WP	SD1_WP	SD1_CMD	SD1_CD_B	USB_OTG1_CHD_B	USB_OTG1_VBUS	VSS	NC	SAI1_TXC	SAI1_RXFS	VSS	VDD_SOC	VSS	VSS	VDD_ARM	VSS	VSS	VDD_ARM	LCD1_RESET	LCD1_DATA04	LCD1_DATA09	LCD1_DATA15	LCD1_DATA20	C
D	VSS	VSS	SD2_CD_B	VSS	SD1_DATA3	SD1_DATA1	VSS	SAI2_TXC	SAI2_TXFS	VSS	SAI1_TXFS	SAI1_RXC	ENET1_RDATA2	VDD_SOC	ENET1_RX_CLK	ENET1_TX_CLK	VDD_ARM	ENET1_TDATA3	ENET1_COL	VDD_ARM	LCD1_DATA00	VSS	LCD1_DATA14	LCD1_DATA19	LCD1_DATA22	D
E	SD3_CMD	SD3_DATA5	SD2_CLK	SD2_DATA0	SD2_DATA1	SD2_DATA3	NVCC_SD1	SAI2_TXD	SAI2_RXD	SAI1_MCLK	SAI1_TXD	SAI1_RXD	ENET1_RDATA3	ENET1_RD0	ENET1_RX_CTL	ENET1_TX_CTL	ENET1_TDATA1	ENET1_TDATA2	ENET1_CRS	LCD1_CLK	LCD1_DATA08	LCD1_DATA13	LCD1_DATA18	LCD1_DATA21	LCD1_HSYNC	E
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Table 96. i.MX 7Solo 19 × 19 mm, 0.75 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
F	SD3_DATA3	SD3_DATA4	VDD_SOC	VDD_SOC	SD2_DATA2	SD2_CMD	VSS	VSS	VSS	VDD_USB_OTG1_3P3_IN	VSS	NVCC_SAI	VSS	ENET1_RDATA1	ENET1_RXC	ENET1_TXC	ENET1_TD0	VDD_SOC	VDD_SOC	LCD1_DATA07	LCD1_DATA12	VDD_ARM	VDD_ARM	LCD1_VSYNC	LCD1_ENABLE	F
G	SD3_RESET_B	SD3_DATA2	SD2_RESET_B	VSS	ECSPI1_MOSI	ECSPI2_MOSI	VSS		VSS		VSS		VSS		VSS		VSS		VSS	LCD1_DATA11	LCD1_DATA17	VSS	LCD1_DATA23	EPDC1_SDCE1	EPDC1_SDCE0	G
H	VSS	VSS	ECSPI1_SCLK	ECSPI1_MISO	ECSPI1_SS0	ECSPI2_MISO		NVCC_SD2		VDD_USB_OTG1_1P0_CAP		VDD_USB_H_1P2		PVCC_ENET_CAP		NVCC_ENET1		MIPI_VREG_0P4V		EPDC1_SDSHR	EPDC1_SDOE	EPDC1_SDCE3	EPDC1_SDCE2	EPDC1_PWRCOM	EPDC1_GDSP	H
J	SD3_STROBE	I2C1_SCL	VDD_SOC	VDD_SOC	ECSPI2_SCLK	ECSPI2_SS0	VSS		PVCC_SAI_SD_CAP		VSS		VDDA_MIPI_1P8		VDD_MIPI_1P0		VDD_MIPI_1P0		VSS	EPDC1_SDLE	EPDC1_SDCLK	VDD_ARM	VDD_ARM	EPDC1_GDOE	EPDC1_GDCLK	J
K	I2C1_SDA	I2C2_SCL	I2C2_SDA	VSS	I2C3_SCL	I2C3_SDA		NVCC_SD3		VSS		VSS		VSS		VSS		NVCC_LCD		EPDC1_PWRSTAT	EPDC1_GDRL	VSS	EPDC1_BDR1	EPDC1_BDR0	EPDC1_DATA15	K
L	I2C4_SCL	I2C4_SDA	UART1_RXD	UART1_TXD	UART2_RXD	UART2_TXD	VSS		NVCC_SPI		VSS		VSS		VSS		NVCC_EPDC2		VSS	EPDC1_DATA14	EPDC1_DATA13	EPDC1_DATA12	EPDC1_DATA11	EPDC1_DATA10	EPDC1_DATA09	L
M	UART3_RXD	UART3_TXD	VDD_SOC	VDD_SOC	UART3_RTS	UART3_CTS		NVCC_I2C		VSS		VSS		VSS		VSS		NVCC_EPDC1		EPDC1_DATA05	EPDC1_DATA06	EPDC1_DATA07	EPDC1_DATA08	VSS	VSS	M
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Table 96. i.MX 7Solo 19 × 19 mm, 0.75 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
N	GPIO1_IO00	GPIO1_IO01	GPIO1_IO02	VSS	GPIO1_IO03	GPIO1_IO04	VSS		NVCC_UART		VSS		VSS		VSS		PVCC_EPDC_LCD_CAP		VSS	EPDC1_DATA02	EPDC1_DATA03	EPDC1_DATA04	DRAM_SDBA2	DRAM_DATA25	DRAM_DATA27	N
P	GPIO1_IO05	GPIO1_IO06	GPIO1_IO07	BOOT_MODE0	BOOT_MODE1	TEST_MODE		NVCC_GPIO1		VSS		VSS		VSS		VSS		VDD_SOC		EPDC_D00	EPDC1_DATA01	DRAM_SDBA1	DRAM_ADDR13	DRAM_DQM3	DRAM_DATA26	P
R	GPIO1_IO08	GPIO1_IO09	VDD_SOC	VDD_SOC	GPIO1_IO10	POR_B	VSS		PVCC_I2C_SPI_UART_CAP		VSS		VSS		VSS		VDD_SOC		VSS	VSS	VSS	DRAM_SDBA0	VSS	DRAM_DATA29	DRAM_DATA24	R
T	GPIO1_IO11	GPIO1_IO12	GPIO1_IO13	VSS	GPIO1_IO14	GPIO1_IO15		NVCC_GPIO2		VSS		VSS		VSS		VSS		VDD_SOC		VSS	NVCC_DRAM	DRAM_ADDR12	DRAM_ADDR10	DRAM_SDQS3_P	DRAM_SDQS3_N	T
U	JTAG_MOD	JTAG_TRST_B	JTAG_TDI	JTAG_TMS	JTAG_TCK	JTAG_TDO	VSS		VDD_1P2_CAP		VSS		VDD_SOC		VDD_SOC		VDD_SOC		VSS	VSS	NVCC_DRAM	DRAM_ADDR11	VSS	DRAM_DATA30	DRAM_DATA28	U
V	XTALI	XTALO	VDDA_1P0_CAP	GPANAIO	VDD_XTAL_1P8	VDDA_1P8_IN		FUSE_FSOURCE		PVCC_GPIO_CAP		VDD_SOC		VDD_SOC		VDD_SOC		VDD_SOC		VSS	NVCC_DRAM	DRAM_ADDR06	DRAM_ADDR09	DRAM_DATA31	DRAM_DATA18	V
W	VSS	VSS	CCM_CLK2	VSS	VDDA_1P8_IN	VDD_LPSR_IN	VSS		VSS		VSS		VSS		VSS		VSS		VSS	VSS	NVCC_DRAM	DRAM_ADDR08	VSS	DRAM_DATA17	DRAM_DATA19	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Table 96. i.MX 7Solo 19 × 19 mm, 0.75 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
Y	CCM_CLK1_N	CCM_CLK1_P	SNVS_TAMPER09	SNVS_TAMPER07	SNVS_TAMPER05	VSS	SNVS_TAMPER03	SNVS_TAMPER01	VDDA_PHY_1P8	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NVCC_DRAM_CKE	NVCC_DRAM	DRAM_ADDR07	DRAM_ADDR05	DRAM_SDQS2_P	DRAM_SDQS2_N	**Y**
AA	VSS	VSS	SNVS_TAMPER08	SNVS_TAMPER06	SNVS_TAMPER04	VSS	SNVS_TAMPER00	VSS	VDDD_1P0_CAP	NC	NC	NC	VSS	DRAM_ODT1	VSS	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	DRAM_CS1_B	VSS	DRAM_DQM2	DRAM_DATA16	**AA**
AB	ADC2_IN2	ADC2_IN3	VDDA_ADC2_1P8	VSS	VSS	SNVS_TAMPER02	VSS	SNVS_PMIC_ON_REQ	VSS	NC	NC	VSS	DRAM_ZQPAD	DRAM_SDWE_B	DRAM_RAS_B	DRAM_ADDR01	DRAM_SDCKE0	DRAM_ADDR14	DRAM_ADDR00	DRAM_ADDR15	DRAM_ADDR04	DRAM_SDCKE1	DRAM_CS0_B	DRAM_DATA22	DRAM_DATA21	**AB**
AC	ADC2_IN0	ADC2_IN1	VDDA_ADC1_1P8	VDD_TEMPSENSOR_1P8	VDD_LPSR_1P0_CAP	VSS	PMIC_STBY_REQ	ONOFF	VSS	NC	NC	VSS	DRAM_VREF	DRAM_CAS_B	VSS	DRAM_ODT0	VSS	DRAM_ADDR02	VSS	DRAM_ADDR03	VSS	DRAM_RESET	VSS	DRAM_DATA23	DRAM_DATA20	**AC**
AD	ADC1_IN0	VSS	ADC1_IN1	TEMPSENSOR_RESERVE	VSS	RTC_XTALO	VSS	VDD_SNVS_IN	VSS	NC	NC	VSS	DRAM_DATA14	DRAM_DATA13	DRAM_SDQS1_P	DRAM_DATA11	DRAM_DQM1	DRAM_DATA06	DRAM_DATA05	DRAM_DQM0	DRAM_SDQS0_N	DRAM_DATA00	DRAM_DATA01	DRAM_SDCLK0_P	DRAM_SDCLK0_N	**AD**
AE	VSS	ADC1_IN2	ADC1_IN3	TEMPSENSOR_REXT	VSS	RTC_XTALI	VSS	VDD_SNVS_1P8_CAP	VSS	NC	NC	VSS	DRAM_DATA15	DRAM_DATA08	DRAM_SDQS1_N	DRAM_DATA12	DRAM_DATA10	DRAM_DATA09	DRAM_DATA07	DRAM_DATA02	DRAM_SDQS0_P	DRAM_DATA04	DRAM_DATA03	VSS	VSS	**AE**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

7 Revision history

Table 97 provides a revision history for this data sheet.

Table 97. Revision history

Rev. Number	Date	Substantive Change(s)

Rev. 4	04/2017	• Throughout: Added content related to uSDHC3
		• In top right margin of page 1, corrected MCIMX7SxDxxxxxB to MCIMX7SxDxxxxxC, and corrected MCIMX7SxExxxxxB to MCIMX7SxExxxxxC
		• In Figure 1, "Part number nomenclature—i.MX 7Solo family of processors:"
		    • Removed row for part differentiator '2'
		    • Updated key for part differentiator '3'
		• Updated Section 4.10.10, "QUAD SPI (QSPI) Timing Parameters"
		• Changed title of Section 4.10.7, from "MIPI-CSI timing parameters" to "Parallel CMOS sensor interface (CSI) timing parameters"
		• Changed title of Section 4.10.8, from "MIPI DSI timing parameters" to "MIPI PHY timing parameters," and changed references to 'MIPI D-PHY' to 'MIPI PHY' throughout the section

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