

Vishay Siliconix

P-Channel 2.5 V (G-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A) ^b		
- 20	0.100 at V _{GS} = - 4.5 V	- 2.4		
- 20	0.150 at V _{GS} = - 2.5 V	- 2.0		

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



HALOGEN FREE Available

TO-236 (SOT-23) G 1 S 2 Top View

Si2301 BDS (L1)* * Marking Code

Ordering Information: Si2301BDS-T1-E3 (Lead (Pb)-free) Si2301BDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	$(T_A = 25 \ ^{\circ}C, unle$	ess otherwise	noted)			
Parameter		Symbol	5 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	- 20		V	
Gate-Source Voltage		V _{GS}	± 8		v	
Continuous Drain Current $(T_{,l} = 150 \text{ °C})^{b}$	T _A = 25 °C	– I _D	- 2.4	- 2.2		
Continuous Drain Current $(1_J = 150^{\circ}C)^2$	T _A = 70 °C		- 1.9	- 1.8		
Pulsed Drain Current ^a		I _{DM}	- 10		A	
Continuous Source Current (Diode Conduction) ^b		۱ _S	- 0.72	- 0.6		
	T _A = 25 °C	- P _D	0.9	0.7	w	
Power Dissipation ^b	T _A = 70 °C		0.57	0.45	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^b	R _{thJA}	120	145	°C/W	
Maximum Junction-to-Ambient ^c	' 'thJA	140	175	0/10	

Notes:

a. Pulse width limited by maximum junction temperature.

b. Surface mounted on FR4 board, t \leq 5 s.

c. Surface mounted on FR4 board.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

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			Limits				
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V$, $I_D = -250 \mu A$	- 20			v	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	- 0.45		- 0.95	v	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 8 V$			± 100	nA	
Zero Gate Voltage Drain Current	1	$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1	μΑ	
	IDSS	V_{DS} = - 20 V, V_{GS} = 0 V, T_{J} = 55 °C			- 10		
On-State Drain Current ^a		$V_{DS}{\leq}$ - 5 V, $V_{GS}{=}$ - 4.5 V	- 6			A	
	I _{D(on)}	$V_{DS} \leq$ - 5 V, V_{GS} = - 2.5 V	- 3				
Drain-Source On-State Resistance ^a		$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -2.8 \text{ A}$		0.080	0.100	- Ω	
	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, \text{ I}_{D} = -2 \text{ A}$		0.110	0.150		
Forward Transconductance ^a	9 _{fs}	$V_{DS} = -5 V, I_{D} = -2.8 A$		6.5		S	
Diode Forward Voltage	V _{SD}	$I_{\rm S}$ = - 0.75 A, $V_{\rm GS}$ = 0 V		- 0.80	- 1.2	V	
Dynamic ^b							
Total Gate Charge	Qg			4.5	10		
Gate-Source Charge	Q _{gs}	V _{DS} = - 6 V, V _{GS} = - 4.5 V I _D ≅ - 2.8 A		0.7		nC	
Gate-Drain Charge	Q _{gd}	D = 2.0 A		1.1			
Gate Resistance	R _g	f = 1 MHz	2	8	16	Ω	
Input Capacitance	C _{iss}			375			
Output Capacitance	C _{oss}	$V_{DS} = -6 V$, $V_{GS} = 0 V$, f = 1 MHz		95		pF	
Reverse Transfer Capacitance	C _{rss}			65			
Switching ^c	· ·						
Turn-On Time	t _{d(on)}			20	30		
	t _r	$V_{DD} = -6 V, R_L = 6 \Omega$ $I_D \cong -1 A, V_{GEN} = -4.5 V$		40	60		
Turn-Off Time	t _{d(off)}	$R_{\rm g} = 6 \Omega$		30	45	ns	
	t _f	g		20	30]	

Notes:

a. Pulse test: pulse width \leq 300 µs duty cycle \leq 2 %.

b. For DESIGN AID ONLY, not subject to production testing.

c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

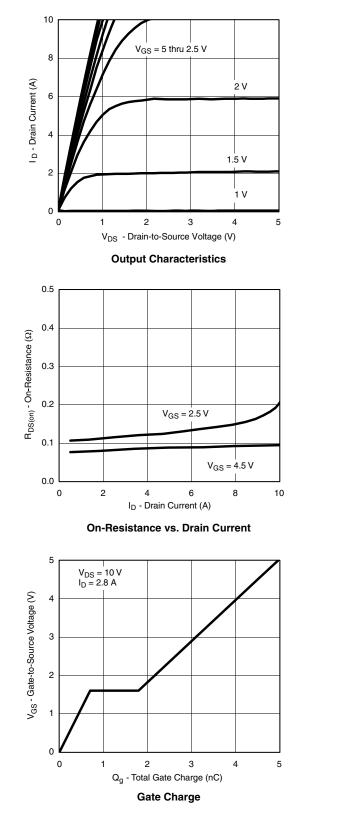
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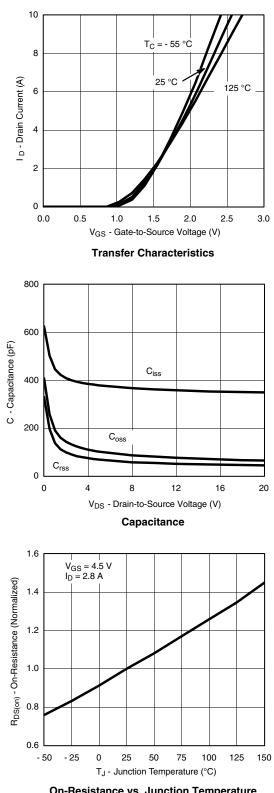
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





On-Resistance vs. Junction Temperature

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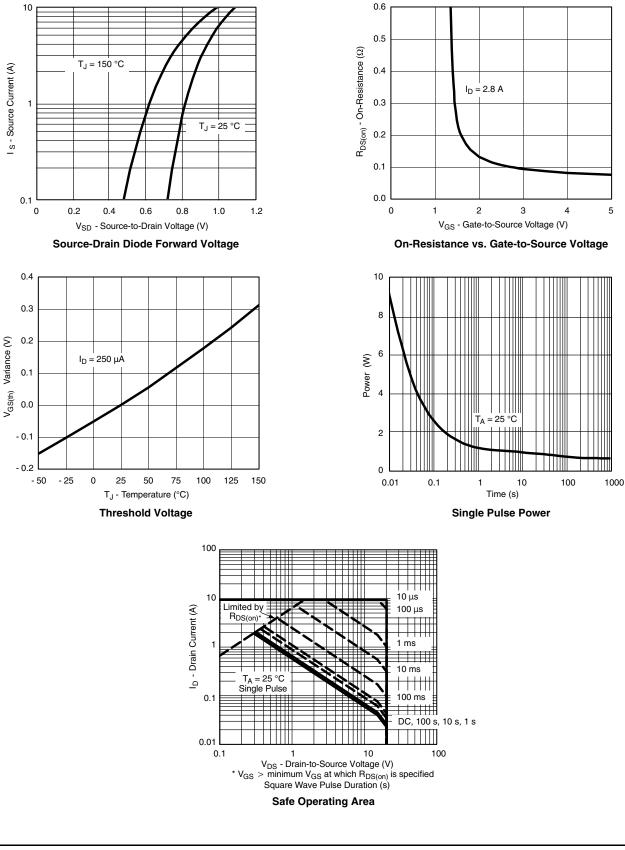
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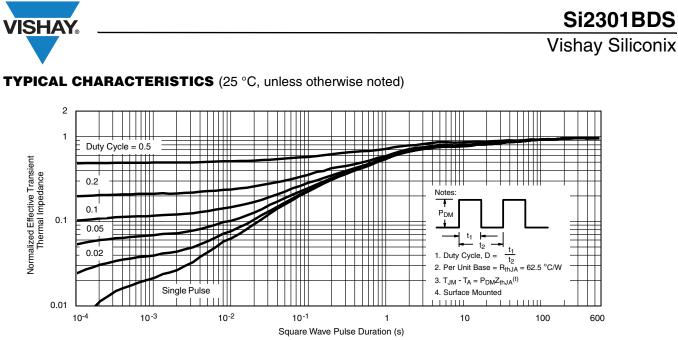


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg772066</u>.

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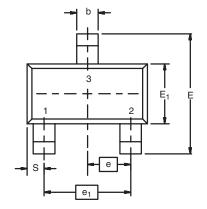
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Package Information

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SOT-23 (TO-236): 3-LEAD







Dim	MILLIN	METERS	INCHES		
	Min	Max	Min	Мах	
Α	0.89	1.12	0.035	0.044	
A ₁	0.01	0.10	0.0004	0.004	
A ₂	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E ₁	1.20	1.40	0.047	0.055	
е	0.95 BSC		0.0374 Ref		
e ₁	1.90 BSC		0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L ₁	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	



Application Note 826

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RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

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