

# MMBTA70LT1G

## General Purpose Transistor PNP Silicon

### Features

- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	-40	Vdc
Emitter-Base Voltage	$V_{EBO}$	-4.0	Vdc
Collector Current - Continuous	$I_C$	-100	mAdc

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board, (Note 1) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 2) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

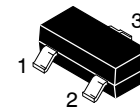
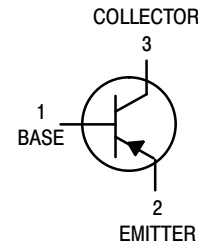
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.



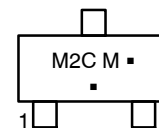
ON Semiconductor®

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SOT-23 (TO-236)  
CASE 318  
STYLE 6

### MARKING DIAGRAM



M2C = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or overbar may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
MMBTA70LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MMBTA70LT1G

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Breakdown Voltage ( $I_C = -1.0\text{ mAdc}$ , $I_B = 0$ )	$V_{(BR)CEO}$	-40	-	Vdc
Emitter-Base Breakdown Voltage ( $I_E = -100\ \mu\text{Adc}$ , $I_C = 0$ )	$V_{(BR)EBO}$	-4.0	-	Vdc
Collector Cutoff Current ( $V_{CB} = -30\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	-	-100	nAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = -5.0\text{ mAdc}$ , $V_{CE} = -10\text{ Vdc}$ )	$h_{FE}$	40	400	-
Collector-Emitter Saturation Voltage ( $I_C = -10\text{ mAdc}$ , $I_B = -1.0\text{ mAdc}$ )	$V_{CE(sat)}$	-	-0.25	Vdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>				
Current-Gain - Bandwidth Product ( $I_C = -5.0\text{ mAdc}$ , $V_{CE} = -10\text{ Vdc}$ , $f = 100\text{ MHz}$ )	$f_T$	125	-	MHz
Output Capacitance ( $V_{CB} = -10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{obo}$	-	4.0	pF

## TYPICAL NOISE CHARACTERISTICS

( $V_{CE} = -5.0\text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$ )

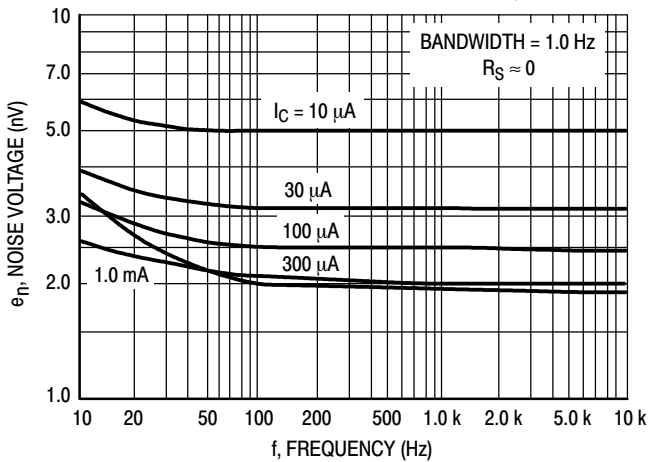


Figure 1. Noise Voltage

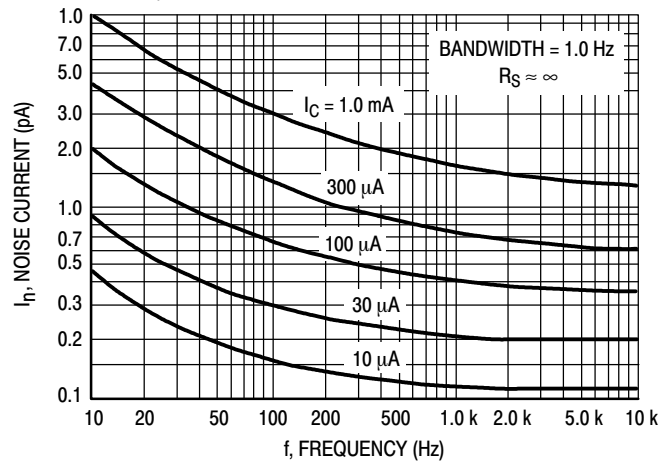


Figure 2. Noise Current

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## NOISE FIGURE CONTOURS

( $V_{CE} = -5.0 \text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$ )

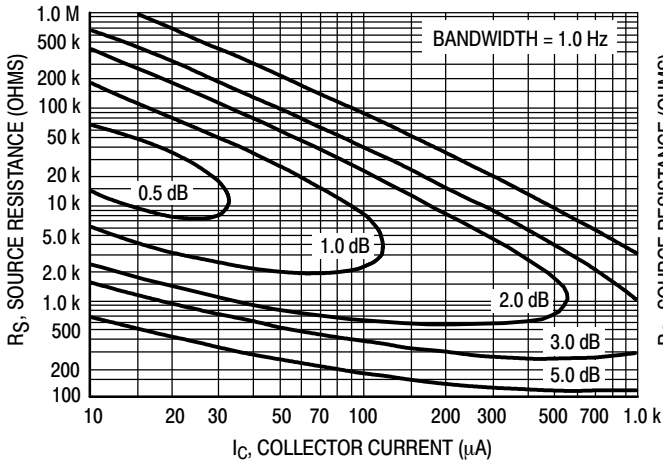


Figure 3. Narrow Band, 100 Hz

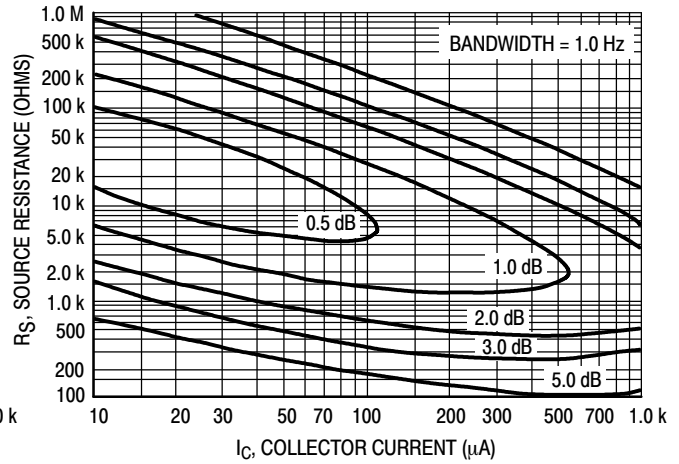


Figure 4. Narrow Band, 1.0 kHz

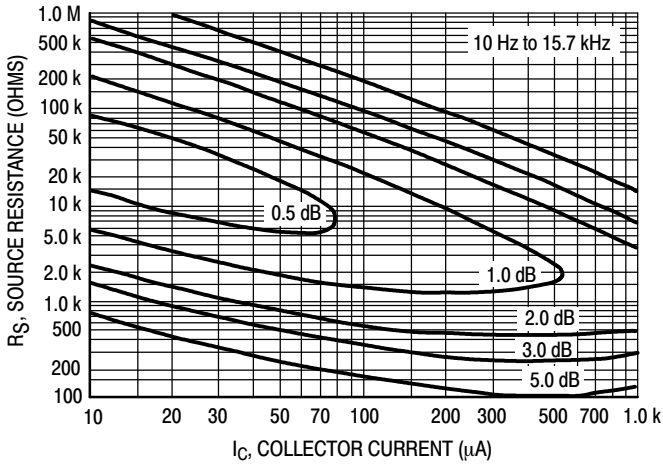


Figure 5. Wideband

Noise Figure is Defined as:

$$NF = 20 \log_{10} \left[ \frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right]^{1/2}$$

$e_n$  = Noise Voltage of the Transistor referred to the input. (Figure 3)

$I_n$  = Noise Current of the Transistor referred to the input. (Figure 4)

$K$  = Boltzman's Constant ( $1.38 \times 10^{-23} \text{ J}^\circ\text{K}$ )

$T$  = Temperature of the Source Resistance ( $^\circ\text{K}$ )

$R_S$  = Source Resistance (Ohms)

# MMBTA70LT1G

## TYPICAL STATIC CHARACTERISTICS

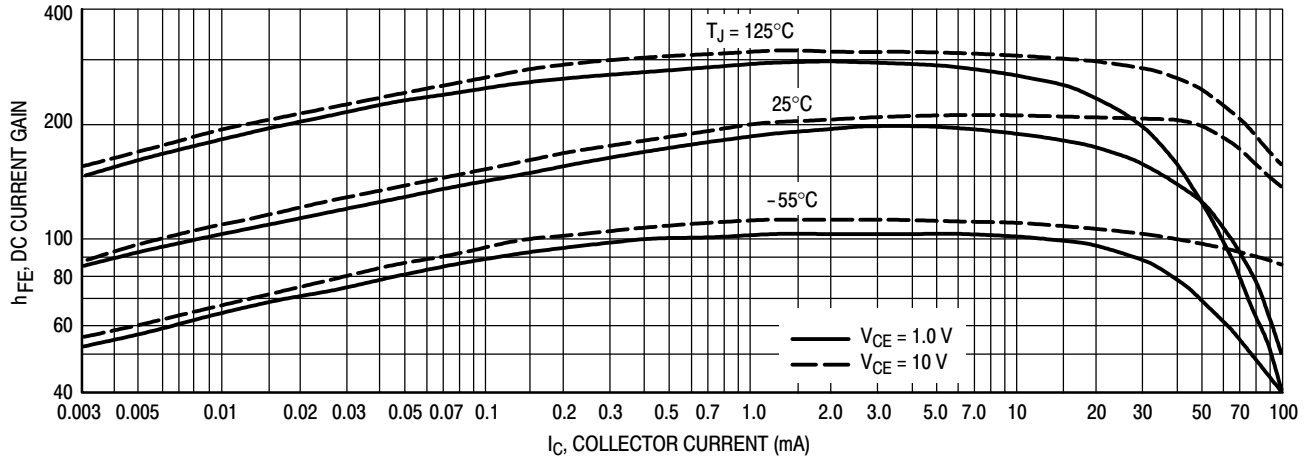


Figure 6. DC Current Gain

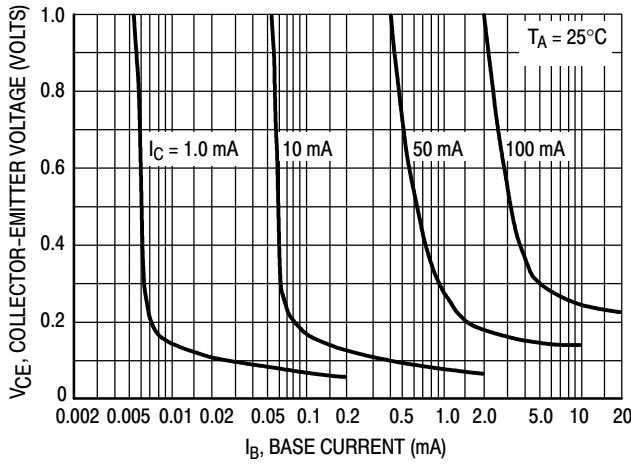


Figure 7. Collector Saturation Region

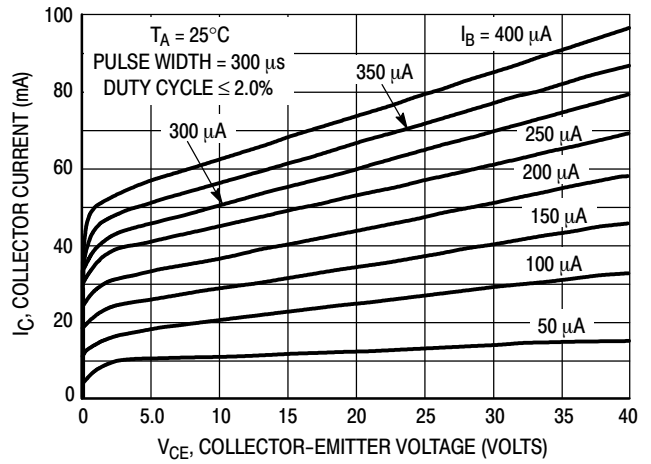


Figure 8. Collector Characteristics

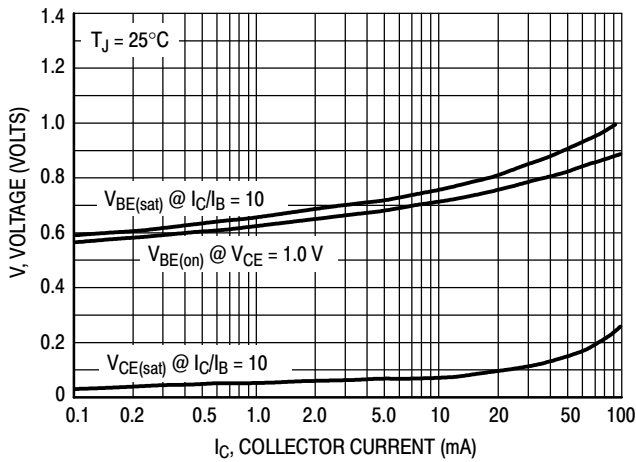


Figure 9. "On" Voltages

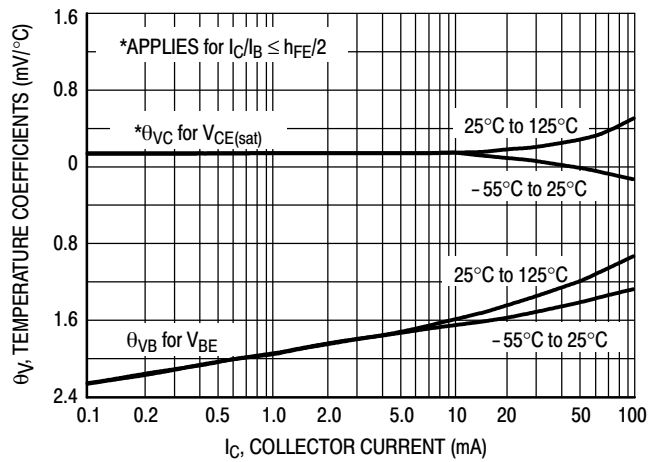


Figure 10. Temperature Coefficients

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## TYPICAL DYNAMIC CHARACTERISTICS

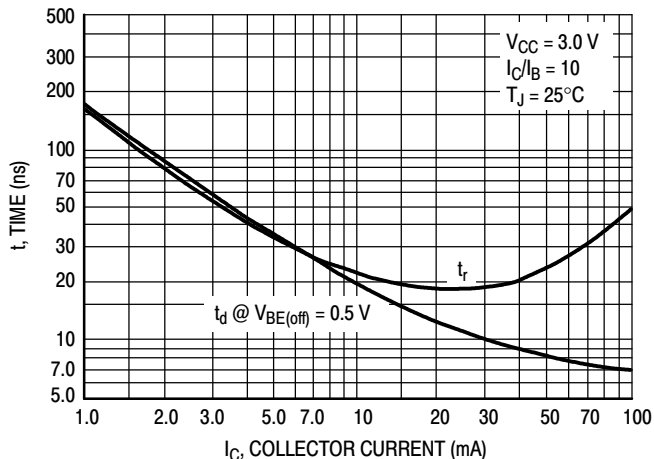


Figure 11. Turn-On Time

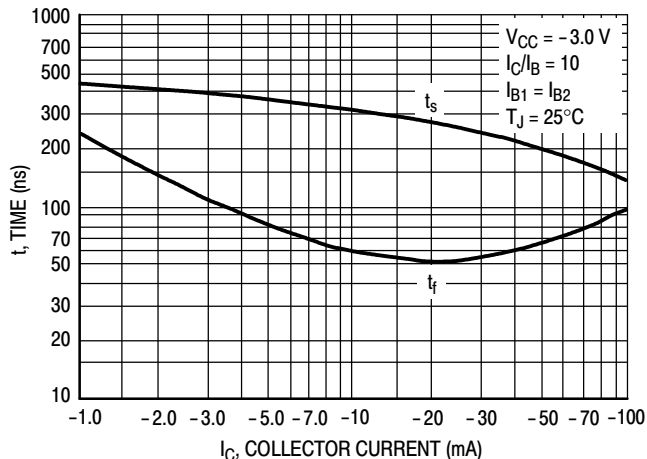


Figure 12. Turn-Off Time

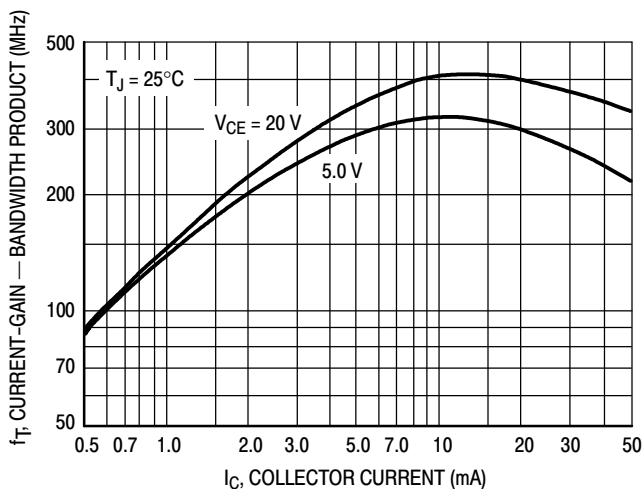


Figure 13. Current-Gain — Bandwidth Product

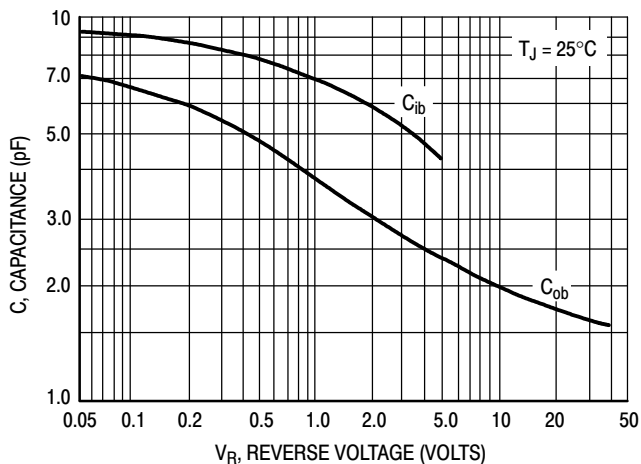


Figure 14. Capacitance

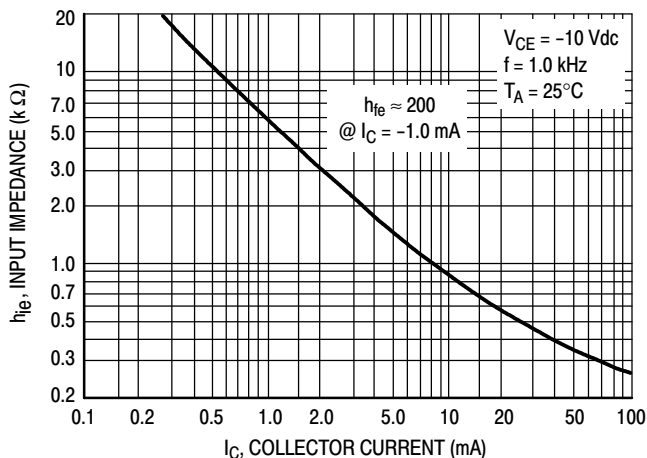


Figure 15. Input Impedance

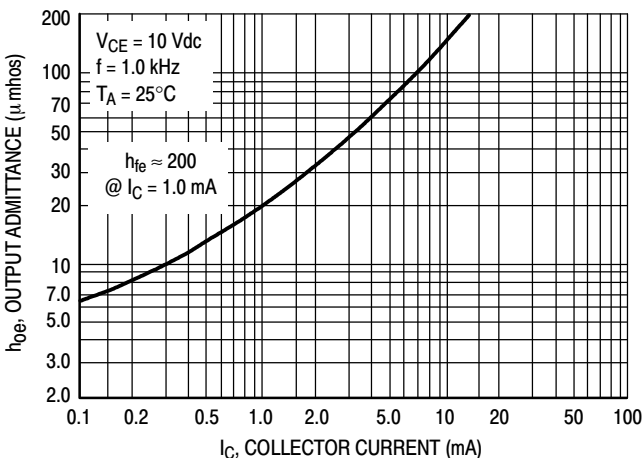


Figure 16. Output Admittance

# MMBTA70LT1G

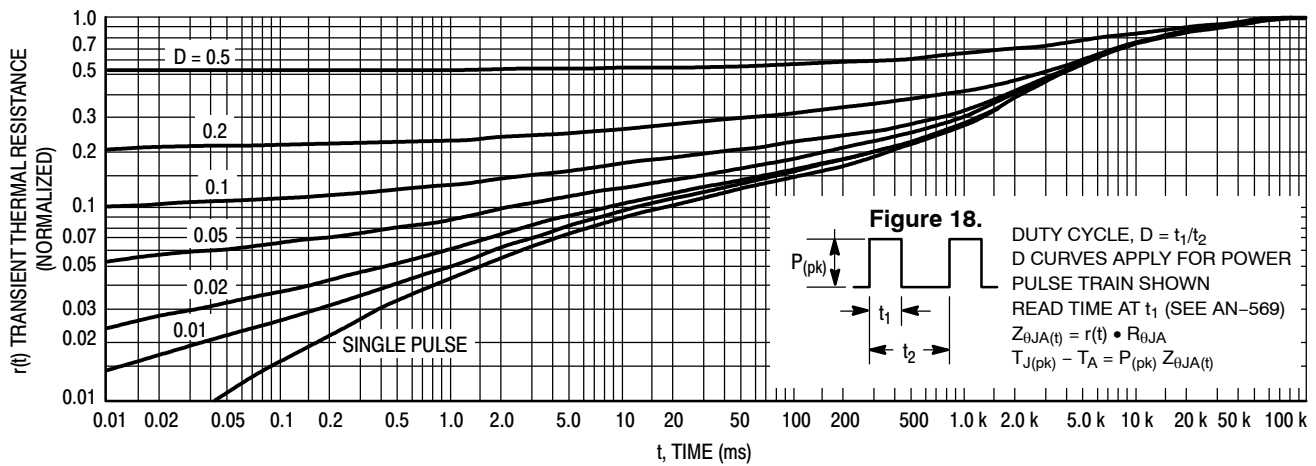


Figure 17. Thermal Response

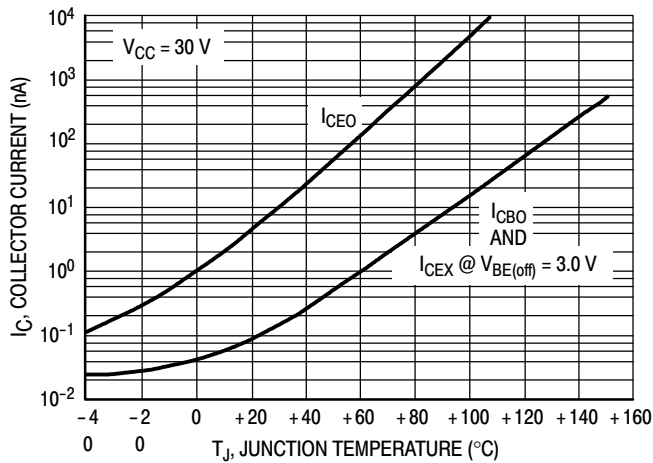


Figure 19. Typical Collector Leakage Current

## DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 18. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 17 was calculated for various duty cycles.

To find  $Z_{\theta JA(t)}$ , multiply the value obtained from Figure 17 by the steady state value  $R_{\theta JA}$ .

Example:

Dissipating 2.0 watts peak under the following conditions:

$$t_1 = 1.0 \text{ ms}, t_2 = 5.0 \text{ ms} (D = 0.2)$$

Using Figure 17 at a pulse width of 1.0 ms and  $D = 0.2$ , the reading of  $r(t)$  is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^\circ\text{C}.$$

For more information, see AN-569.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



**SOT-23 (TO-236)**  
CASE 318-08  
ISSUE AS

DATE 30 JAN 2018

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**RECOMMENDED SOLDERING FOOTPRINT**



**GENERIC MARKING DIAGRAM\***



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- |   |   |   |  |
|---|---|---|--|
| STYLE 1 THRU 5:<br>CANCELLED                                | STYLE 6:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR       | STYLE 7:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR       | STYLE 8:<br>PIN 1. ANODE<br>2. NO CONNECTION<br>3. CATHODE |
| STYLE 9:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE          | STYLE 10:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE           | STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 12:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE      |
| STYLE 13:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE           | STYLE 14:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          | STYLE 15:<br>PIN 1. GATE<br>2. CATHODE<br>3. ANODE          | STYLE 16:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE      |
| STYLE 17:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. CATHODE | STYLE 18:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. ANODE | STYLE 19:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE-ANODE | STYLE 20:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE         |
| STYLE 21:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN           | STYLE 22:<br>PIN 1. RETURN<br>2. OUTPUT<br>3. INPUT         | STYLE 23:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE         | STYLE 24:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE          |
| STYLE 25:<br>PIN 1. ANODE<br>2. CATHODE<br>3. GATE          | STYLE 26:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION | STYLE 27:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE     | STYLE 28:<br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE          |

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