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November 2013

FDP12N50 / FDPF12N50T N-Channel UniFETTM MOSFET 500 V, 11.5 A, 650 m Ω

Features

- $R_{DS(on)}$ = 550 $m\Omega$ (Typ.) @ V_{GS} = 10 V, I_D = 6 A
- Low Gate Charge (Typ. 22 nC)
- Low C_{rss} (Typ. 11 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

Applications

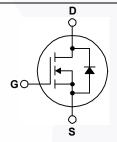
- LCD/LED/PDP TV
- · Lighting
- · Uninterruptible Power Supply

Description

UniFETTM MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDP12N50	FDPF12N50T	Unit	
V_{DSS}	Drain to Source Voltage	rain to Source Voltage			500		
V_{GSS}	Gate to Source Voltage	Gate to Source Voltage			:30	V	
	Drain Current	- Continuous (T _C = 25°C)		11.5	11.5 *	Α	
ID	DialifCullent	- Continuous (T _C = 100°C)		6.9	6.9 *		
I _{DM}	Drain Current	- Pulsed	(Note 1)	46	46 *	Α	
E _{AS}	Single Pulsed Avalanche E	Single Pulsed Avalanche Energy (Note 2)			56	mJ	
I _{AR}	Avalanche Current	Avalanche Current (Note 1)			1.5	Α	
E _{AR}	Repetitive Avalanche Energ	gy	(Note 1)	1) 16.7		mJ	
dv/dt	Peak Diode Recovery dv/d	t	(Note 3)	4	1.5	V/ns	
В	Power Dissipation	(T _C = 25°C)		165	42	W	
P_{D}	Power Dissipation	- Derate Above 25°C		1.33	0.3	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to	o +150	°C	
TL	Maximum Lead Temperatu	re for Soldering, 1/8" from Case for	5 Seconds	3	00	°С	

^{*}Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP12N50	FDPF12N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.75	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	-C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP12N50	FDP12N50	TO-220	Tube	N/A	N/A	50 units
FDPF12N50T	FDPF12N50T	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	500	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.5	-	V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	-	-	1	^
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 400 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μΑ
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$	-	0.55	0.65	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 6 A	ı	11.5	ı	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V/ 05 V/ V/ 0 V/		-	985	1315	pF
C _{oss}	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-	140	190	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12		- \	11	17	pF
Q_g	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 11.5 A,		- \	22	30	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V		-	6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	9	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	24	60	ns
t _r		$V_{DD} = 250 \text{ V}, I_D = 11.5 \text{ A},$	-	50	110	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_G = 25 Ω	-	45	100	ns
t _f	Turn-Off Fall Time	(Note 4)	-	30	70	ns

Drain-Source Diode Characteristics

Is	Maximum Continuous Drain to Source Dioc	Maximum Continuous Drain to Source Diode Forward Current		-	11.5	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Fo	orward Current	-	-	46	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 11.5 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 11.5 A,	-	375	/ -	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs	-	3.5	-	μС

Notes

- ${\it 1. Repetitive\ rating: pulse-width\ limited\ by\ maximum\ junction\ temperature.}$
- 2. L = 6.9 mH, I_{AS} = 11.5 A, V_{DD} = 50 V, R_{G} = 25 Ω , starting T_{J} = 25°C.
- 3. $I_{SD} \le 11.5$ A, di/dt ≤ 200 A/ μ s, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.



Typical Performance Characteristics

Figure 1. On-Region Characteristics

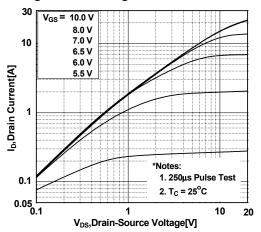


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

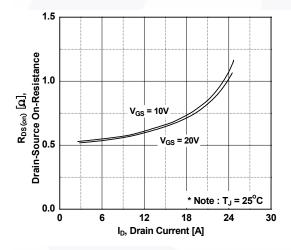


Figure 5. Capacitance Characteristics

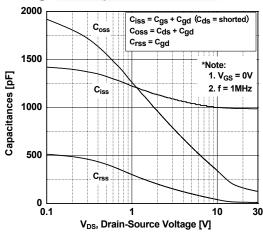


Figure 2. Transfer Characteristics

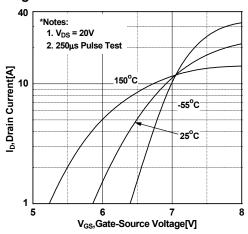


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

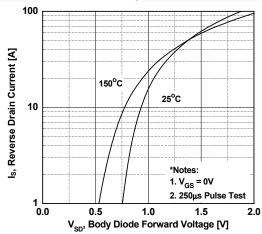
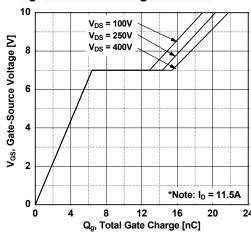


Figure 6. Gate Charge Characteristics



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Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

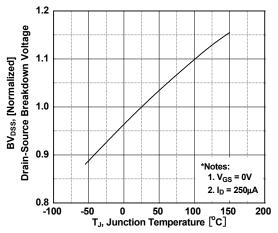


Figure 9-1. Maximum Safe Operating Area - FDP12N50

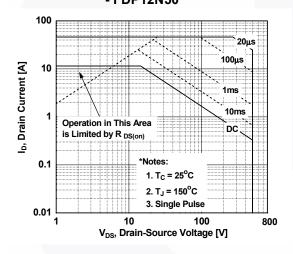


Figure 8. On-Resistance Variation vs. Temperature

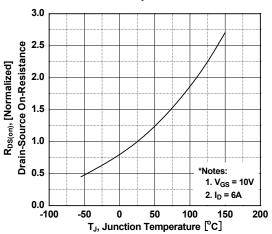


Figure 9-2. Maximum Safe Operating Area - FDPF12N50T

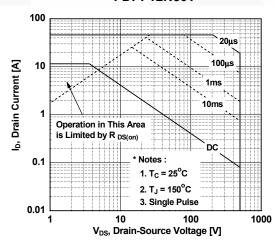
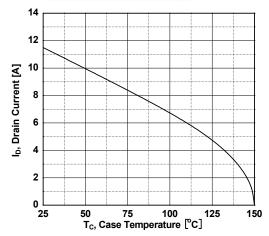


Figure 10. Maximum Drain Current vs. Case Temperature



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Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve - FDP12N50

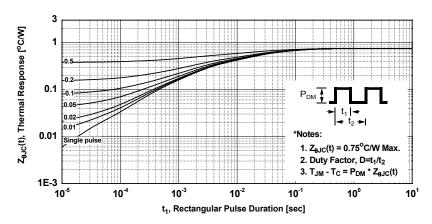
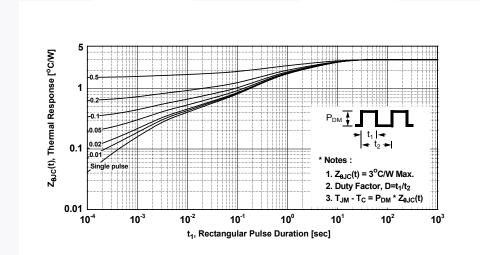


Figure 11-2. Transient Thermal Response Curve - FDPF12N50T



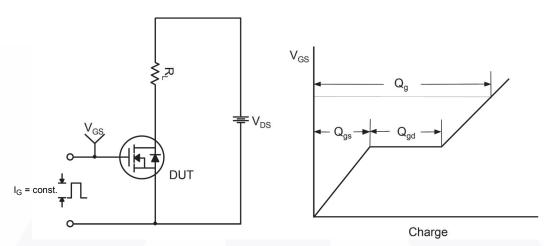


Figure 12. Gate Charge Test Circuit & Waveform

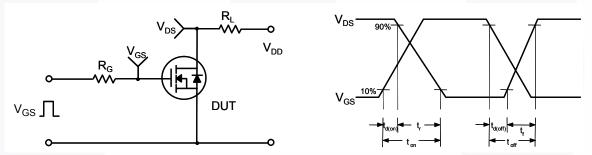


Figure 13. Resistive Switching Test Circuit & Waveforms

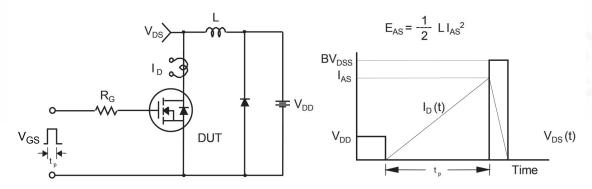


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

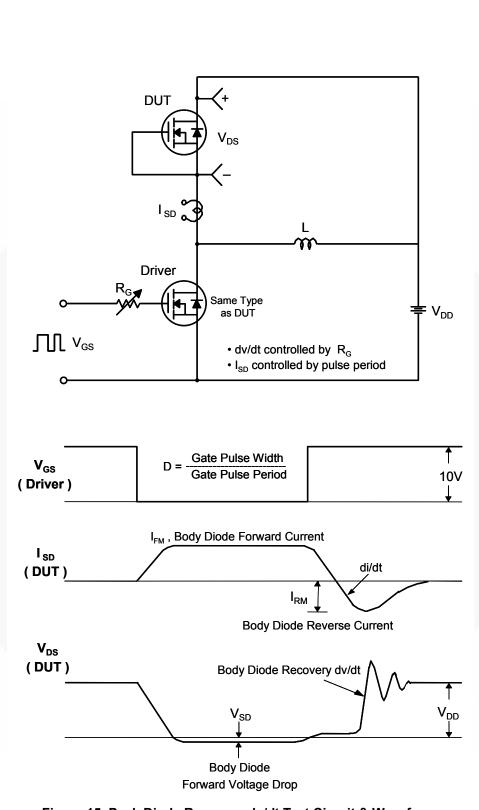


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

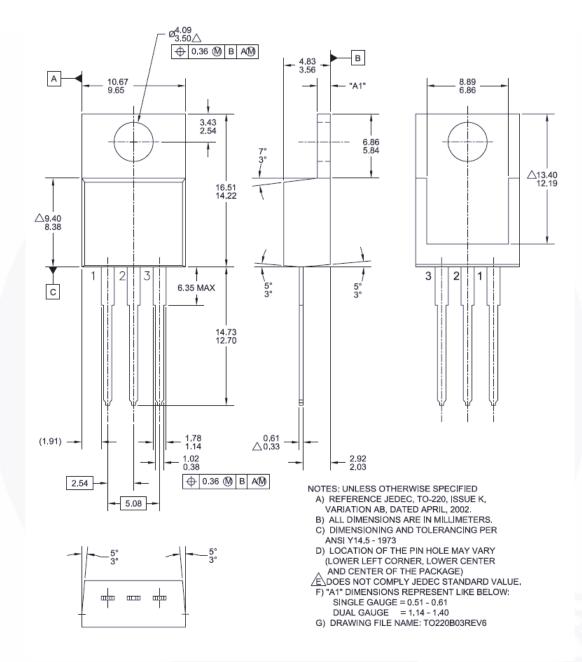


Figure 16. TO-220, Molded, 3-Lead, Jedec Variation AB

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Mechanical Dimensions

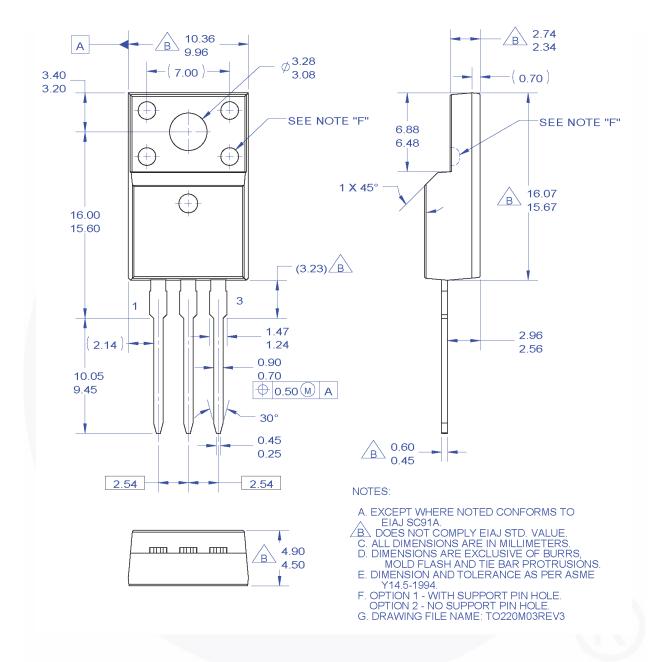


Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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