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FDD6682/FDU6682

30V N-Channel PowerTrench[®] MOSFET

General Description

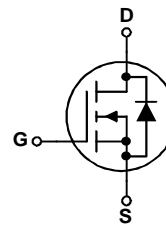
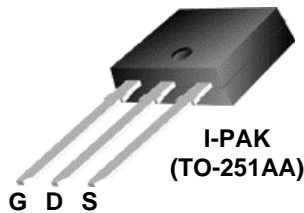
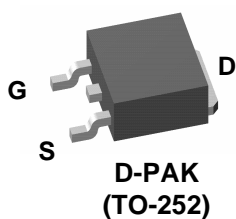
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

- DC/DC converter
- Motor Drives

Features

- 75 A, 30 V $R_{DS(ON)} = 6.2 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 8.0 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Low gate charge
- Fast switching
- High performance trench technology for extremely low $R_{DS(ON)}$



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	
I_D	Drain Current – Continuous (Note 3)	75	A
	– Pulsed (Note 1a)	100	
P_D	Power Dissipation for Single Operation (Note 1)	71	W
	(Note 1a)	3.8	
	(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+175$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6682	FDD6682	D-PAK (TO-252)	13"	12mm	2500 units
FDU6682	FDU6682	I-PAK (TO-251)	Tube	N/A	75

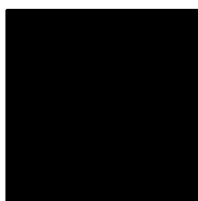
Electrical Characteristics <small>T_A = 25°C unless otherwise noted</small>						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
W _{DSS}	Drain-Source Avalanche Energy	Single Pulse, V _{DD} = 15 V, I _D = 17 A			240	mJ
I _{AR}	Drain-Source Avalanche Current				17	A
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		20		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate-Body Leakage	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		-7		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 17 A V _{GS} = 4.5 V, I _D = 15 A V _{GS} = 10 V, I _D = 17 A, T _J = 125°C		5.2 6.4 8.0	6.2 8 11.9	mΩ
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	50			A
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 17 A		65		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz		2400		pF
C _{oss}	Output Capacitance			577		pF
C _{riss}	Reverse Transfer Capacitance			258		pF
R _G	Gate Resistance	V _{GS} = 15 mV, f = 1.0 MHz		1.4		Ω
Switching Characteristics (Note 2)						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		14	20	ns
t _r	Turn-On Rise Time			12	37	ns
t _{d(off)}	Turn-Off Delay Time			38	64	ns
t _f	Turn-Off Fall Time			18	32	ns
Q _g	Total Gate Charge	V _{DS} = 15V, I _D = 17 A, V _{GS} = 5 V		24	31	nC
Q _{gs}	Gate-Source Charge			6.5		nC
Q _{gd}	Gate-Drain Charge			8.1		nC

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				3.2	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.2\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 17\text{ A}, d_i/d_t = 100\text{ A}/\mu\text{s}$		32		nS
Q_{rr}	Diode Reverse Recovery Charge			20		nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA} = 40^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $R_{\theta JA} = 96^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

- Maximum current is calculated as:
$$\sqrt{\frac{P_D}{R_{DS(ON)}}}$$

where P_D is maximum power dissipation at $T_C = 25^\circ\text{C}$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10\text{V}$. Package current limitation is 21A

Typical Characteristics

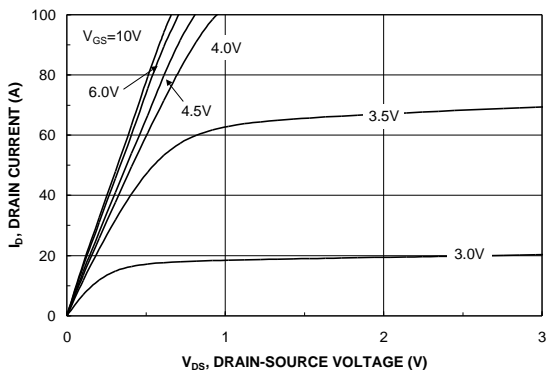


Figure 1. On-Region Characteristics.

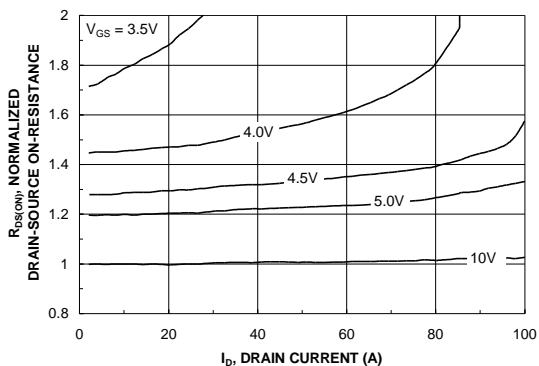


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

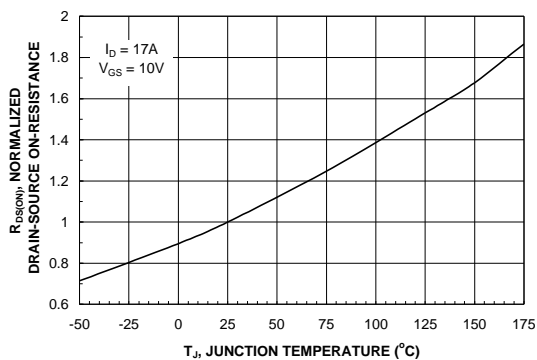


Figure 3. On-Resistance Variation with Temperature.

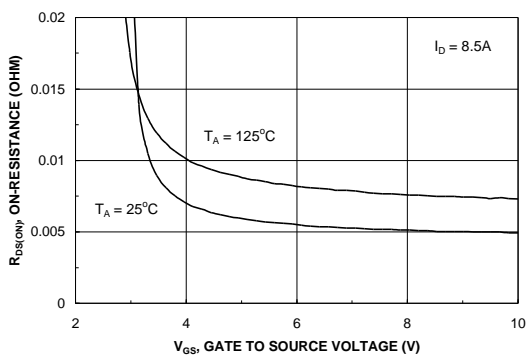


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

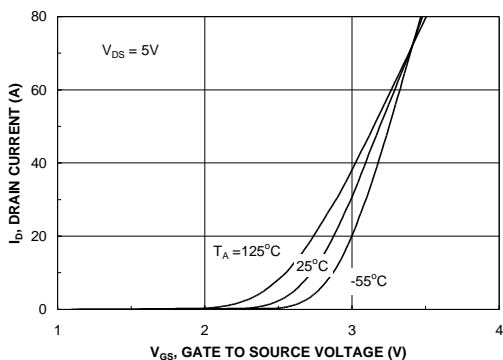


Figure 5. Transfer Characteristics

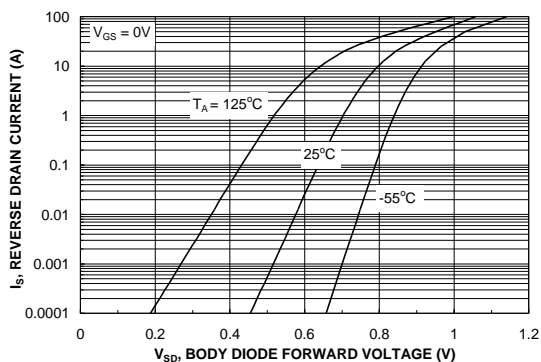


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

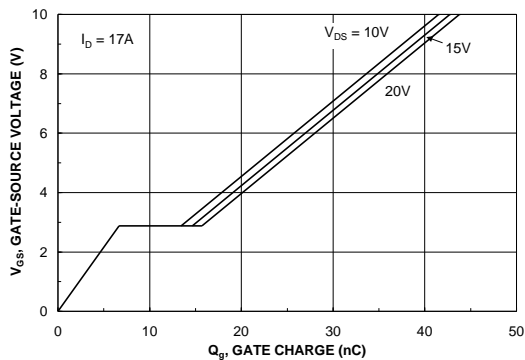


Figure 7. Gate Charge Characteristics

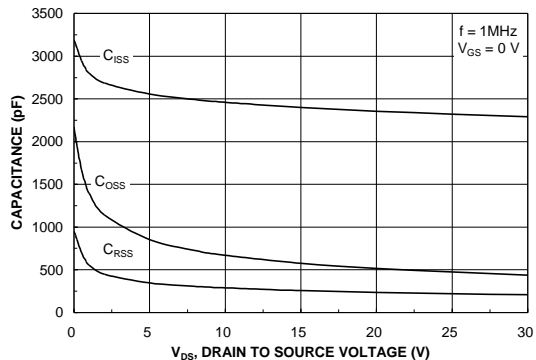


Figure 8. Capacitance Characteristics

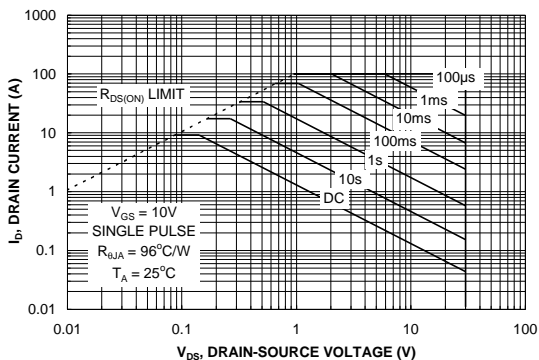


Figure 9. Maximum Safe Operating Area

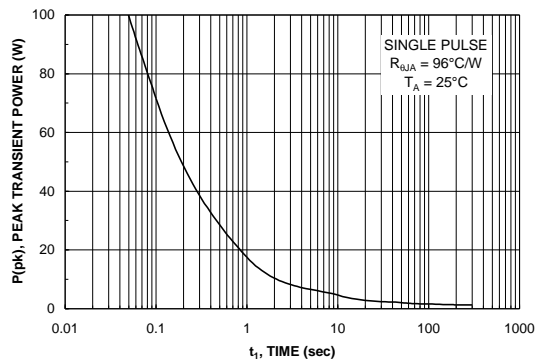


Figure 10. Single Pulse Maximum Power Dissipation

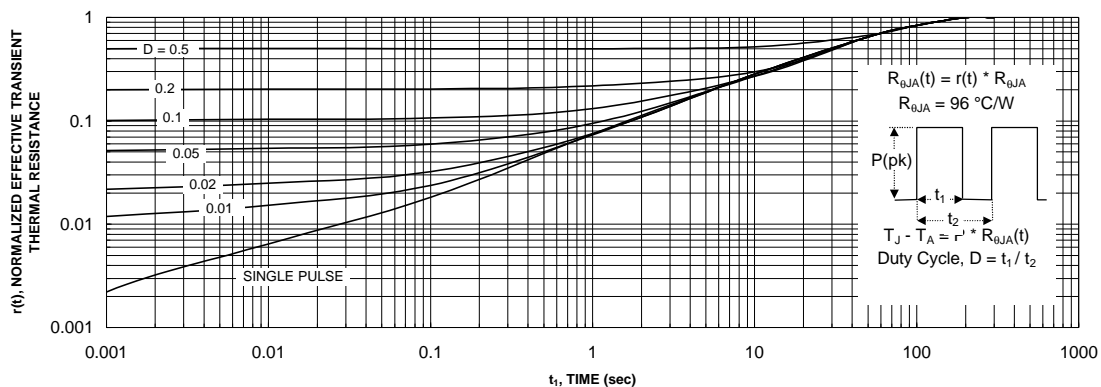


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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