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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

June 2013

FDMB3900AN

Dual N-Channel PowerTrench® MOSFET

25 V, 7.0 A, 23 mΩ

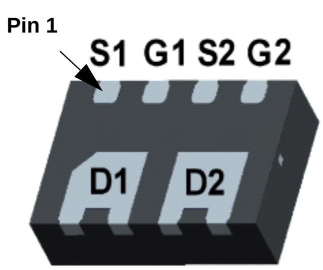
Features

- Max $r_{DS(on)}$ = 23 mΩ at V_{GS} = 10 V, I_D = 7.0 A
- Max $r_{DS(on)}$ = 33 mΩ at V_{GS} = 4.5 V, I_D = 5.5 A
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- RoHS Compliant

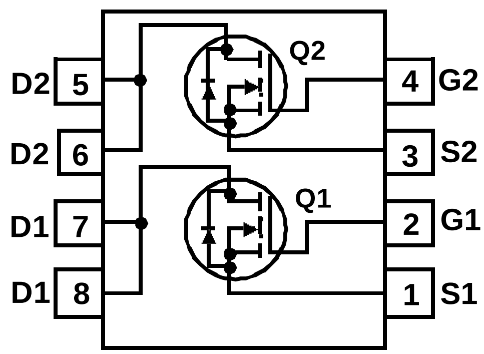
General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where the low in-line power loss and fast switching are required.



MicroFET 3X1.9



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			25	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_A = 25 °C	(Note 1a)	7.0	A
	-Pulsed			28	
P_D	Power Dissipation	T_A = 25 °C	(Note 1a)	1.6	W
	Power Dissipation	T_A = 25 °C	(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	165	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
3900	FDMB3900AN	MicroFET 3X1.9	7 ”	8 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		17		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7.0 A		19	23	mΩ
		V_{GS} = 4.5 V, I_D = 5.5 A		26	33	
		V_{GS} = 10 V, I_D = 7.0 A, T_J = 125 °C		26	32	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7.0 A		27		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 13 V, V_{GS} = 0 V, f = 1MHz		650	890	pF
C_{oss}	Output Capacitance			151	200	pF
C_{rss}	Reverse Transfer Capacitance			141	215	pF
R_g	Gate Resistance			0.8		Ω

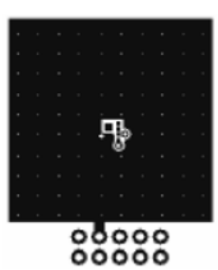
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 13 V, I_D = 7.0 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		6	12	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			15	26	ns
t_f	Fall Time			3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 13 V, I_D = 7.0 A		11	17	nC
	Total Gate Charge	V_{GS} = 0 V to 5 V		7	10	nC
Q_{gs}	Gate to Source Charge			2.0		nC
Q_{gd}	Gate to Drain “Miller” Charge			3.0		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)		0.8	1.2	V
		V_{GS} = 0 V, I_S = 7.0 A (Note 2)		0.9	1.2	
t_{rr}	Reverse Recovery Time	I_F = 7.0 A, di/dt = 100 A/μs		14	24	ns
Q_{rr}	Reverse Recovery Charge			3	10	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 80 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b.165 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

Typical Characteristics T_J = 25°C unless otherwise noted

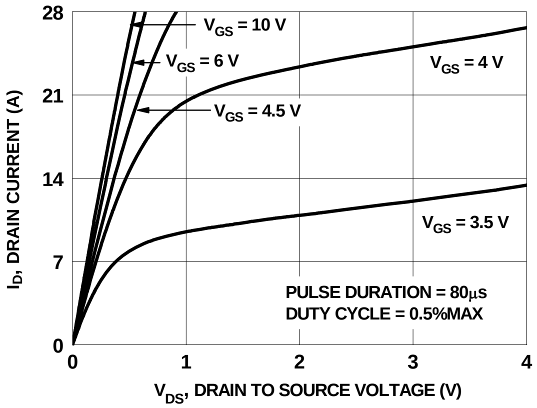


Figure 1. On-Region Characteristics

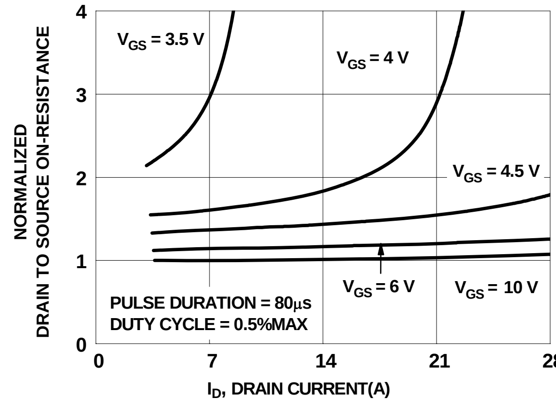


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

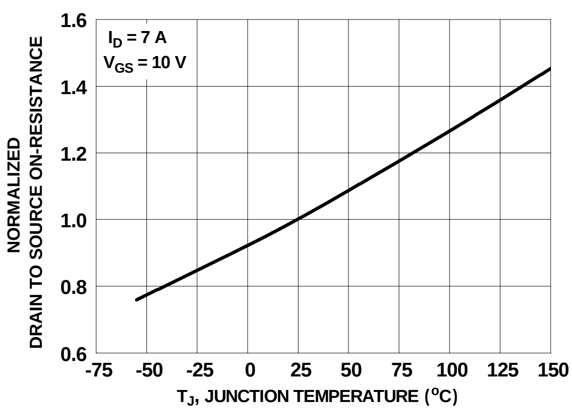


Figure 3. Normalized On-Resistance vs Junction Temperature

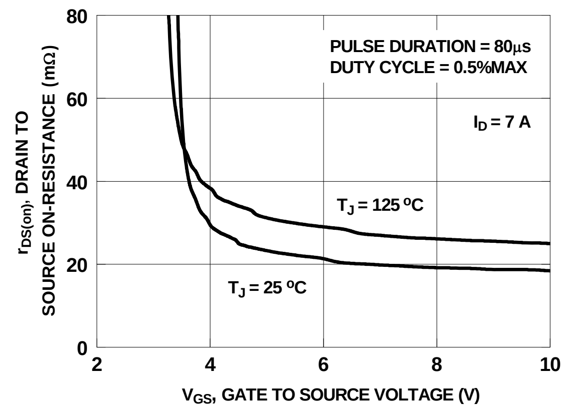


Figure 4. On-Resistance vs Gate to Source Voltage

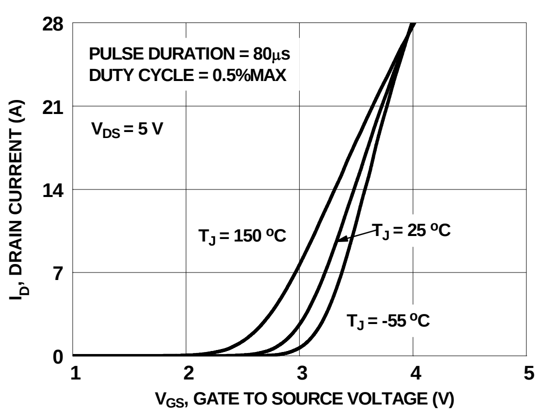


Figure 5. Transfer Characteristics

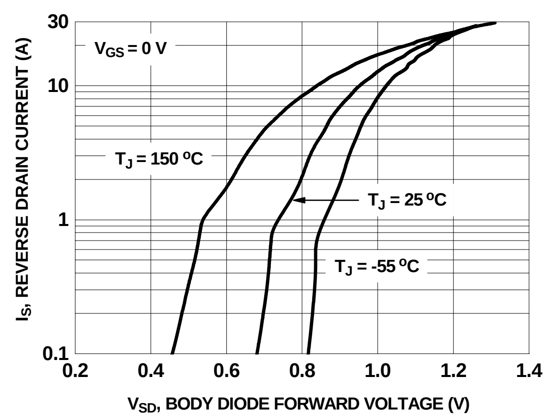


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

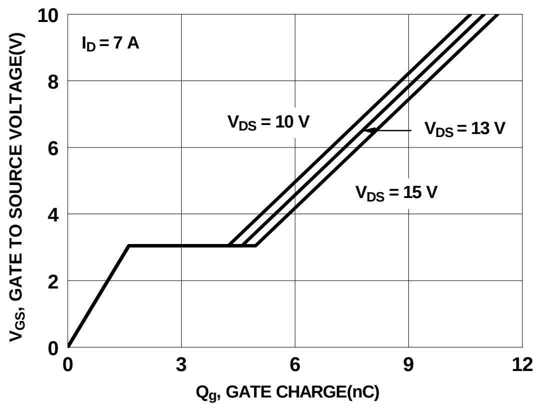


Figure 7. Gate Charge Characteristics

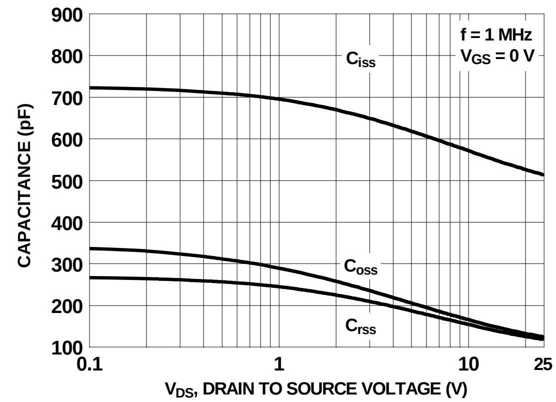


Figure 8. Capacitance vs Drain to Source Voltage

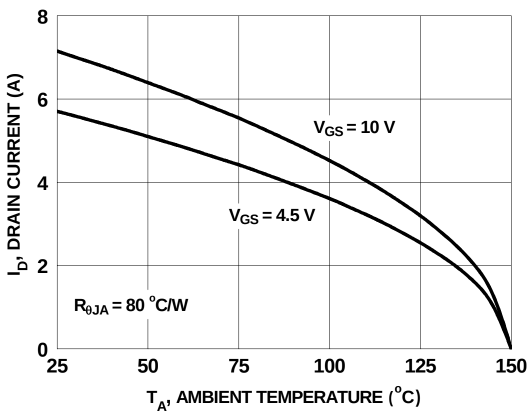


Figure 9. Maximum Continuous Drain Current vs Ambient Temperature

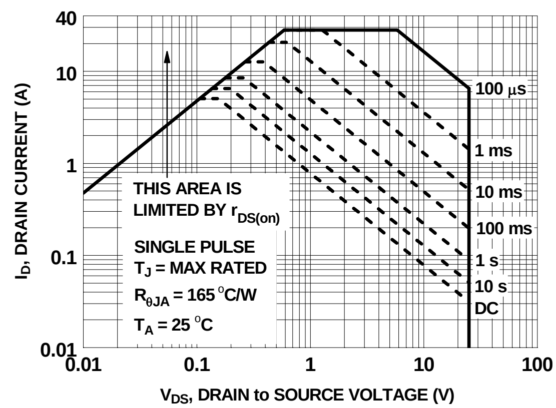


Figure 10. Forward Bias Safe Operating Area

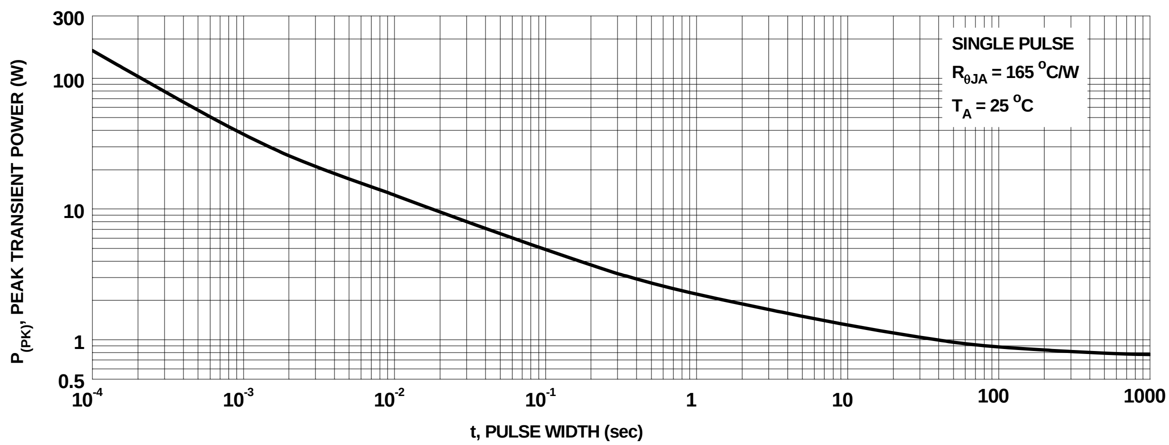


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

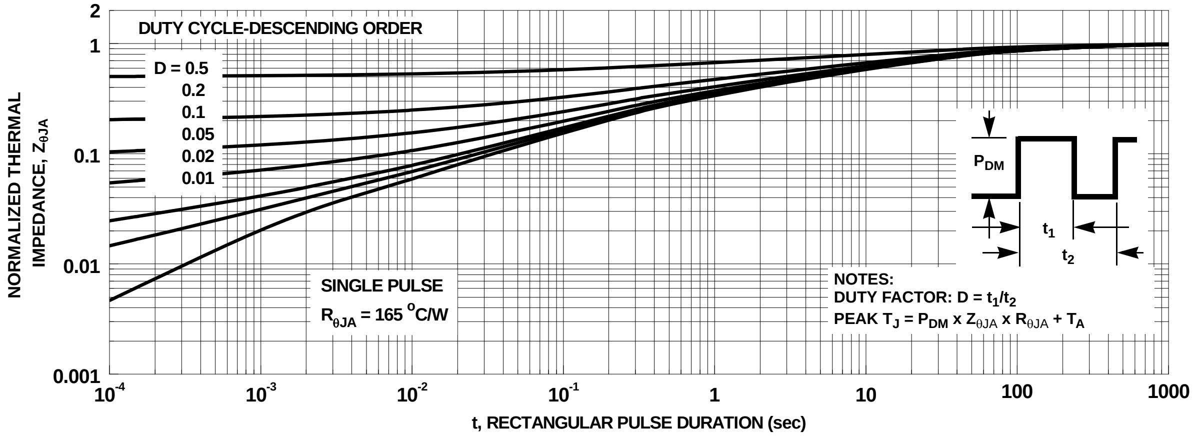
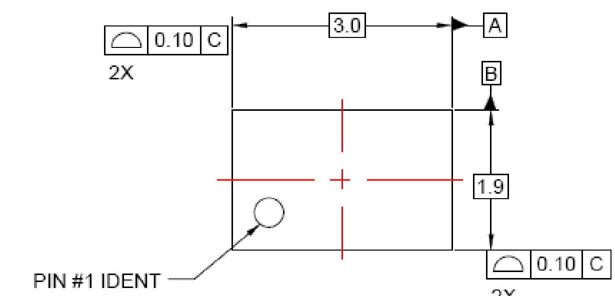
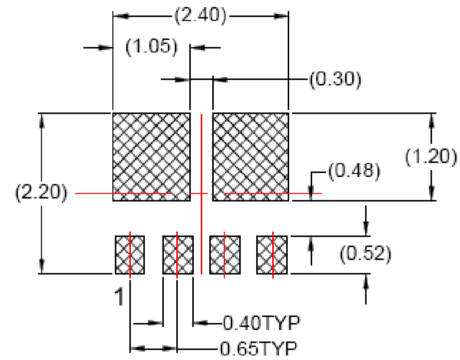


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

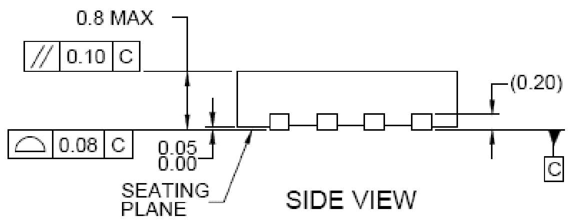
Dimensional Outline and Pad Layout



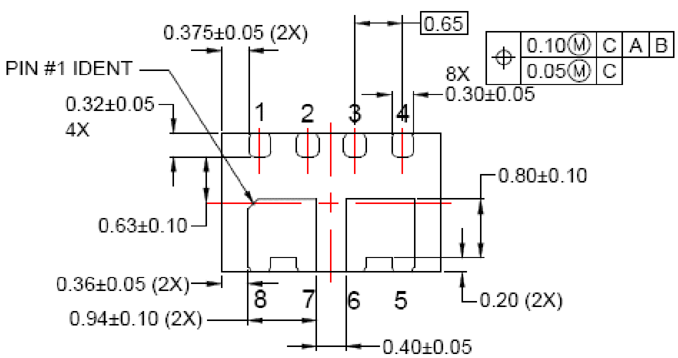
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. DOES NOT FULLY CONFORM TO JEDED REGISTRATION MO-229.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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