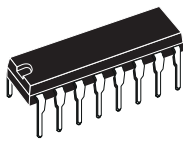
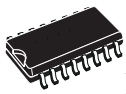
HCF40103B

8-STAGE PRESETTABLE SYNCHRONOUS 8 BIT BINARY DOWN COUNTERS

- SYNCHRONOUS OR ASYNCHRONOUS PRESET
- MEDIUM -SPEED OPERATION : f_{CL} =3.6MHz (Typ.) at V_{DD} = 10V
- CASCADABLE
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP



SOP

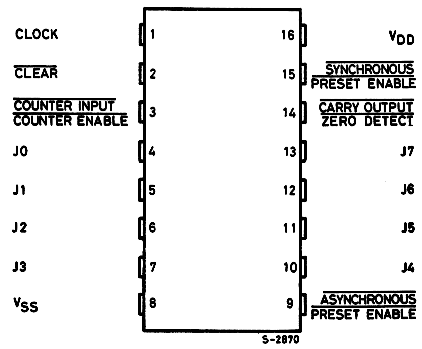
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF40103BEY	
SOP	HCF40103BM1	HCF40103M013TR

DESCRIPTION

HCF40103B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
HCF40103B consists of an 8-stage synchronous down counter with a single output that is active when the internal count is zero. This device contains a single 8-bit binary counter. It has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO DETECT output are active-low logics. In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI}$/$\overline{CE}$) input is high. The $\overline{CARRY\text{-}OUT/ZERO\ DETECT}$ ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period. When the $\overline{SYNCHRONOUS\ PRESET\ ENABLE}$ ($\overline{SPE}$) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input. When the $\overline{ASYNCHRONOUS\ PRESET\ ENABLE}$ ($\overline{APE}$) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. JAM inputs J0-J7 represent a single 8 bit binary word. When the CLEAR ($\overline{CLR}$) input is low, the counter is asynchronously cleared to its maximum count (255_{10}) regardless of the state of any other input. The precedent relationship between control input is indicated in the truth table. If all control

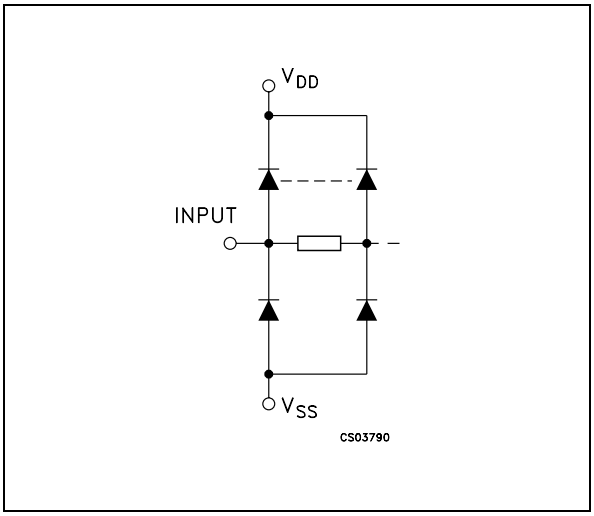
PIN CONNECTION



inputs are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.

HCF40103B may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode.

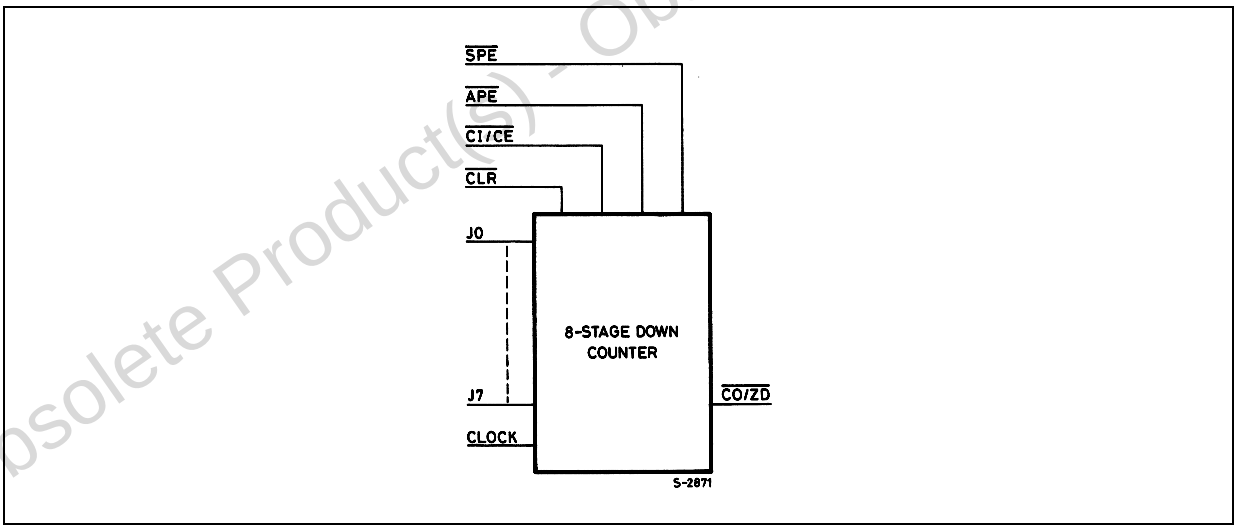
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK	Clock Input (LOW to HIGH edge triggered)
2	$\overline{CLEAR}$	Asynchronous Master Reset Input (Active Low)
3	$\overline{CI/CE}$	Terminal Enable Input
4, 5, 6, 7, 10, 11, 12, 13	J0 to J7	Jam Inputs
9	$\overline{APE}$	Asynchronous Preset Enable Inputs(Active Low)
14	$\overline{CO/ZD}$	Terminal Count Output (Active Low)
15	$\overline{SPE}$	Synchronous Preset Enable Input (Active Low)
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM

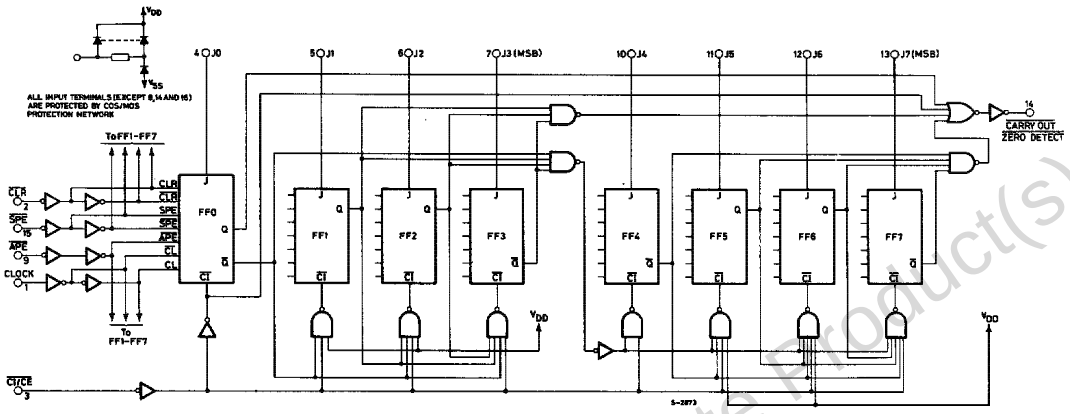


TRUTH TABLES

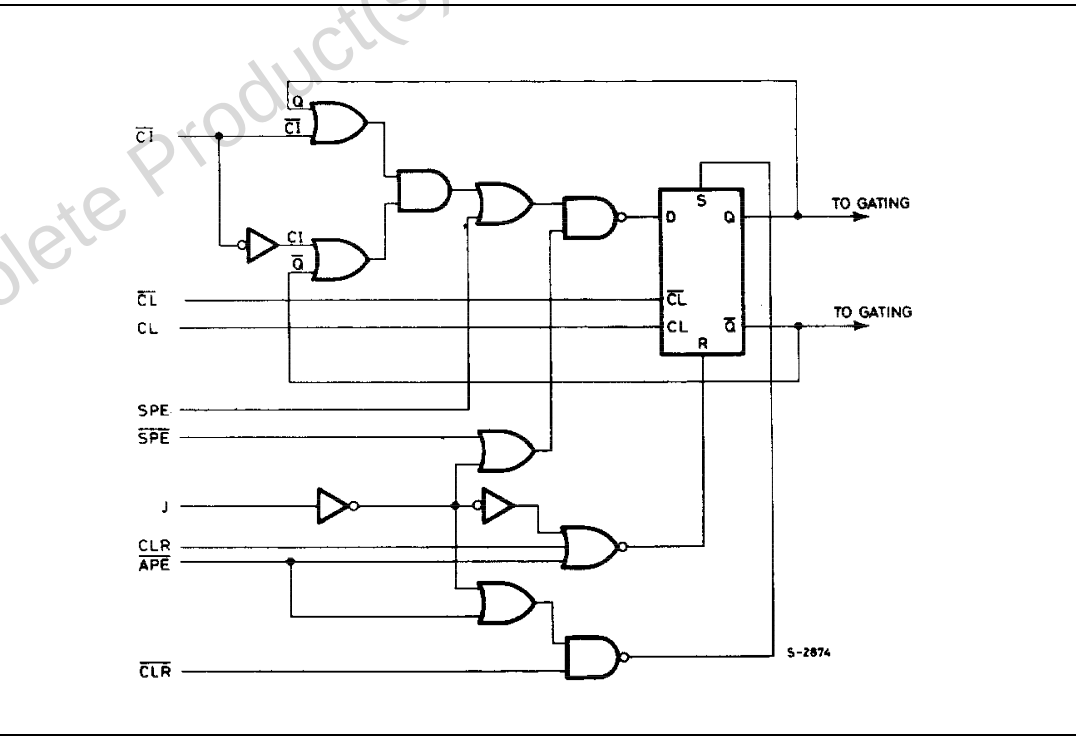
CONTROL INPUTS				PRESET MODE	ACTION
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	Synchronous	Inhibit Counter
H	H	H	L		Count Down
H	H	L	X		Preset on Next Positive Clock Transition
H	L	X	X	Asynchronous	Preset Asynchronously
L	X	X	X		Clear to Maximum Count

X : Don't Care
Clock connected to Clock input
Synchronous Operation : changes occur on negative to positive clock transitions.

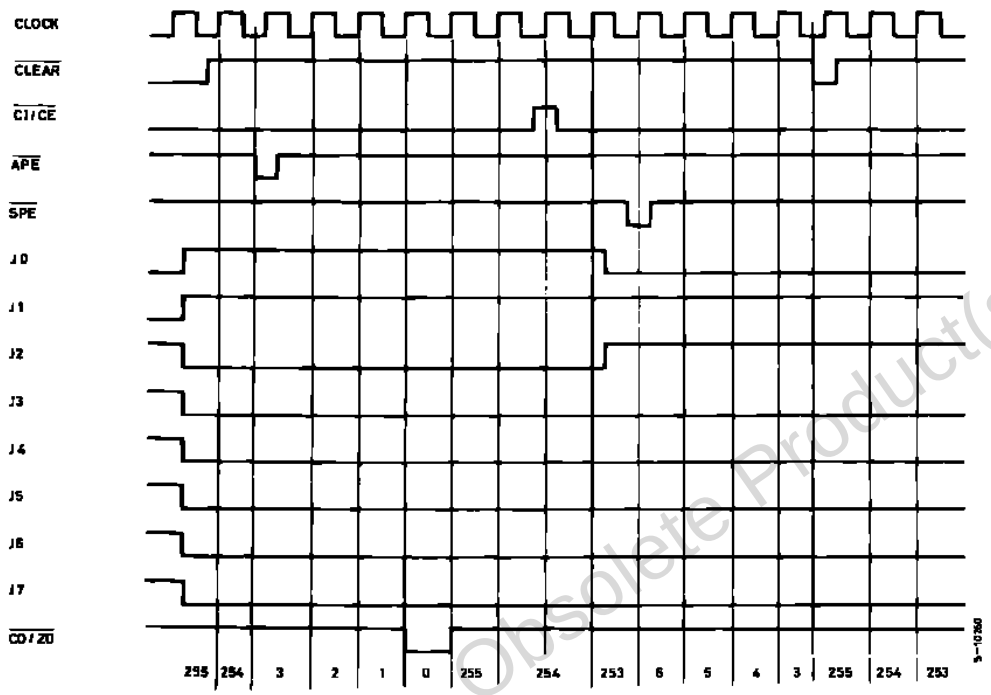
LOGIC DIAGRAM



LOGIC DIAGRAM FOR FLIP-FLOPS, FF0-FF7



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

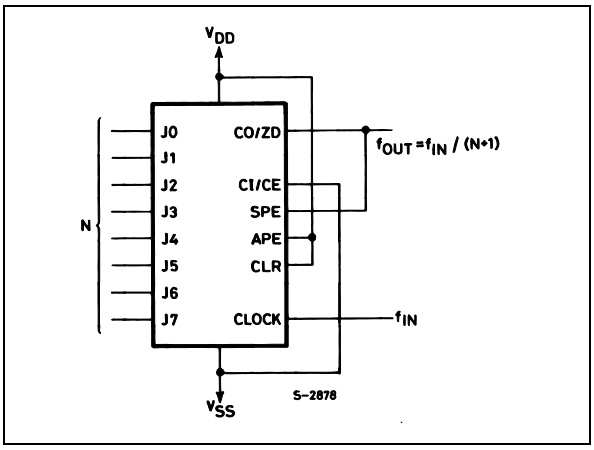
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time Clock To Out	5			300	600	ns
		10			130	260	
		15			95	190	
t_{PHL} t_{PLH}	Propagation Delay Time Carry In/counter Enable To Output	5			200	400	ns
		10			90	180	
		15			65	130	
t_{PHL} t_{PLH}	Propagation Delay Time Asynchronous Preset Enable To Output	5			650	1300	ns
		10			300	600	
		15			200	400	
t_{PHL} t_{PLH}	Propagation Delay Time $\overline{\text{Clear}}$ To Output	5			375	750	ns
		10			180	360	
		15			100	200	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Clock Pulse Width	5		300	150		ns
		10		180	90		
		15		80	40		
t_W	$\overline{\text{Clear}}$ Pulse Width	5		320	160		ns
		10		160	80		
		15		100	50		
t_W	$\overline{\text{APE}}$ Pulse Width	5		360	180		ns
		10		160	80		
		15		120	60		
t_{setup}	$\overline{\text{SPE}}$ Setup Time	5		280	140		ns
		10		140	70		
		15		100	50		
t_{setup}	JAM Setup Time	5		200	100		ns
		10		80	40		
		15		60	30		
f_{CL}	Maximum Clock Input Frequency	5		0.7	1.4		MHz
		10		1.8	3.6		
		15		2.4	4.8		

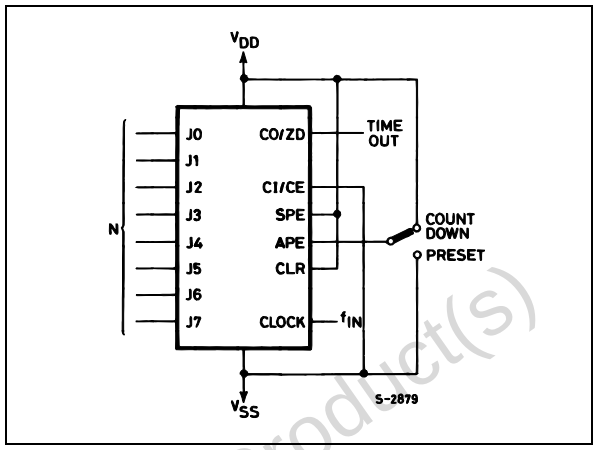
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TYPICAL APPLICATIONS

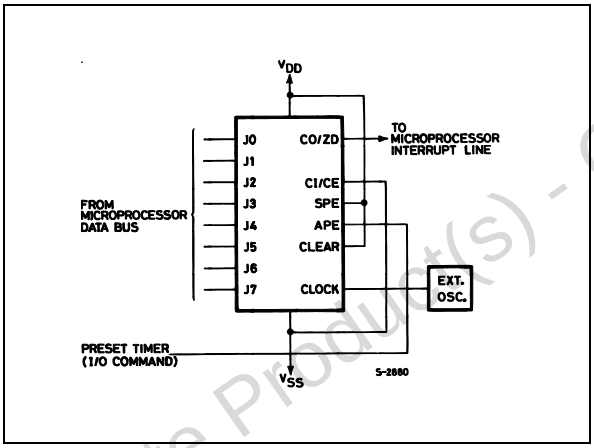
DIVIDE BY "N" COUNTER



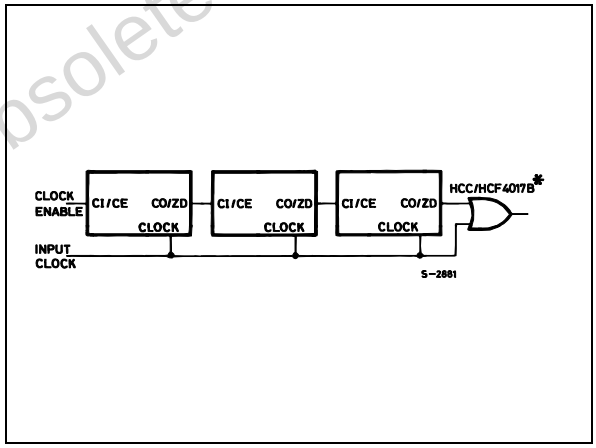
SYNCHRONOUS CASCADING



MICROPROCESSOR INTERRUPT TIMER

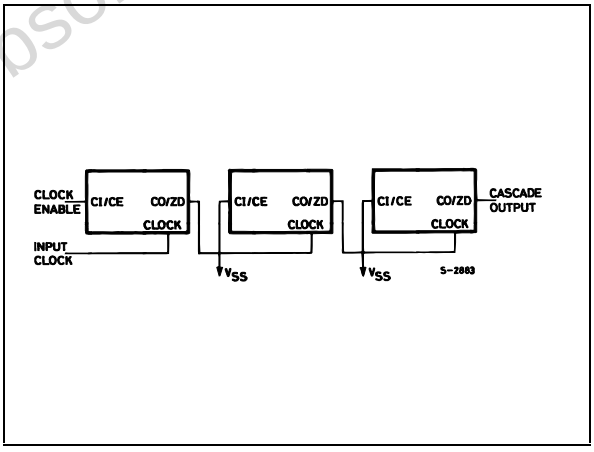


SYNCHRONOUS CASCADING

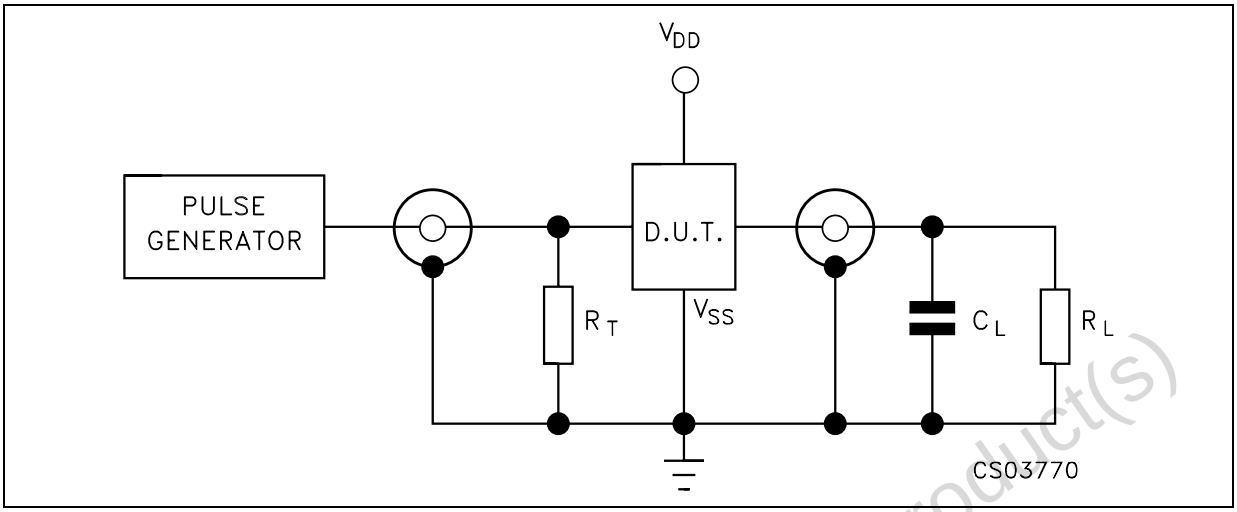


* An Output spike (160ns at V_{DD} = 5V) occurs whenever two or more devices are cascaded in the parallel clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry-out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

MICROPROCESSOR INTERRUPT TIMER

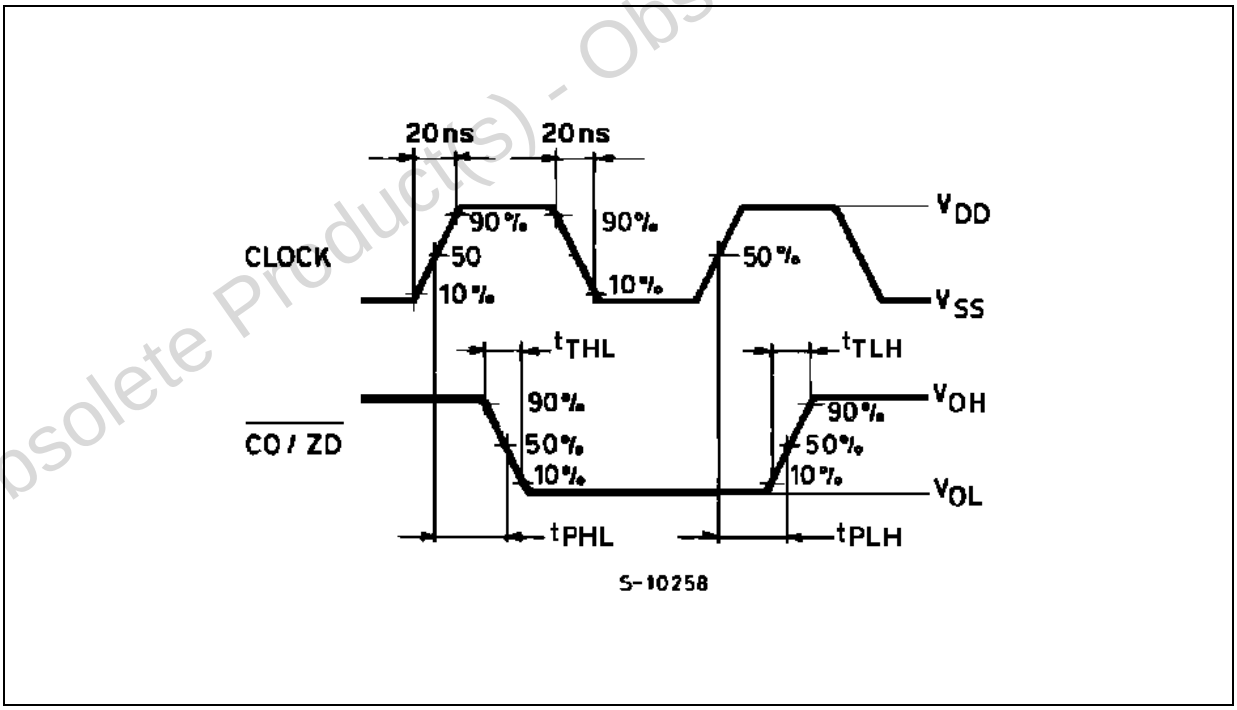


TEST CIRCUIT

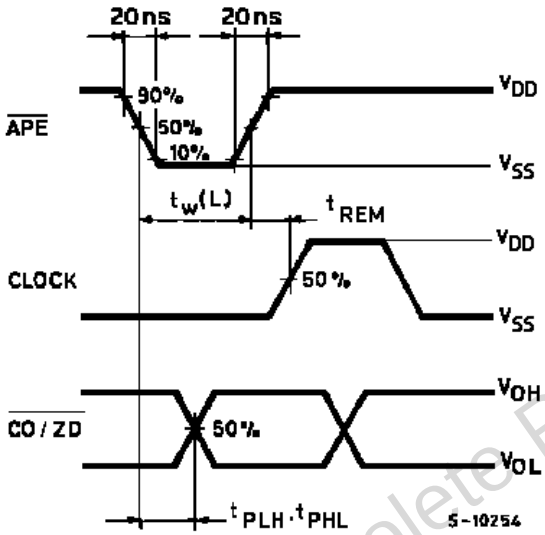


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

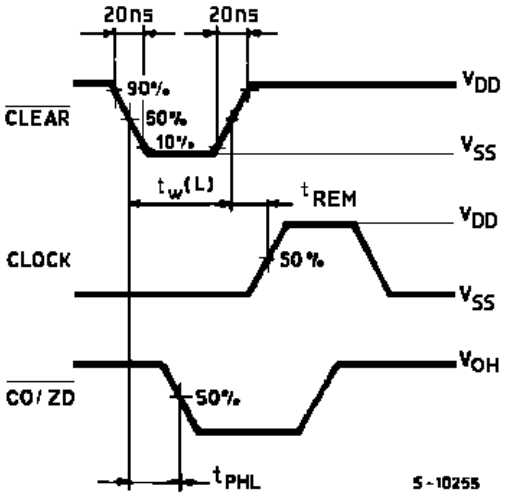
WAVEFORM 1 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



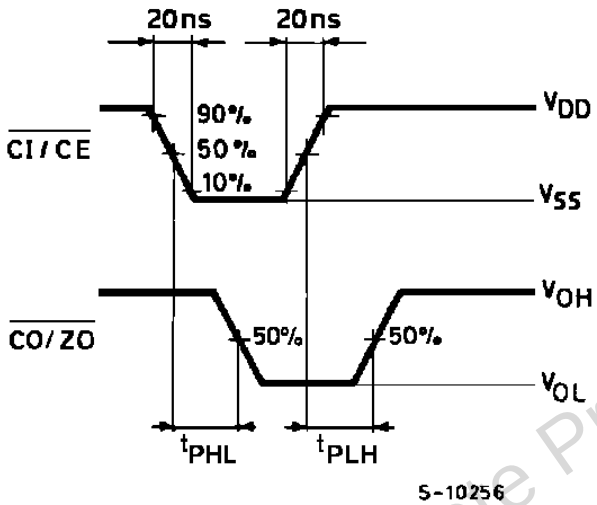
WAVEFORM 2 : PROPAGATION DELAY, MINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)



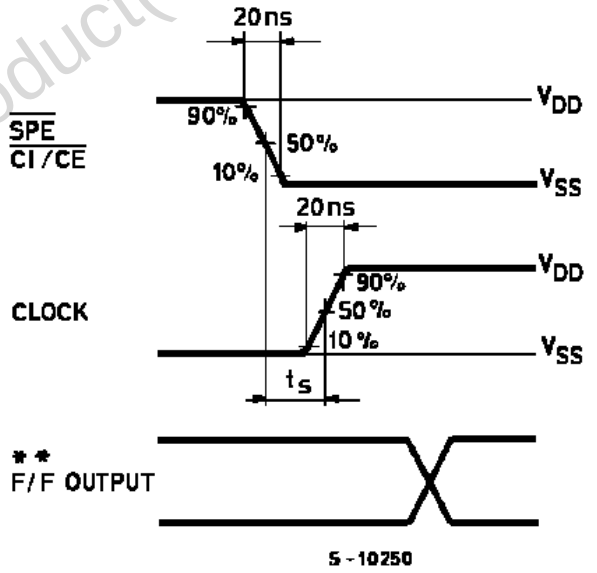
WAVEFORM 3 : PROPAGATION DELAY, MINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)



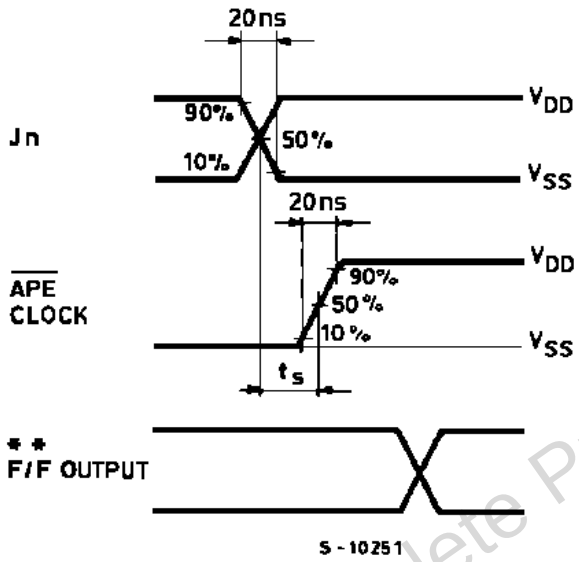
WAVEFORM 4 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



WAVEFORM 5 : MINIMUM SETUP TIME (f=1MHz; 50% duty cycle)

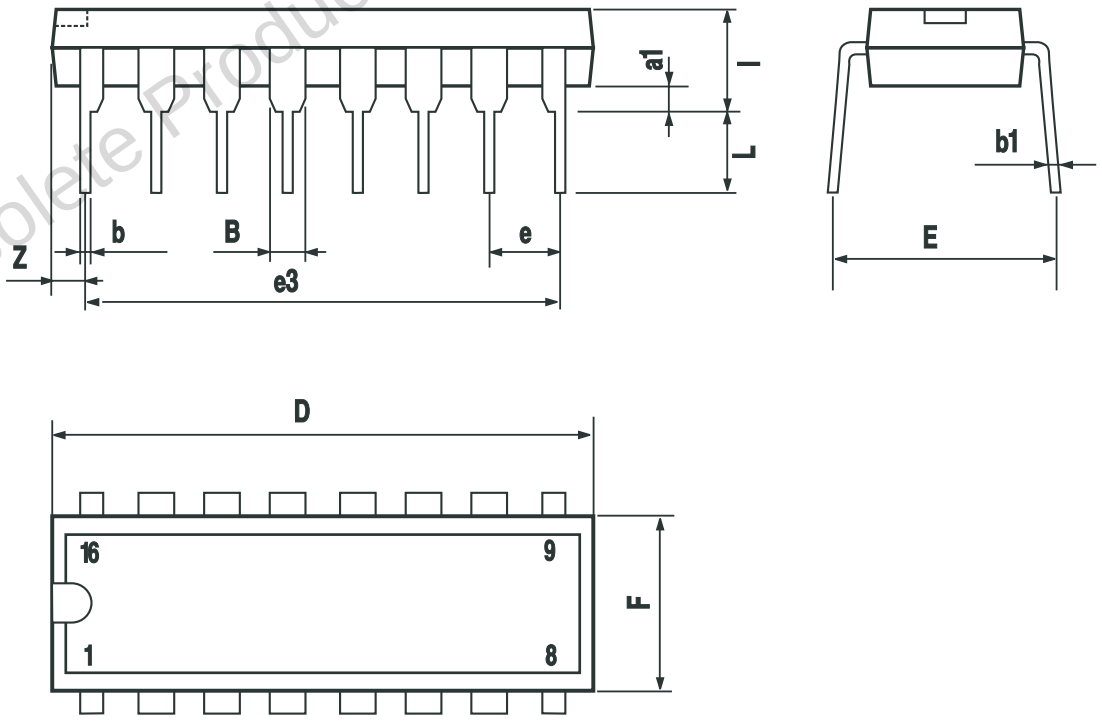


WAVEFORM 6 : MINIMUM SETUP TIME (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

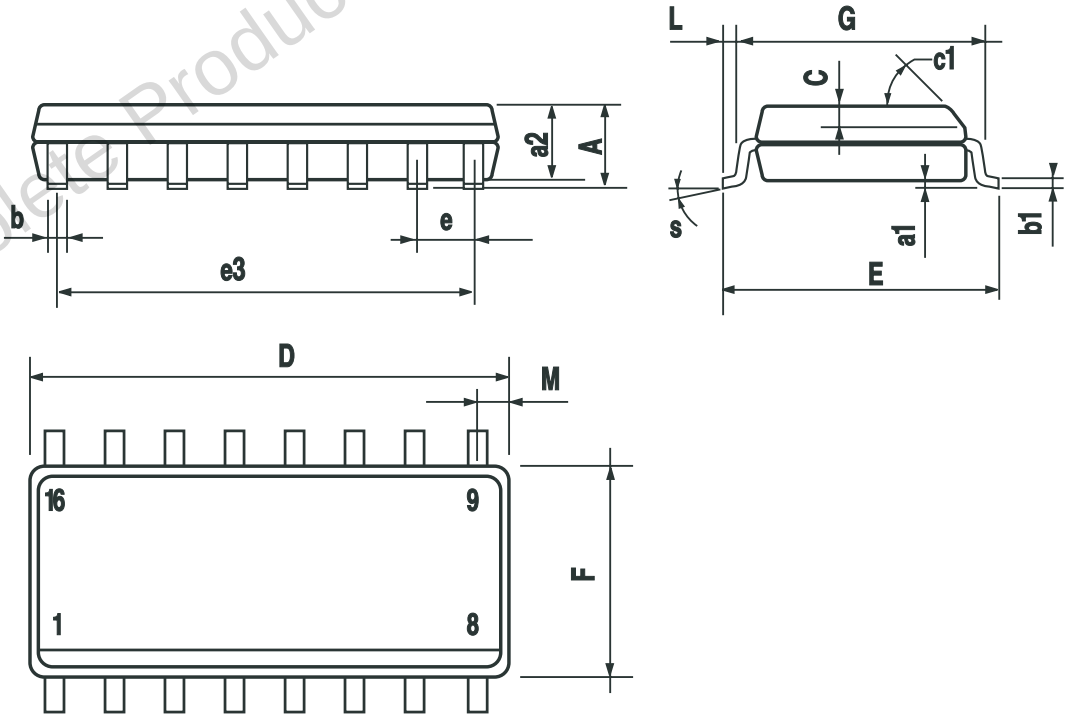
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H