

MC74HC4094A

8-Bit Shift and Store Register

High-Performance Silicon-Gate CMOS

The MC74HC4094A is a high speed CMOS 8-bit serial shift and storage register. This device consists of an 8-bit shift register and latch with 3-state output buffers. Data is shifted on positive clock (CP) transitions. The data in the shift register is transferred to the storage register when the Strobe (STR) input is high. The output buffers are enabled when the Output Enable (OE) input is set high. Two serial outputs (QS₁, QS₂) are available for cascading multiple devices.

Features

- Wide Operating Voltage Range: 2.0 to 6.0 V
- Low Power Dissipation: I_{CC} = < 10 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

Typical Applications

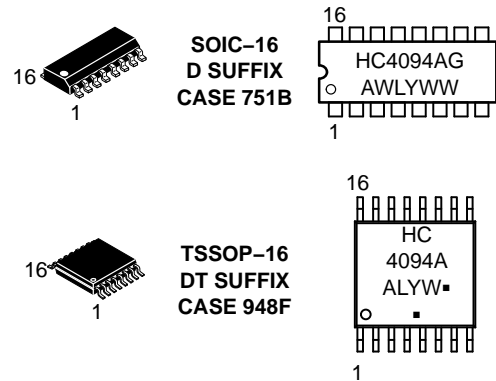
- Serial-to-Parallel Conversion
- Remote Control Storage Register



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MARKING DIAGRAMS



SOIC-16
D SUFFIX
CASE 751B

TSSOP-16
DT SUFFIX
CASE 948F

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G, ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

MC74HC4094A

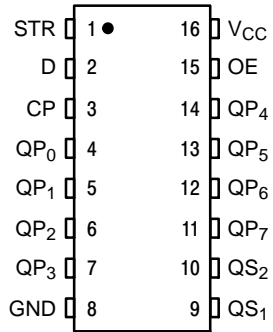


Figure 1. Pin Assignment

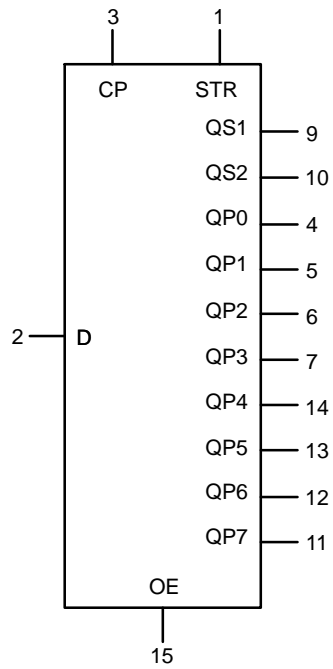


Figure 2. Logic Symbol

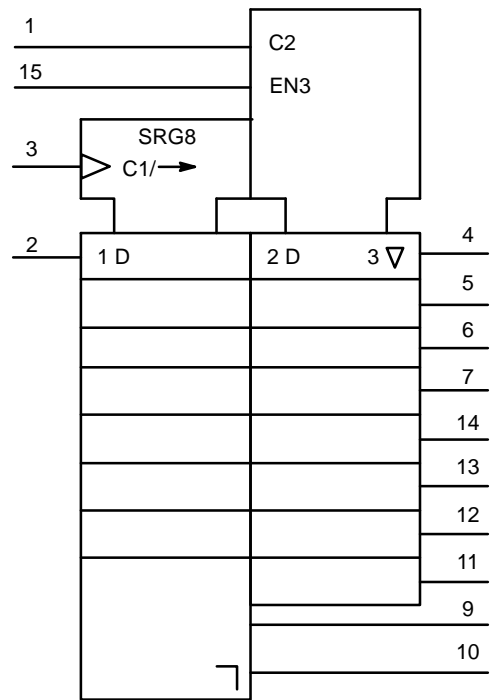


Figure 3. IEC Logic Symbol

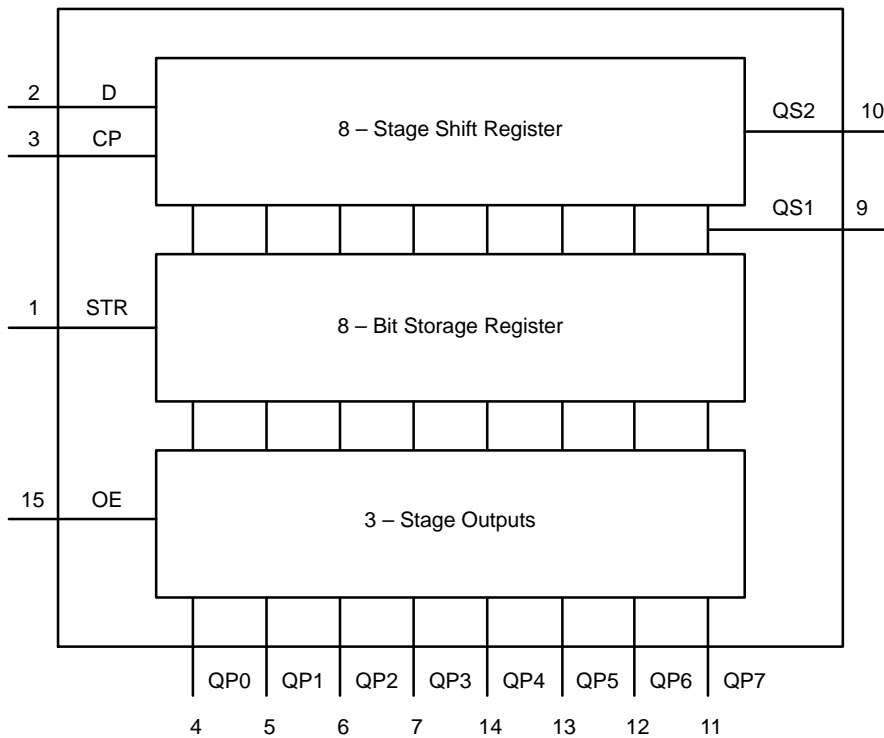


Figure 4. Functional Diagram

MC74HC4094A

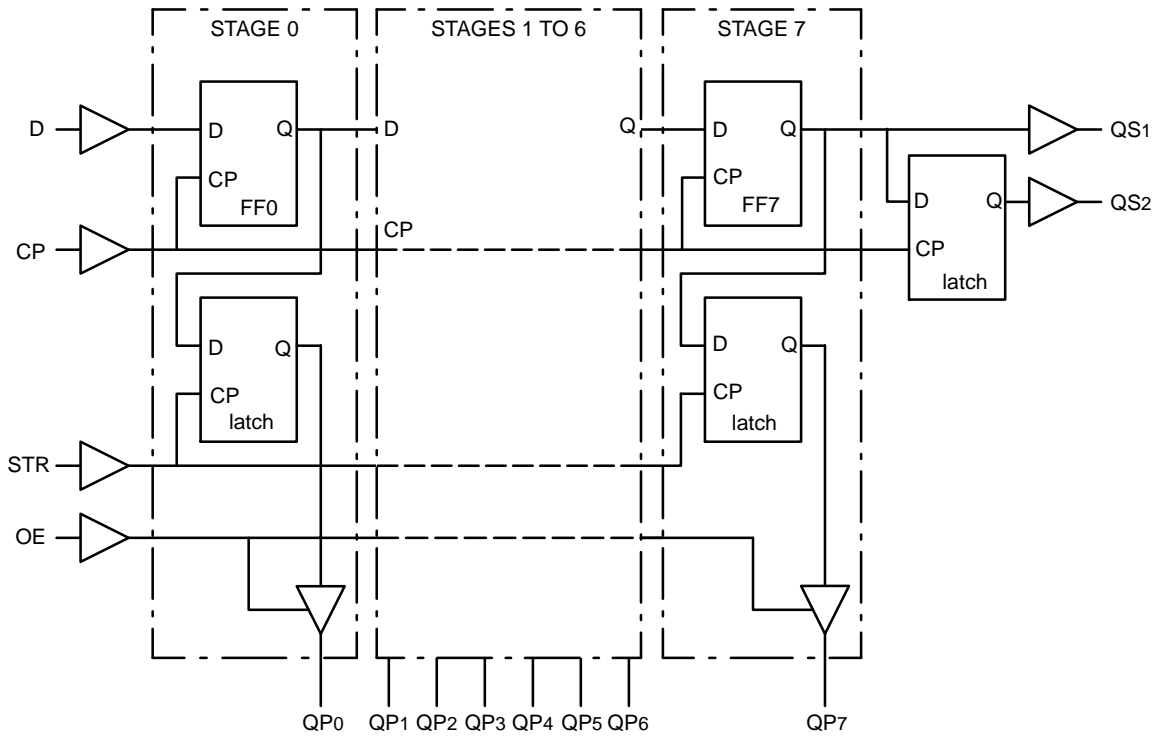


Figure 5. Logic Diagram

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 35 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA |
| P_D | Power Dissipation in Still Air, SOIC Package† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature | - 65 to + 150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating - SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|--|-----|----------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t_r, t_f | Input Rise and Fall Time (Figure 1) | | | ns |
| | $V_{CC} = 2.0 \text{ V}$ | 0 | 1000 | |
| | $V_{CC} = 4.5 \text{ V}$ | 0 | 500 | |
| | $V_{CC} = 6.0 \text{ V}$ | 0 | 400 | |

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FUNCTIONAL TABLE

| INPUTS | | | | PARALLEL OUTPUTS | | SERIAL OUTPUTS | |
|--------|----|-----|---|------------------|-------|----------------|-----|
| CP | OE | STR | D | QP0 | QPn | QS1 | QS2 |
| ↑ | L | X | X | Z | Z | Q'6 | NC |
| ↓ | L | X | X | Z | Z | NC | QP7 |
| ↑ | H | L | X | NC | NC | Q'6 | NC |
| ↑ | H | H | L | L | QPn-1 | Q'6 | NC |
| ↑ | H | H | H | H | QPn-1 | Q'6 | NC |
| ↓ | H | H | H | NC | NC | NC | QP7 |

Notes

- H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state
 NC = no change
 ↑ = LOW-to-HIGH CP transition
 ↓ = HIGH-to-LOW CP transition
 Q'6 = the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge

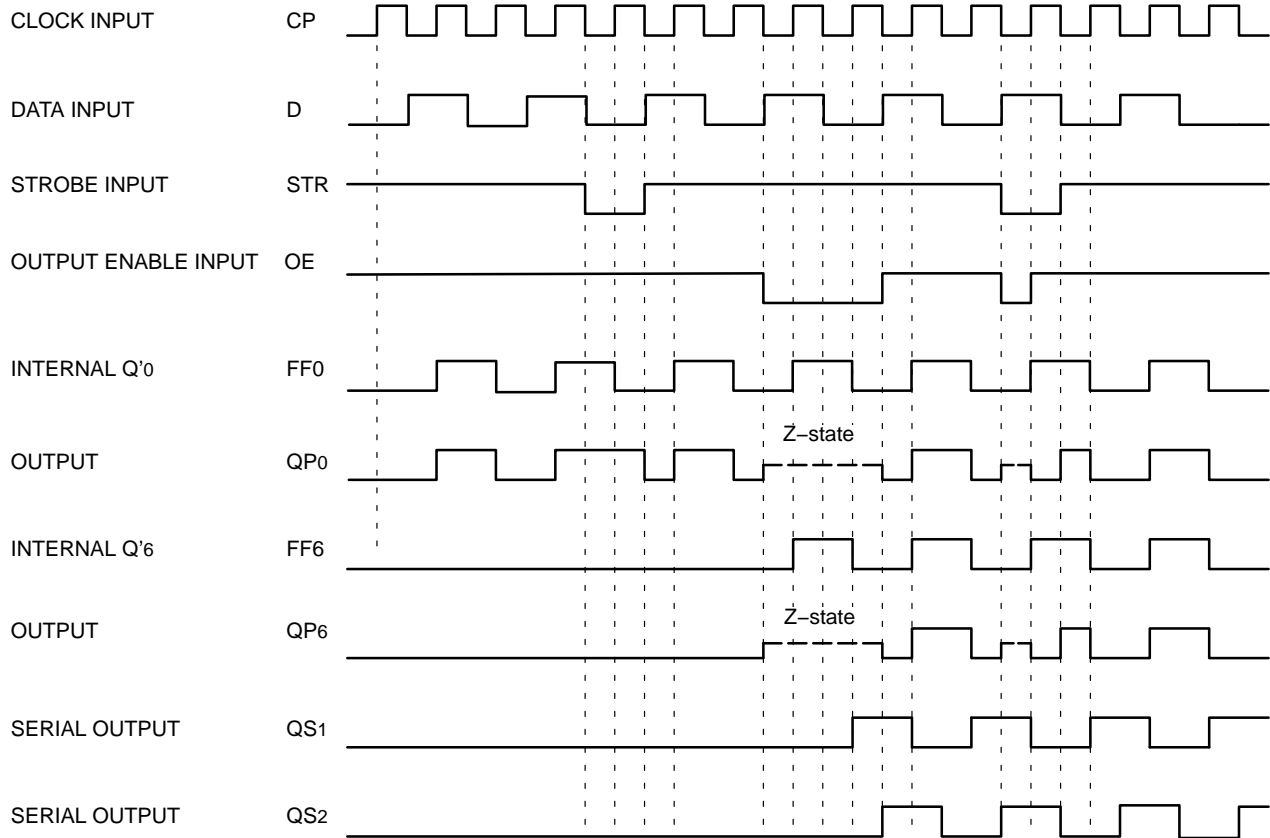


Figure 6. Timing Diagram

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DC CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | Guaranteed Limits | | | Unit |
|-----------------|--|---|---------------------|-------------------|--------|---------|------|
| | | | | -55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 3.0 | 2.9 | 2.9 | 2.9 | |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 2.4 mA | 3.0 | 2.75 | 2.7 | 2.6 | |
| | | V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4 mA | 4.5 | 4.25 | 4.2 | 4.1 | |
| | | V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 5.2 mA | 6.0 | 5.75 | 5.7 | 5.6 | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 3.0 | 0.1 | 0.1 | 0.1 | |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 2.4 mA | 3.0 | 0.25 | 0.3 | 0.4 | |
| | | V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4 mA | 4.5 | 0.25 | 0.3 | 0.4 | |
| | | V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 5.2 mA | 6.0 | 0.25 | 0.3 | 0.4 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = V _{CC} or GND | 6.0 | ±0.1 | ±1 | ±1 | μA |
| I _{OZ} | Maximum Tri-State Output Leakage Current | V _{IN} = V _{CC} or GND V _{OUT} = V _{CC} or GND | 6.0 | ±0.5 | ±5 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 6.0 | 4.0 | 40 | 80 | μA |

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AC CHARACTERISTICS ($t_f = t_r = 6 \text{ ns}$, $C_L = 50 \text{ pF}$)

| Symbol | Parameter | Test Conditions | V _{CC} (V) | Guaranteed Limits | | | Unit |
|-------------------------------------|---|-----------------|---------------------|-------------------|--------|---------|------|
| | | | | -55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PHL} , t _{PLH} | Maximum Propagation Delay CP to QS ₁ | Figure 7 | 2.0 | 120 | 150 | 170 | ns |
| | | | 3.0 | 90 | 100 | 110 | |
| | | | 4.5 | 30 | 38 | 45 | |
| | | | 6.0 | 26 | 33 | 38 | |
| t _{PHL} , t _{PLH} | Maximum Propagation Delay CP to QS ₂ | Figure 7 | 2.0 | 120 | 150 | 170 | ns |
| | | | 3.0 | 90 | 100 | 110 | |
| | | | 4.5 | 27 | 34 | 41 | |
| | | | 6.0 | 23 | 29 | 35 | |
| t _{PHL} , t _{PLH} | Maximum Propagation Delay CP to QP _n | Figure 7 | 2.0 | 120 | 150 | 170 | ns |
| | | | 3.0 | 90 | 100 | 110 | |
| | | | 4.5 | 39 | 49 | 59 | |
| | | | 6.0 | 33 | 42 | 50 | |
| t _{PHL} , t _{PLH} | Maximum Propagation Delay STR to QP _n | Figure 8 | 2.0 | 120 | 150 | 170 | ns |
| | | | 3.0 | 90 | 100 | 110 | |
| | | | 4.5 | 36 | 45 | 54 | |
| | | | 6.0 | 31 | 38 | 46 | |
| t _{PZH} , t _{PZL} | Maximum 3-State Output Enable Time OE to QP _n | Figure 9 | 2.0 | 120 | 140 | 160 | ns |
| | | | 3.0 | 80 | 100 | 120 | |
| | | | 4.5 | 35 | 44 | 53 | |
| | | | 6.0 | 30 | 37 | 45 | |
| t _{PHZ} , t _{PLZ} | Maximum 3-State Output Enable Time OE to QP _n | Figure 9 | 2.0 | 100 | 120 | 140 | ns |
| | | | 3.0 | 70 | 90 | 110 | |
| | | | 4.5 | 25 | 31 | 38 | |
| | | | 6.0 | 21 | 26 | 32 | |
| t _{THL} , t _{TLH} | Maximum Output Transition Time | Figure 7 | 2.0 | 70 | 90 | 110 | ns |
| | | | 3.0 | 40 | 60 | 80 | |
| | | | 4.5 | 18 | 22 | 25 | |
| | | | 6.0 | 16 | 19 | 22 | |
| t _w | Minimum Clock Pulse Width High or Low | Figure 7 | 2.0 | 80 | 100 | 120 | ns |
| | | | 3.0 | 50 | 60 | 80 | |
| | | | 4.5 | 16 | 20 | 24 | |
| | | | 6.0 | 14 | 17 | 20 | |
| t _w | Minimum Strobe Pulse Width High | Figure 8 | 2.0 | 80 | 100 | 120 | ns |
| | | | 3.0 | 50 | 60 | 80 | |
| | | | 4.5 | 16 | 20 | 24 | |
| | | | 6.0 | 14 | 17 | 20 | |
| t _{SU} | Minimum Set-up Time D to CP | Figure 10 | 2.0 | 50 | 65 | 75 | ns |
| | | | 3.0 | 30 | 35 | 45 | |
| | | | 4.5 | 10 | 13 | 15 | |
| | | | 6.0 | 9 | 11 | 13 | |

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AC CHARACTERISTICS ($t_f = t_r = 6 \text{ ns}$, $C_L = 50 \text{ pF}$)

| Symbol | Parameter | Test Conditions | V _{CC} (V) | Guaranteed Limits | | | Unit |
|------------------|--|-----------------|---------------------|-------------------|--------|---------|------|
| | | | | -55°C to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{SU} | Minimum Set-up Time CP to STR | Figure 8 | 2.0 | 100 | 125 | 150 | ns |
| | | | 3.0 | 60 | 75 | 90 | |
| | | | 4.5 | 20 | 25 | 30 | |
| | | | 6.0 | 17 | 21 | 26 | |
| t _h | Minimum Hold Time D to CP | Figure 10 | 2.0 | 3 | 3 | 3 | ns |
| | | | 3.0 | 3 | 3 | 3 | |
| | | | 4.5 | 3 | 3 | 3 | |
| | | | 6.0 | 3 | 3 | 3 | |
| t _h | Minimum Hold Time CP to STR | Figure 8 | 2.0 | 0 | 0 | 0 | ns |
| | | | 3.0 | 0 | 0 | 0 | |
| | | | 4.5 | 0 | 0 | 0 | |
| | | | 6.0 | 0 | 0 | 0 | |
| f _{MAX} | Minimum Clock Pulse Frequency | Figure 7 | 2.0 | 6 | 5 | 4 | MHz |
| | | | 3.0 | 18 | 14 | 12 | |
| | | | 4.5 | 30 | 24 | 20 | |
| | | | 6.0 | 35 | 28 | 24 | |
| C _{in} | Maximum Input Capacitance | | - | 10 | 10 | 10 | pF |
| C _{out} | Maximum Output Capacitance | | - | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Note 2) | | - | 140 | 140 | 140 | pF |

2. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:
 $I_{CC(\text{operating})} \approx C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where N_{SW} = total number of outputs switching and f_{IN} = switching frequency.

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AC WAVEFORMS

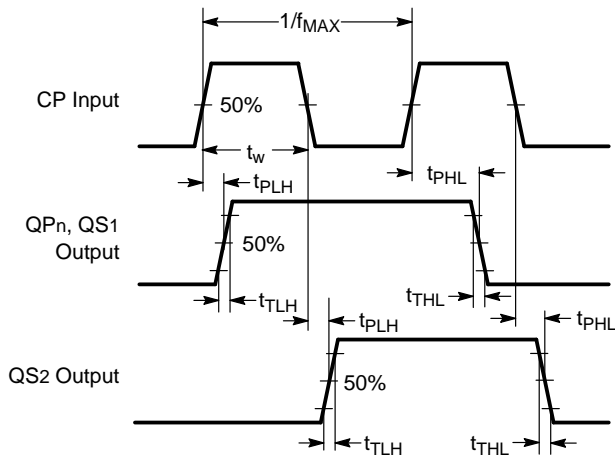


Figure 7. Waveforms showing the clock (CP) to output (QPn, QS1, QS2) propagation delays, the clock pulse width and the maximum clock frequency.

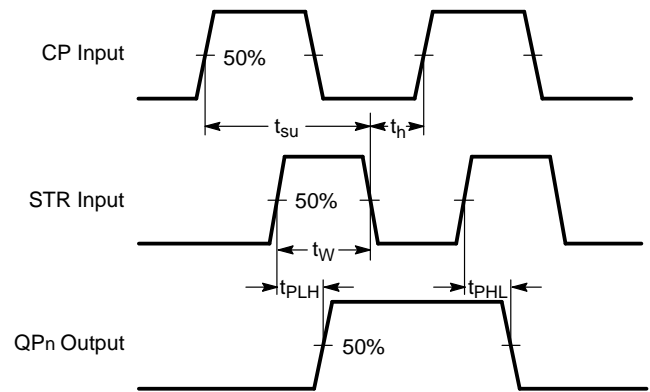


Figure 8. Waveforms showing the strobe (STR) to output (QPn) propagation delays, the strobe pulse width, the clock set-up and hold times for the strobe input.

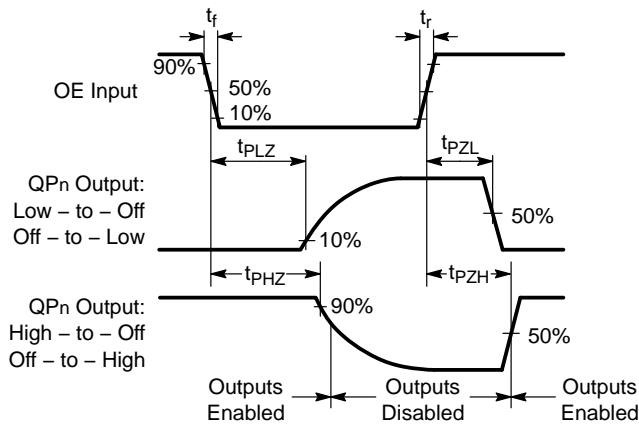
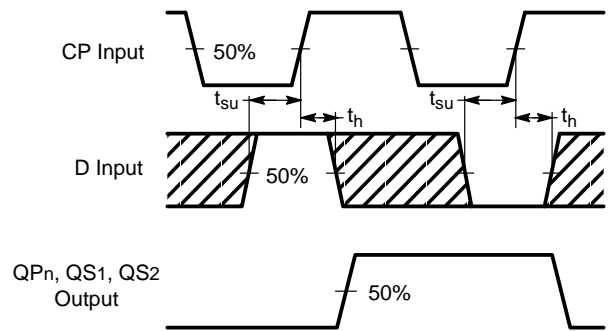


Figure 9. Waveforms showing the 3-state enable and disable times for input OE.



The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 10. Waveforms showing the data set-up and hold times for the data input.

MC74HC4094A

TEST CIRCUITS

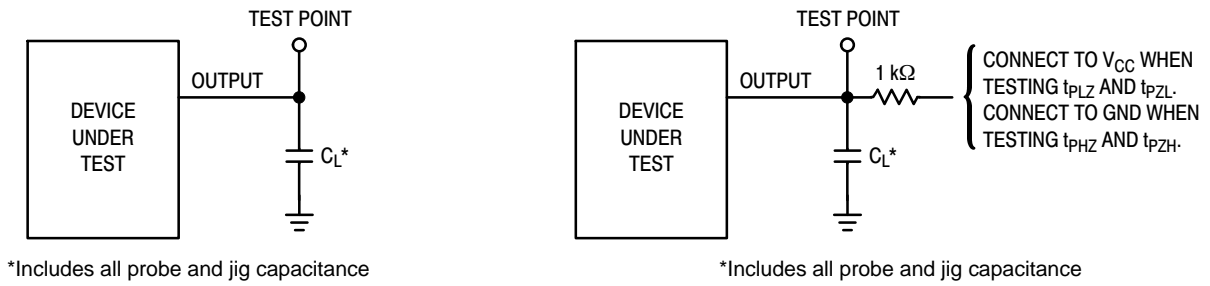


Figure 11. AC Characteristics Load Circuits

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|-----------------------|--------------------|
| MC74HC4094ADG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC74HC4094ADR2G | SOIC-16 (Pb-Free) | 2500 / Tape & Reel |
| MC74HC4094ADTG | TSSOP-16 (Pb-Free) | 96 Units / Rail |
| MC74HC4094ADTR2G | TSSOP-16 (Pb-Free) | 2500 / Tape & Reel |
| NLVHC4094BDTR2G* | TSSOP-16 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



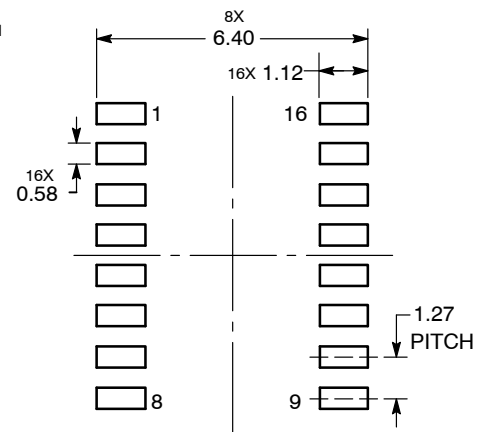
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

SOLDERING FOOTPRINT



| | | |
|------------------|-------------|--|
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| DESCRIPTION: | SOIC-16 | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16
CASE 948F-01
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

| | | |
|------------------|-------------|--|
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