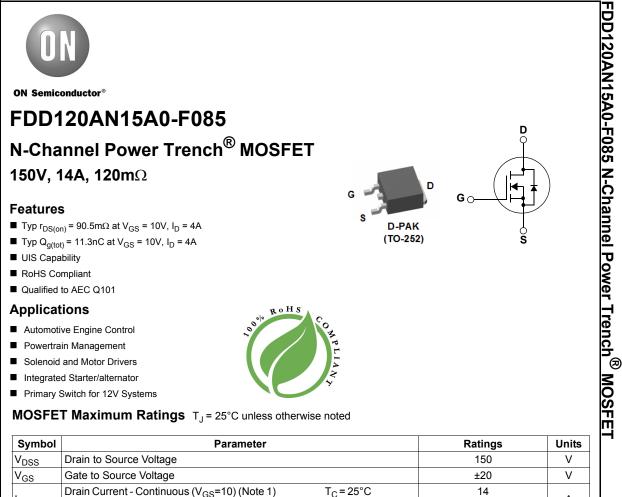
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V <sub>GS</sub>	Gate to Source Voltage		±20	V
	Drain Current - Continuous (V <sub>GS</sub> =10) (Note 1)	T <sub>C</sub> =25°C	14	Α
D	Pulsed Drain Current	T <sub>C</sub> = 25°C	See Figure4	A
E <sub>AS</sub>	Single Pulse Avalanche Energy	(Note 2)	122	mJ
Р	Power Dissipation		65	W
P <sub>D</sub>	Derate above 25°C		0.43	W/ºC
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case		2.3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient	(Note 3)	52	°C/W

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD120AN15A0	FDD120AN15A0-F085	D-PAK(TO-252)	330mm	12mm	2500 units

Notes:

1: Current is limited by bondwire configuration.

2: Starting  $T_J = 25^{\circ}C$ , L = 27mH,  $I_{AS} = 3A$ ,  $V_{DD} = 100V$  during inductor charging and  $V_{DD} = 0V$  during time in avalanche 3:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

Symbol	Parameter	Test	Conditions	Min	Тур	Мах	Units
Off Cha	racteristics						
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250μA, V	/ <sub>GS</sub> = 0V	150	-	-	V
	Drain to Source Leakage Current	V <sub>DS</sub> =150V,		-	-	1	μA
IDSS	Drain to Source Leakage Current	$V_{GS} = 0V$	T <sub>J</sub> = 175 <sup>o</sup> C(Note 4	) -	-	1	mA
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS}$ = ±20V		-	-	±100	nA
V <sub>GS(th)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 4A,	T <sub>J</sub> = 25 <sup>o</sup> C	-	90.5	120	mΩ
	racteristics						
	Drain to Source On Resistance	$V_{GS} = V_{DS}, I_D$ $I_D = 4A,$	T <sub>J</sub> = 25 <sup>o</sup> C		90.5	120	mΩ
r <sub>DS(on)</sub>	Diam to Source On Resistance	V <sub>GS</sub> = 10V	T <sub>J</sub> = 175 <sup>o</sup> C(Note 4	) -	227	302	mΩ
Dynami C <sub>iss</sub> C <sub>oss</sub>	Input Capacitance	– V <sub>DS</sub> = 25V, V	u <sub>GS</sub> = 0V,	-	743 85	-	pF pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f = 1MHz		-	20	-	pF
R <sub>g</sub>	Gate Resistance	f = 1MHz		-	3.4	-	Ω
Q <sub>g(ToT)</sub>	Total Gate Charge at 10V	$V_{GS} = 0$ to 10	)V V <sub>DD</sub> = 75V	-	11.3	14	nC
	Threshold Gate Charge	V <sub>GS</sub> = 0 to 2\	/ I <sub>D</sub> = 4A	-	1.4	1.6	nC
$Q_{q(th)}$	Osta ta Osuma Osta Ohanna			-	3.1	-	nC
Q <sub>g(th)</sub> Q <sub>gs</sub>	Gate to Source Gate Charge				1	1	nC

# **Switching Characteristics**

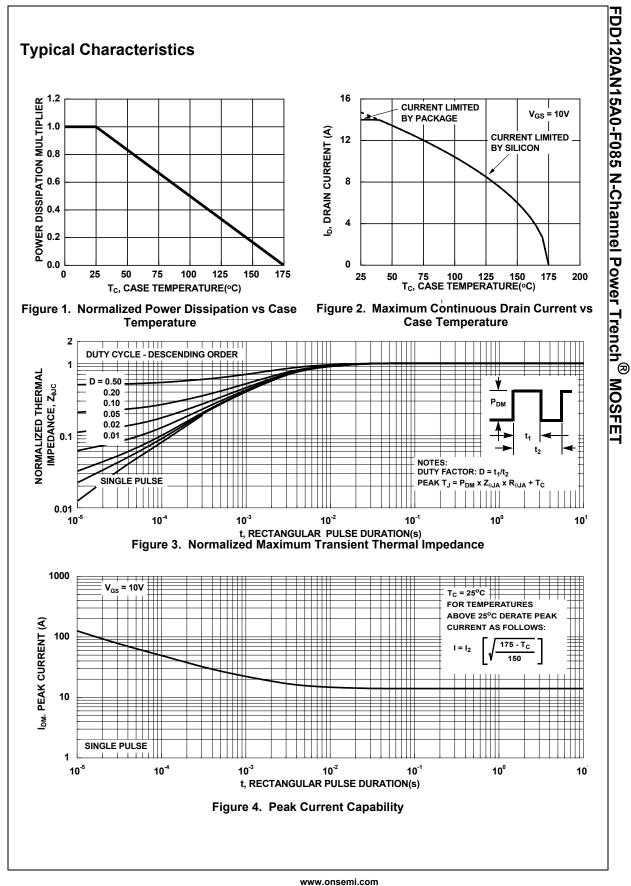
t <sub>on</sub>	Turn-On Time		-	-	31	ns
t <sub>d(on)</sub>	Turn-On Delay Time		-	14	-	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 75V, I <sub>D</sub> = 4A,	-	13	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{DD}$ = 75V, I <sub>D</sub> = 4A, V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 24Ω	-	34	-	ns
t <sub>f</sub>	Fall Time		-	15	-	ns
t <sub>off</sub>	Turn-Off Time		-	-	59	ns

# **Drain-Source Diode Characteristics**

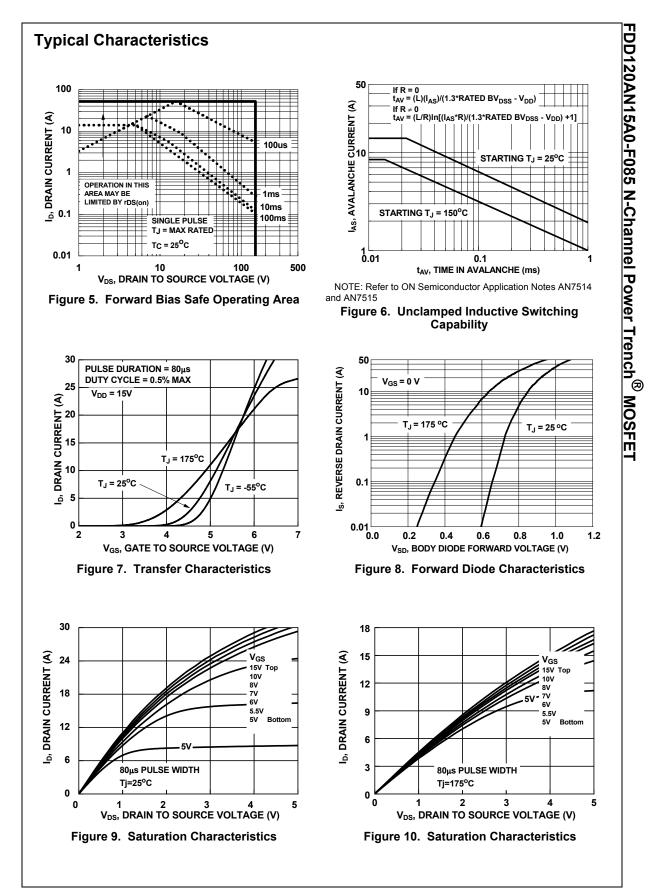
V <sub>SD</sub> Source to Drain Diode Voltage	Source to Drain Diade Voltage	$I_{SD}$ = 4A, $V_{GS}$ = 0V	-	-	1.25	V
	Source to Drain Diode voltage	$I_{SD}$ = 2A, $V_{GS}$ = 0V	-	-	1.2	V
T <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 4A, dI <sub>SD</sub> /dt = 100A/μs,	-	46	60	ns
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> =120V	-	94	108	nC

Notes:

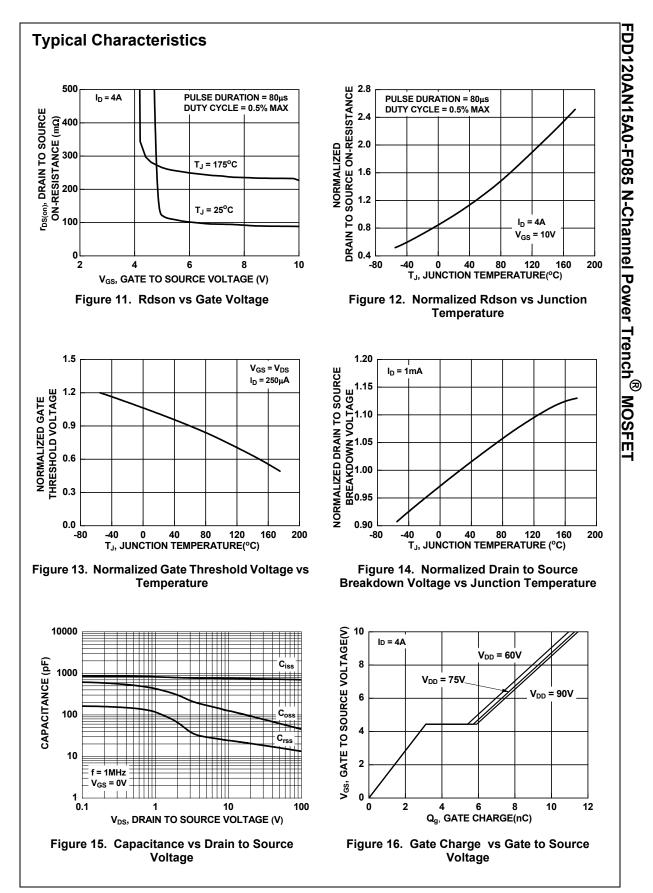
4: The maximum value is specified by design at  $T_J$  = 175°C. Product is not tested to this condition in production.



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